

# Three-channel CMOS transimpedance amplifier for LiDAR sensor receiver

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**Abstract:** For time-of-flight (TOF) light detection and ranging (LiDAR), a three-channel high-performance transimpedance amplifier (TIA) with high immunity to input load capacitance is presented. A regulated cascade (RGC) as the input stage is at the core of the complementary metal oxide semiconductor (CMOS) circuit chip, giving it more immunity to input photodiode detectors. A simple smart output interface acting as a feedback structure, which is rarely found in other designs, reduces the chip size and power consumption simultaneously. The circuit is designed using a 0.5  $\mu\text{m}$  CMOS process technology to achieve low cost. The device delivers a 33.87 dB $\Omega$  transimpedance gain at 350 MHz. With a higher input load capacitance, it shows a -3 dB bandwidth of 461 MHz, indicating a better detector tolerance at the front end of the system. Under a 3.3 V supply voltage, the device consumes 5.2 mW, and the total chip area with three channels is 402.8 $\times$ 597.0  $\mu\text{m}^2$  (including the test pads).

**Keywords:** transimpedance amplifier (TIA), three-channel, regulated cascade (RGC), light detection and ranging (LiDAR).

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## 1. Introduction

Target detection, advanced driver assistance systems (ADAS), and autonomous piloted driving are application examples of light detection and ranging (LiDAR) technologies that have sparked a lot of interest recently. However, these applications require low-cost, low-power, and compact three-dimensional LiDARs [1–3]. For detecting and processing the reflected signals from targets, LiDAR uses laser light to characterize targets across a scene [4,5]. Laser, atmospheric optics, target and environment features, radars, mechatronics, and computer technologies are used simultaneously in LiDARs [6,7]. The so-called time-of-flight (TOF) sensors, which measure the transit time ( $\Delta T$ ) of a laser pulse to the target and back to the receiver, are used in advanced rapidly-growing

LiDAR sensors with imaging capacity. The pulsed TOF methods, however, rely on the use of short, generally ns-scale laser pulses, necessitating the employment of precise wide-band signal processing techniques [8–10].

The design of a generic type of TOF consists of a pulsed laser transmitter, photodetector and receiver optics, and a preamplifier and comparator (CMP) receiving device [11]. Then, the ranging result is obtained through the time-to-digital converter (TDC) and field programmable gate array (FPGA) data processing. The reflected LiDAR signal of the target is usually a Gaussian pulse. Its level varies widely as a function of the distance. For the best accuracy, the LiDAR receiver requires wide bandwidth and appropriate gain amplifier. Also, the gain should be as controlled as possible to minimize degradation of the signal to noise ratio (SNR) before any distortion occurs [12].

LiDAR systems often use arrays of light-emitting diodes (LEDs), avalanche photodiode detectors (APDs), or laser diodes (LDs) to diffusely illuminate targets in the scene. Due to their basic electro-optical architecture and low-cost implementations, these sensors appear to have sparked a lot of attention [13]. However, the parasitic capacitance of some types of APDs in these sensors is in the range of 1 pF to 10 pF [14], although most researchers use a 2 pF standard as the usual detector capacitance [15,16]. As a result, for the LiDAR receiving system, a preamplifier insensitive to the parasitic capacitance of the detectors must be considered during design.

As shown in Fig. 1, the preamplifier is the key module in the front-end receiver of the LiDAR system. It transforms and amplifies the photodetector's weak current signal into a voltage signal. Because the preamplifier has such a strong influence on system requirements such as sensitivity, speed, and stability, selecting the circuit settings for the best performance necessitates extensive design work. As a front-end circuit, a voltage-mode inverter (INV) TIA has been conventionally utilized

[17–19]. However, due to the intrinsic design trade-off between gain and bandwidth (BW), the INV-transimpedance amplifier (TIA) gain is limited, which may result in a significant noise rise and sensitivity loss [20]. This would lead to a shorter detection range unless laser power is increased. In general, TIA is utilized in preamplifiers. However, in this paper, we propose a novel diode metal oxide semiconductor (MOS) feed-forward TIA. As a result, the three-channel TIA parallel array in 0.5  $\mu\text{m}$  CMOS technology provides a low-cost and low-area solution for the front-end receiver in LiDAR applications, thanks to its strong immunity to the parasitic capacitance of the detectors.

The rest of the paper is organized as follows. Section 2 describes the TIA's construction and operation, as well as its characteristics. Section 3 shows the layout design and simulation results. Section 4 summarizes the test results obtained with the entire chip. Section 5 concludes the paper with a summary of the findings.

## 2. System design

The three-channel TIA which comprises a micro-optic module, a three-channel parallel optical receiver preamplifier amplifier and a dummy amplifier is shown in Fig. 1. Three-channel parallel input optical signals are connected to a three-channel photo-detector, which converts these optical signals to electric current signals and transmits them to three-channel preamplifiers to produce output signals.

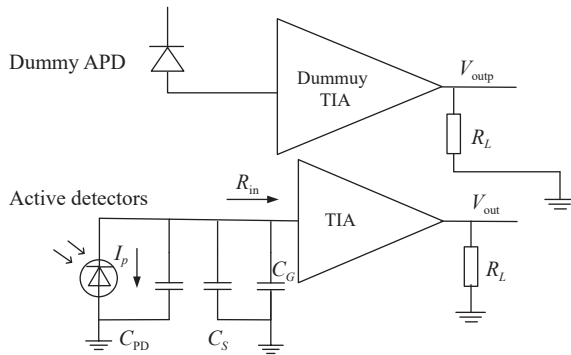


Fig. 1 Proposed three-channel transimpedance preamplifier

Fig. 1 and Fig. 2 depict the schematic of the proposed transimpedance preamplifier.  $R_L$  is the load resistance,  $V_{\text{out}}$  is the dummy output voltage, and  $V_{\text{out}}$  is the real output voltage. The photodetector is represented by current source  $I_p$ .  $C_{\text{PD}}$  may be treated as the parasitic capacitance of the photodiode, which is in the range of 1 pF to 10 pF.  $C_s$  and  $C_G$  denote the parasitic capacitance of transimpedance preamplifier.  $C_{\text{PD}} + C_s + C_G = C_T$ .  $R_{\text{in}}$  is the equivalent input resistance.

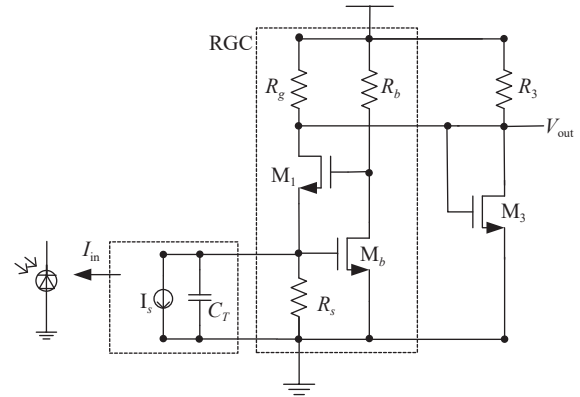


Fig. 2 Schematic of the proposed diode MOS feedforward TIA

CMOS  $M_1$  and  $M_b$ , resistance  $R_g$ ,  $R_s$ , and  $R_b$  constitute an RGC input stage. A diode MOS  $M_3$  is selected to operate as the feedforward to the regulated cascode (RGC) to maximize the transconductance and increase the gain BW.

The design criteria for TIAs in LiDAR systems include variable transimpedance gain, low input impedance, and wide BW for narrow-pulse recovery, low noise current spectral density for weak reflected signal detection, and low power dissipation per channel for chip reliability.

### 2.1 Input impedance

As the common-gate input stage, transistors  $M_1$  and  $M_b$  and the resistance  $R_g$  is the RGC stage, the bias voltage of  $M_1$  is provided by the common-source stage: transistor  $M_b$  and resistance  $R_b$ . The RGC input stage is stable enough thanks to the feedback loop. Fig. 3 shows the small-signal equivalent circuit of RGC structure, and the equivalent input resistance  $R_{\text{in}}$  is shown as follows:

$$I_{\text{in}} = -g_{m_1} V_1 = -g_{m_1} (V_b - V_{\text{in}}), \quad (1)$$

$$V_b = -g_{m_b} V_{\text{in}} R_b, \quad (2)$$

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{1}{g_{m_1} (1 + g_{m_b} R_b)}, \quad (3)$$

where  $I_{\text{in}}$  is the equivalent input current,  $g_{m_1}$  is the transconductance of  $M_1$ .  $V_1$  is the voltage of  $M_1$ .  $V_b$  is the voltage of the resistance  $R_b$ .  $V_{\text{in}}$  is the input voltage.  $g_{m_b}$  is the transconductance of  $M_b$ .

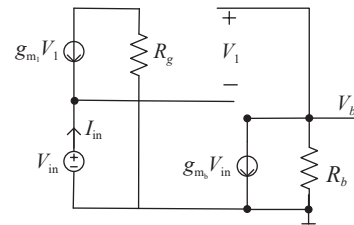


Fig. 3 Small signal equivalent circuit of RGC

The circuit shows current stability as a result of the feedback. When the  $M_1$  drain source current increases, the voltage difference  $R_s$  increases, the CMOS  $M_b$  gate voltage increases, and the  $M_b$  source current increases. As a result, the voltage difference  $R_s$  grows larger, and the  $M_b$  gate voltage decreases. Therefore, the source current of  $M_1$  decreases and it stabilizes the DC operating point of the circuit.

## 2.2 Transimpedance gain

The basic structure of the preamplifier is the voltage parallel negative feedback with  $R_f$ , as shown in Fig. 4(a), in the direct current (DC) case, its closed-loop gain is  $-R_f$ . However, in most CMOS technologies, perfectly controlled resistance levels or precise and suitable physical dimensions are difficult to achieve. Therefore, instead of a feedback resistance, a diode-connected MOS structure of  $M_3$  is used in this paper, as shown in Fig. 4(b). Its impedance is roughly  $1/g_{m3}$ , where  $g_{m3}$  is the transconductance  $M_3$ . The  $M_3$  not only ensures chip processing accuracy but also reduces the layout area. This type of feedback is uncommon in other designs. When the process parameters are fixed, the aspect ratio of  $M_3$  can be decreased to increase the circuit's gain.

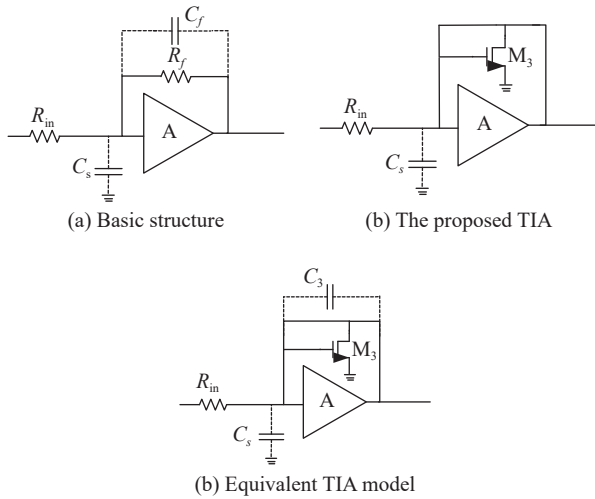


Fig. 4 Basic structure of the proposed diode MOS feedforward TIA

## 2.3 BW

Usually, the bandwidth of the RGC circuit is given as

$$BW = 1/2\pi R_g C_{d1}$$

where  $C_{d1}$  is the drain capacitance of  $M_1$ . Based on the resistance and capacitance parameters of the detector, the equivalent load diagram of the preamplifier circuit

designed in this work is shown in Fig. 1 and Fig. 4. In Fig. 4(a),  $C_s$  and  $R_f$  introduce a zero-point in the amplitude-frequency plot of the closed-loop system which affects the stability of the circuit. To compensate the zero point, the normal technique is to add a compensated capacitance, as shown in Fig. 4(a). A compensation capacitor  $C_f$  is connected in parallel to  $R_f$  to form a phase complement between the  $R_{in}C_f$  and  $R_fC_s$  networks. Thus, a pole  $P_0$  is generated into the amplitude-frequency plot. The frequency of the pole is  $f=1/2\pi R_f C_f$ . Therefore, the pole counteracts the influence of the zero point, thus keeping the whole loop stable. The parasitic capacitance  $C_3$  of  $M_3$  can also be employed as a compensation capacitor, thanks to the bulk effect of the diode connection  $M_3$  presented in this study. Consequently, the BW of the circuit is

$$f = g_{m3}/2\pi C_3$$

where  $C_3$  is proportional to the length and width of  $M_3$  pipeline channel. Here,  $M_3$  and  $R_3$  should be carefully chosen in the circuit, hence giving rise to the well-known design tradeoff between gain (which is directly proportional to  $M_3$  channel length) and BW (which is inversely proportional to the input resistance and thus to  $M_3$ ).

## 2.4 Noise

Using Kirchhoff's current law, the input-referred equivalent noise power spectral density of the TIA shown in Fig. 5 can be calculated using

$$i_{n,eq}^2 = \frac{4kT}{R_s} + \frac{4kT}{R_g} + \frac{4kT}{R_3} + 2qI_1 + 2qI_3 + 2qI_{gb} + 4kT\gamma g_{m1} \left[ \frac{(1 + \omega C_t R_s)^2}{(1 + g_{m1} R_s)^2 + (\omega C_t R_s)^2} \right] + \frac{4kT\gamma}{g_{m_b}} \left[ \frac{1}{R_s} + (\omega C_t)^2 \right] + \frac{4kT\gamma}{g_{m_3}} \left[ \left( \frac{1}{R_s} + \frac{1}{R_1} \right)^2 + \omega^2 (C_{gs3} + C_{gd1} + C_{gd3})^2 \right] \quad (4)$$

where  $C_t = C_{gdb} + C_{gs1}$ ,  $\gamma = 2/3$ ,  $k$  is Boltzmann constant,  $T$  is the absolute temperature.  $C_{gsb}$ ,  $C_{gdb}$ ,  $C_{gs1}$ ,  $C_{gd1}$ ,  $C_{gs3}$ , and  $C_{gd3}$  represent the gate-source capacitances and the gate-drain capacitances of  $M_b$ ,  $M_1$ , and  $M_3$ .  $q$  is the electronic charge quantity,  $I_1$  is the average DC of  $M_1$ ,  $I_3$  is the average DC of  $M_3$ ,  $I_{gb}$  is the average DC of  $M_b$ , and  $w = g_{m1}/c_{gs1}$ . Equation (4) indicates that the thermal noise of  $R_1$ ,  $R_3$ , and  $R_g$  is dominant at low frequencies whereas  $g_{m1}$ ,  $g_{m_b}$ , and  $g_{m_3}$  become the critical factors to determine the high-frequency noise. There are two main approaches for improving noise performance as follows: increasing

$R_1$ ,  $R_3$ , and  $R_g$  lowers the low-frequency noise. Increasing  $M_b$ 's gate width improves  $g_{mb}$ 's value, hence  $M_b$ 's gate width has an optimum value for achieving the smallest equivalent input noise current power spectrum density. The values of  $g_m$ , on the other hand, should be carefully chosen to maximize the design tradeoff between input resistance, bandwidth, and high-frequency noise.

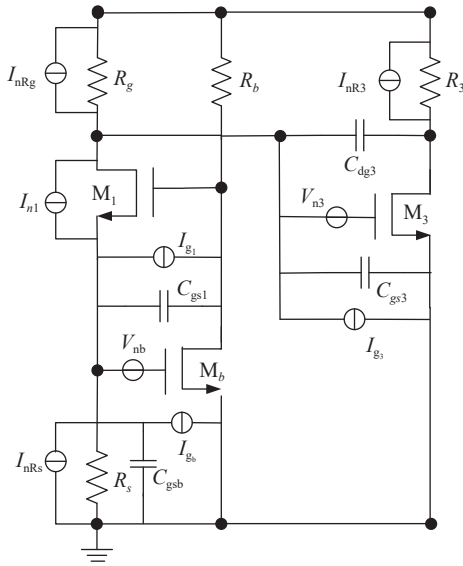


Fig. 5 Equivalent noise model of the TIA

### 3. Layout design and simulation results

Post-layout simulations are performed for the proposed diode MOS feedforward TIA by using the model parameters of a 0.5  $\mu\text{m}$  CMOS technology. The post layout is shown in Fig. 6. The number of pads is kept at 11, which accounts for more than a third of the entire design space for ease of testing.

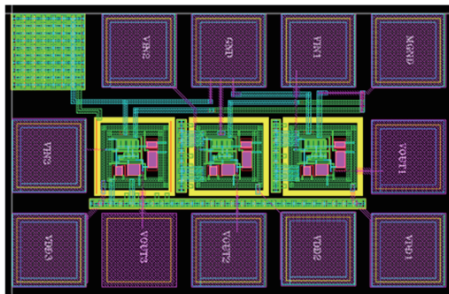


Fig. 6 Three-channel parallel array layout

The total area of the layout is  $402.8 \times 597.0 \mu\text{m}^2$ . The total power consumption is 5.2 mW under 3.3 V voltage operation. The photodiode is electrically modeled as a current source with a parasitic capacitance of 5 pF and 10 pF, and parasitic resistance of 50  $\Omega$  in simulations to

demonstrate that the diode MOS feedforward TIA has good immunity to its input photodiode capacitance. The parasitic capacitance from the input/output (I/O) pads and the electro-static discharge (ESD) protection diodes are included in the simulations. Table 1 and Fig. 7 present the simulation results.

Table 1 Three channel post-layout simulation results (100 MHz)

Channel	Input $C_s$ /pF	Bandwidth/ MHz	Output voltage/V	Noise/ ( $\text{pA} \cdot \text{s}^{-1}$ )	Gain/ $\text{dB}\Omega$
1	5	739.9	0.4–2	3.051	41.01
2	5	750.7	0.4–2	3.058	40.09
3	5	827.7	0.4–2	3.049	41.03
1	10	612.8	0.5–2	3.749	40.09

For Table 1, typical nMOS and typical pMOS in corner analysis are conducted at 27°C. There are three channels in this design, and the performance of each channel is tested respectively. It can be seen from the first three rows that the performance of the three channels is basically the same. When the capacitance of 5 pF is added at the input end, the chip BW is greater than 700 MHz and the input noise performance is stable. From the comparison of the first line with the last line, it can be seen that even if the load capacitance is increased by up to 10 pF at the input, the chip bandwidth is greater than 600 MHz, and the noise performance is basically stable.

From Fig. 7 and Table 1, it is clearly seen that the diode MOS feedforward TIA achieves transimpedance gain and lower noise current spectral density, which can meet the essential design requirements of LiDAR. In other words, the product of transimpedance gain and BW is greatly improved while the noise penalty is minimal. It is also worth noting that the input dynamic range is 60 dB, and the power supply rejection ratio (PSRR) is 50 dB.

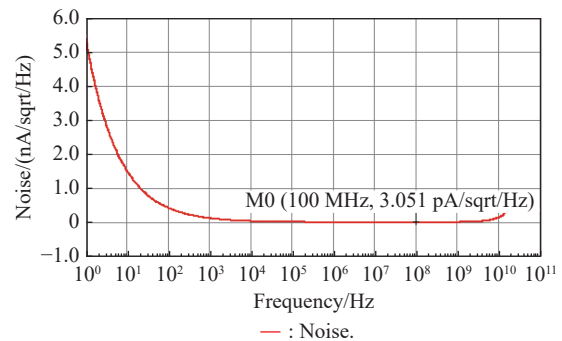
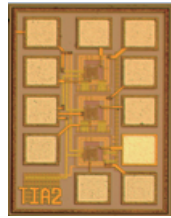


Fig. 7 Post-layout simulated input noise current spectral density of the TIA

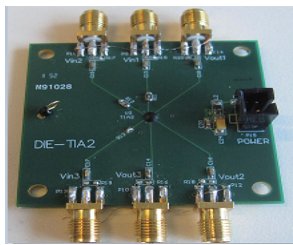
### 4. Measurement data

This diode MOS feedforward TIA is fabricated in the 0.5  $\mu\text{m}$  standard CMOS technology. Fig. 8(a) shows a

chip photomicrograph of the preamplifier. The printed circuit board (PCB) is shown in Fig. 8(b).



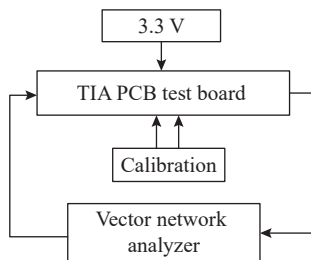
(a) Preamplifier chip photomicrograph



(b) PCB test board

**Fig. 8 Images of the chips**

After finishing the design, the performance of the front-end preamplifier is tested and verified in an Agilent open laboratory setup using the test PCB. Fig. 9 shows the schematic diagram of the test setup. The transimpedance gain and bandwidth are measured by generating a single-ended current signal from a 50 Ω output of Agilent vector network analyzer (E5071C) with a resistive attenuator. Fig. 10 shows the measured S-parameters ( $S_{21}$  and  $S_{11}$ ) responses.



**Fig. 9 Schematic diagram of the gain and bandwidth measurement**



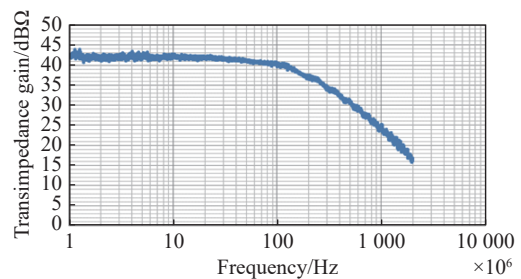
(a)  $S_{21}$  parameter



(b)  $S_{11}$  parameter

**Fig. 10 Measured S-parameters**

The transimpedance gain plot can be obtained as shown in Fig.11 with 5 pF parasitic capacitance load [21] as follows:  $|Z_{TIA}| = |Z_0| \times |S_{21}| / |1 - S_{11}|$ . The transimpedance gain is evaluated to be 33.87 dBΩ and the -3 dB BW is 461 MHz.  $Z_0$  is 50 Ω.



**Fig. 11 Gain response of the TIA**

Fig. 12 shows the measured noise spectrum from the Agilent spectrum analyzer (N9020MAX), which has the basic noise of -166 dBm. It can also be used to calculate the equivalent input noise current spectral density. The equivalent input noise current spectral density of the preamplifier is found to be 26.17 Pa/√Hz.



**Fig. 12 Gain response of the TIA**

Table 2 compares the performance of the proposed TIA with other reported TIAs. The circuit in [12] shows better transimpedance gain performance than this work with the 5 pF input capacitance load. However, its -3 dB

BW is worse with large power consumptions. Compared to [17,18], the proposed TIA circuit has wider BW and lower power consumptions, indicating a better detector tolerance at the front end of the system.

**Table 2 Perform comparison of published TIA circuits**

Channel	The proposed circuit	[12]	[22]	[23]
Input $C_{in}$ /pF	5	5	1.5	2
$f_{-3dB}$ /MHz	461	170	150	50
Gain/dB $\Omega$	33.92	113	106	106
Power/mW	5.2	250	165	12.6
Chip size/mm <sup>2</sup>	0.4 $\times$ 0.6	3 $\times$ 3	0.9	–

## 5. Conclusions

A three-channel high-performance TIA has been designed and produced for use in the TOF LiDAR sensor receiver. Chip gain, 3 dB BW, noise, and other performance parameters are improved by using the RGC input structure and a diode-connected MOS output stage. In addition, CSMC 0.5 m CMOS technology is used to keep the chip's cost low. The TIA has high immunity to the parasitic capacitances of the detectors in the LiDAR receiving system, as demonstrated by the measured results. The entire chip integration of the array of receiving circuits for use in LiDAR is performed.

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