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A transceiver frequency conversion module based on 3D micropackaging technology

LIU Boyuan, WANG Qingping*, WU Weiwei, and YUAN Naichang

School of Electronic Science and Engineering, National University of Defense Technology, Changsha 410073, China

Abstract: The idea of Ku-band transceiver frequency conversion module design based on 3D micropackaging technology is proposed. By using the double frequency conversion technology, the dual transceiver circuit from Ku-band to L-band is realized by combining with the local oscillator and the power control circuit to complete functions such as amplification, filtering and gain. In order to achieve the performance optimization and a high level of integration of the Ku-band monolithic microwave integrated circuits (MMIC) operating chip, the 3D vertical interconnection micro-assembly technology is used. By stacking solder balls on the printed circuit board (PCB), the technology decreases the volume of the original transceiver to a miniaturized module. The module has a good electromagnetic compatibility through special structure designs. This module has the characteristics of miniaturization, low power consumption and high density, which is suitable for popularization in practical application.

Keywords: Ku-band, frequency conversion, 3D packaging, chip, electromagnetic compatibility.

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1. Introduction

After a long period of development, the wireless communication system has achieved a breakthrough in the performance and function improvement of millimeter wave and microwave devices [1]. As the core research content, the transceiver frequency conversion part of the wireless communication system is widely concerned and constantly improved.

However, it is difficult for a transceiver system to diversify its functions at the traditional technical level. Nowadays, transceiver systems demand more and more multifunctional and highly integrated devices [2]. Although the traditional transceiver system has good indexes, it usually has a large volume because it meets the indexes unilaterally, which is an obstacle to be solved when it is used to achieve miniaturization.

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*Corresponding author.

The 3D micropackaging can revolutionize the miniaturization of modules. Considering the available space in the vertical direction [3], this micropackaging technology greatly reduces the length and width. The 3D packaging possesses features of lightweight, compact, clear and convenient winding, as well as low cost from a systematic perspective.

In this paper, a new 3D vertically-connected ball grid array (BGA) structure module is constructed and designed, and micropackaging and integrated packaging technologies are adopted to improve the integration, meet the requirements of miniaturization design, and achieve the good electromagnetic compatibility [4]. Because the module has many functions, the test of each index is considered convenient and accurate.

2. Design idea of module

2.1 Design index of module

The transceiver frequency conversion module usually consists of the radio frequency (RF) amplification link, the local oscillator (LO) signal input circuit and the power control circuit. The transmitting chain can mix the intermediate frequency (IF) modulation signal and the LO signal to reach the carrier frequencies (CF), filter the clutter, and amplify useful signals to enough power, meeting the request of transmitting [5]. The receiving link can pass the weak signals received by the antenna through the low-noise amplifier (LNA), the filter, and then through the RF-LO mixer to realize frequency conversion down to IF baseband signals [6].

The frequency conversion module requires a range of RF output (RFo) signals of 17 GHz$\pm$1 GHz, a range of the 1st IF (IF1) signals of 3.5 GHz to 4.5 GHz, a range of the 2nd IF (IF2) signal of 2.0 GHz$\pm$50 MHz, a transmission link gain no less than 9 dB, and a compression point of 1 dB (P-1) no less than 10 dBm. The gain of the receiving link shall not be less than 20 dB, the noise figure shall

not be more than 4 dB at the room temperature, the output power of P-1 shall not be less than 5 dBm. Gain flatness should be less than 2 dB. The overall dimension is less than 25 mm×20 mm×6 mm. According to the index, this module is characterized by low noise, small volume and low power consumption. In order to meet such requirements, appropriate circuit design and device selection are needed.

The block diagram of the transceiver model is shown in Fig. 1.

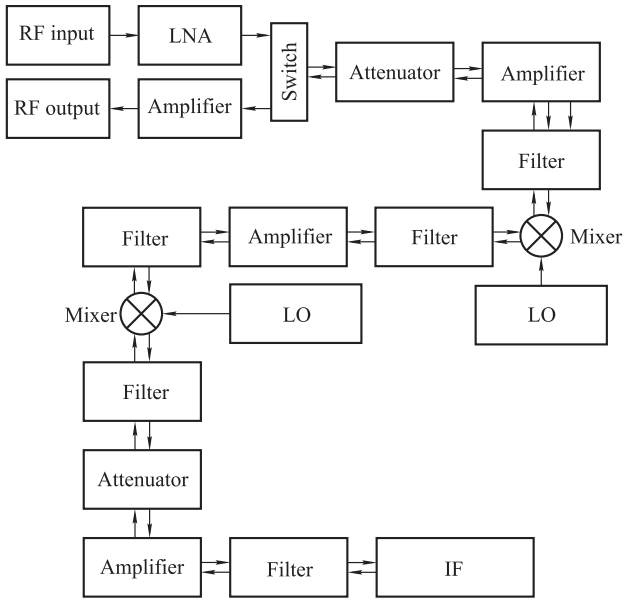


Fig. 1 Block diagram of the transceiver model

2.2 Parameter analysis and index allocation

As shown in Fig. 1, the down-conversion channel is composed of LNA, transceiver conversion switch, computer numerical control (CNC) attenuator, mixing IF amplifier, filter and other circuits [7]. It is used for front-end RF amplification of the receiving system, which determines the RF filtering characteristics and noise figure of the system.

In order to ensure the high rejection of mirror frequency signals and clutter, the circuit adopts a secondary frequency conversion scheme. Through a specific filter, the signal is converted from high frequency broadband to s-band and finally to narrow low frequency band. When switching to the transmission link, the up-conversion only needs to exchange the primary 1st LO (LO1) signal and 2nd LO (LO2) signal sweeping signals, and the frequency band can be widened to broadband. The receiving front-end amplifier needs to select a high gain to prevent the gain from being offset by the conversion loss of the back-end mixer and other factors, leading to noise deterioration [8]. Before the intermediate frequency output ends, it is necessary to select an amplifier with high P-1 and high gain, and try to prevent the signal close to saturation to be amplified with small amplitudes, resulting in power compression. Generally speaking, for the receiver, P-1 is affected by the former stage, but determined by the latter stage, and the influence of the former stage is only significant when P-1 and the saturation point are very close to each other [9].

By finding out the main clutter frequency after mixing the frequency of the two mixers, the appropriate filter is selected to suppress the clutter to the level of 40 dBc, and at the same time change the passband bandwidth to satisfy the frequency band index of the link end signal.

A design is made to reduce the circuit size and power consumption as far as possible [10].

3. Module circuit design

3.1 Design of frequency conversion link

By using the software CASCADE, the transmitting and receiving links as shown in Fig. 2, are designed to meet the requirements of the link.

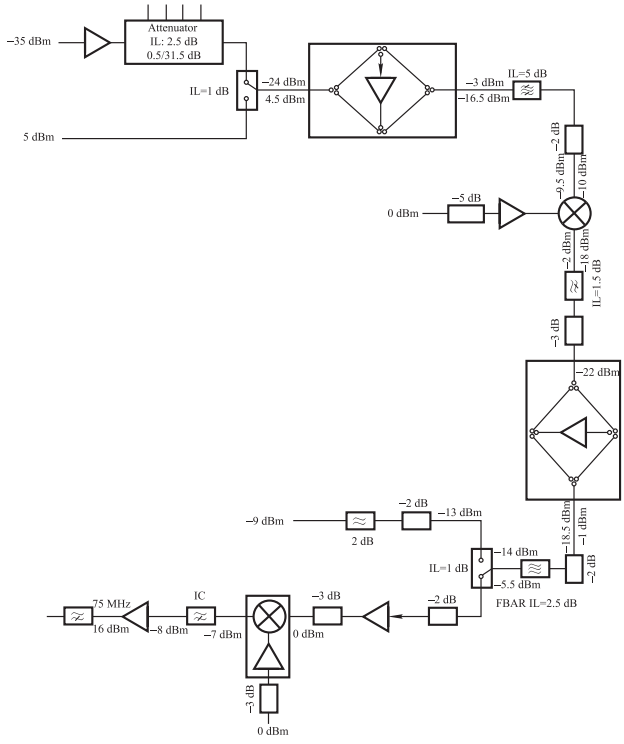


Fig. 2 Block diagram of the transceiver

3.1.1 Design of transceiver switch

The link design is integrated with the transceiver, and the bi-directional amplification design is adopted for common amplifiers. In order to reduce the volume, the selection of components should consider the chip as much as possible. The design of the switch plays a key role in the transceiver switch [11]. In the actual circuit, a driver is required to

logically control the switch to select the on-off of the transmitting or receiving link.

According to the principle, the single-pole double-throw switch is designed and simulated. The design requires the switch to work in 16 GHz to 18 GHz and the branch port isolation degree is greater than 30 dB.

The switch is modeled in the high frequency structure simulator (HFSS). When thrown to on-state, the diode can be equivalent to a resistance, and the bypass diode can be equivalent to a ground inductance to filter out low-frequency components [12]. In order to ensure the isolation degree of the two branches, the circuit board is designed by punching. The schematic diagram is shown in Fig. 3.

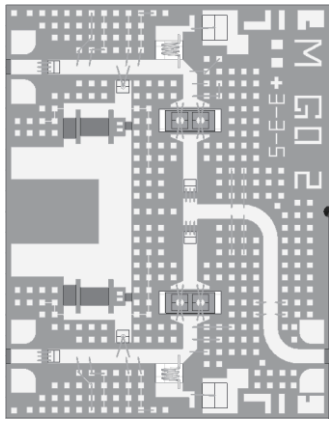


Fig. 3 Diagram of switch circuit HFSS model

Set port 1 of the two branches to be on with port 2 off. In the reference state, the plug loss and the port standing wave are simulated, and the results are shown in Fig. 4 and Fig. 5.

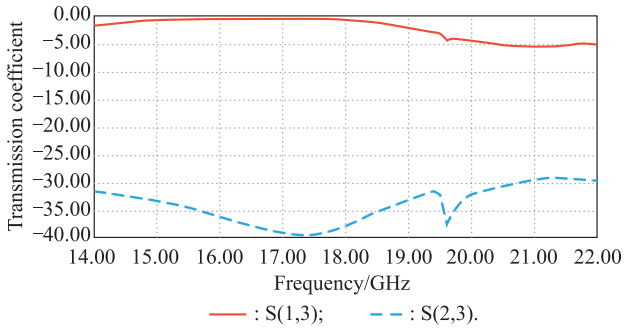


Fig. 4 Simulation result of transmission coefficient

The frequency band of 16 GHz to 18 GHz has a good standing wave, and port 1 presents a high isolation to port 2.

3.1.2 Design of MEMS filter

Microelectromechanical system (MEMS) is made of silicon wafer by lithography, anisotropy etching and inductively coupled plasma (ICP) etching [13]. The MEMS filter has the characteristics of small size, good performance, light weight and high reliability.

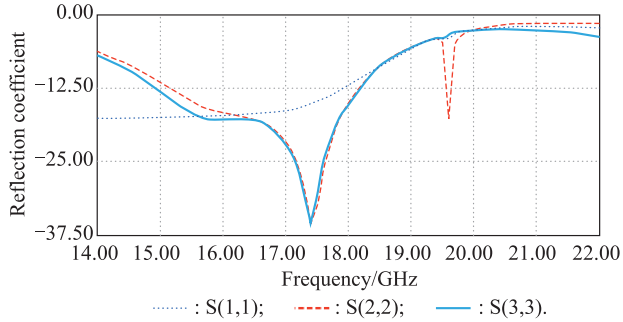


Fig. 5 Simulation result of reflection coefficient

When processing high frequency signals, the MEMS bandpass filter will generate out-of-band clutter at the N-time base wave frequency of the far-end of its similar bandwidth. Therefore, it is usually matched up with a low pass filter. Compared with the traditional filter, the MEMS bandpass filter has more energy storage, less loss, less plug loss and better rectangle coefficient [14].

Since the low-noise amplifier can only provide a gain of 11 dB to 12 dB, and the index requires that the noise figure of the single-channel mixing channel should not be more than 4 dB at the room temperature, this requires that the subsequent filter should have a low loss of less than 2 dB, otherwise the noise characteristics will be greatly affected.

By using modeling and simulation software HFSS and advanced design system (ADS), a class of MEMS bandpass filter chip is actually designed. Its bandpass is 15.9 GHz to 18 GHz, and the center plug loss is no more than 1.8 dB. The reflection coefficient is greater than 30 dB, and the out-of-band attenuation no less than 40 dB@15.00 GHz and 40 dB@19 GHz.

The HFSS model of the MEMS bandpass filter is shown in Fig. 6.

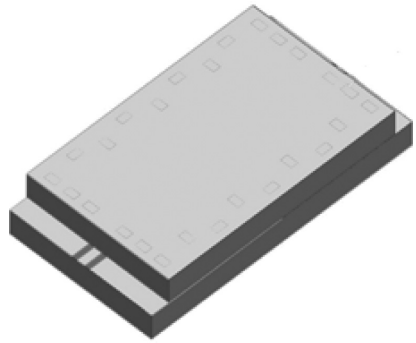


Fig. 6 HFSS model diagram of MEMS bandpass filter

The designed MEMS filter is processed and tested, and the test results of S(1,1) and S(2,1) are shown in Fig. 7.

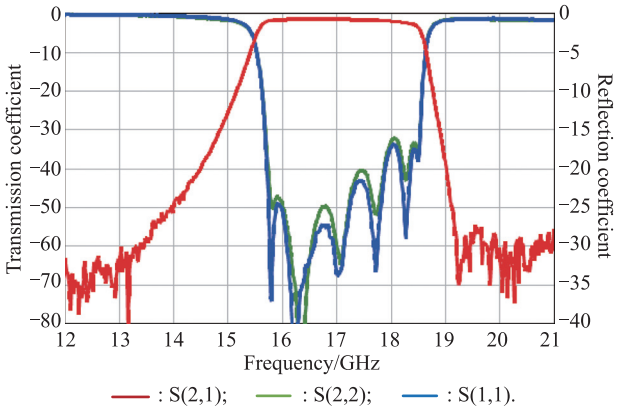


Fig. 7 Actual measurement results of MEMS bandpass filter chip

It can be seen that in the 15.9 GHz to 18 GHz frequency band, the signal transmission coefficient is very high, with center plug loss less than 1.5 dB, and the port reflection coefficient is more than 20 dB, with a good matching degree. The out-of-band attenuation of 40 dB also meets the corresponding design requirement.

3.1.3 Design of electrically modulated attenuator

The Ku-band electrically modulated attenuator model is shown in Fig. 8.

Standing waves of the port and electrical modulation attenuation are simulated in 16 GHz to 18 GHz, and the results are shown in Fig. 9 and Fig. 10. Fig. 10 shows the corresponding relationship of direct current (DC) with S(2,1) and the voltage standing wave ratio (VSWR), respectively.

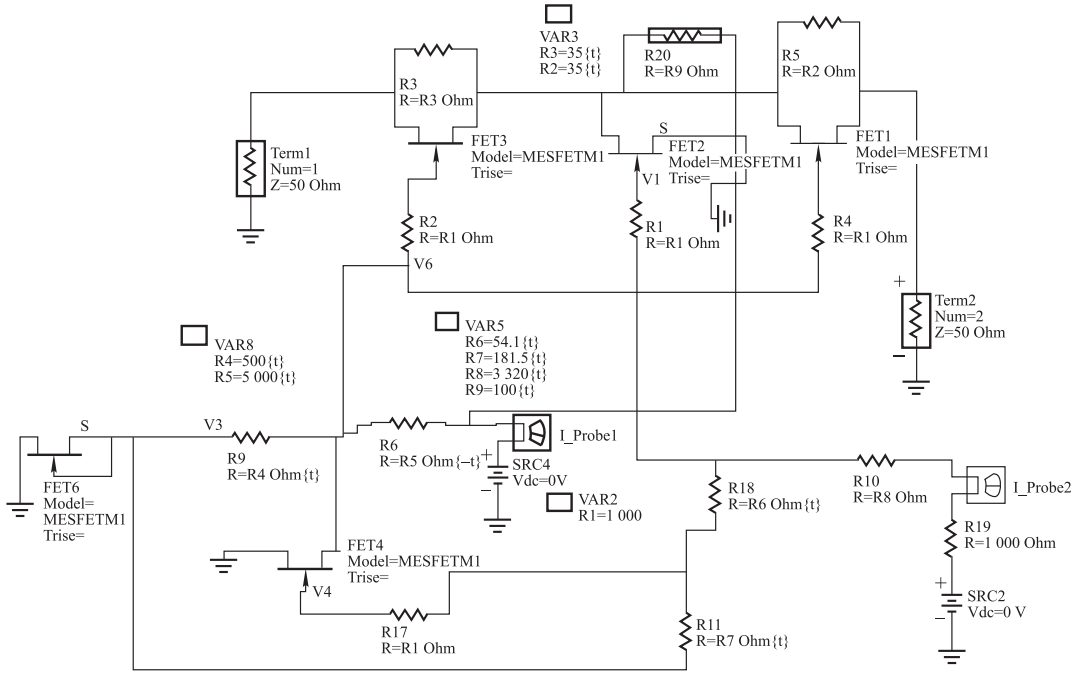


Fig. 8 Circuit model of electric attenuator

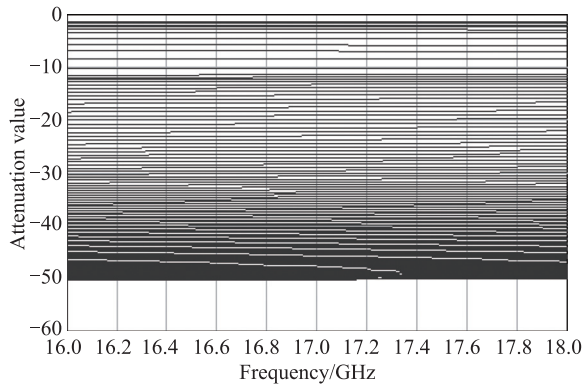
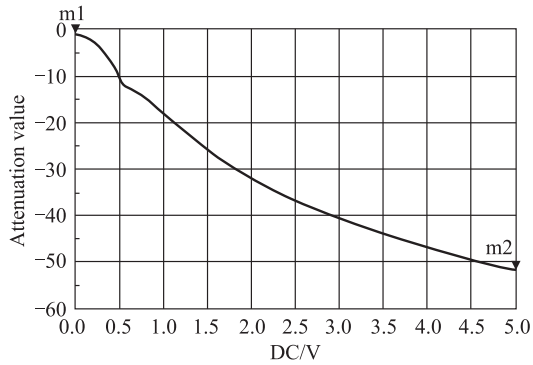
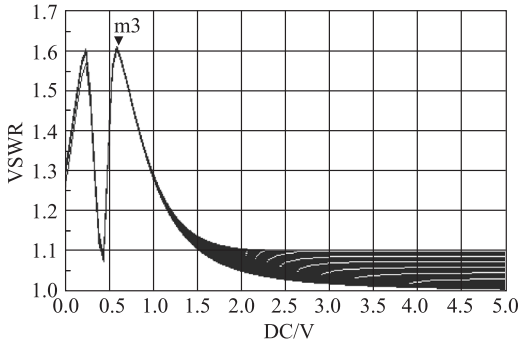


Fig. 9 Each attenuation value of the electric attenuator from 16 GHz to 18 GHz



(a) Transmission coefficient of attenuator model varied by DC



(b) VSWR of attenuator model varied by DC

m1 indep(m1)=0.000 plot_vs(dB(S2,1)),DC.V)=−1.098 Frequency=10.00 MHz	m2 indep(m2)=5.000 plot_vs(dB(S2,1)),DC.V)=−51.703 Frequency=2.110 GHz

m3
indep(m3)=0.600
plot_vs(VSWR1,DC.V)=1.614
Frequency=10.00 GHz

Fig. 10 S(2,1) parameter and its standing wave ratio

Based on the above results, in the frequency band of 16 GHz to 18 GHz, the flatness reaches 0.15 dB when the bias voltage is 3.6 V. The attenuation range of the attenuator is within 1.5 dB to 27 dB, and the input/output standing wave ratio is less than 1.62.

3.1.4 Design of amplifiers of each level

The coverage range of the electrically modulated attenuator is 0 dB to 27 dB. Therefore, in order to ensure that the final gain meets the requirements of the index, for the receiving link, the gain of the front-stage LNA is 26 dB. A total of three bi-directional amplifiers are added before and after two frequency conversions. At normal temperature, the gains are 24 dB, 13 dB and 14 dB, respectively. The bi-directional amplifier works at 195 mA, and the direction is controlled by a logic signal generated by the driver [15].

3.1.5 Design of amplifier mixing circuit

In order to reduce the volume, the Ku-band multifunction chip is adopted for amplifying the mixing circuit [16], which integrates mixers, RF amplifiers and up-down frequency conversion with a gain of around 11 dB. The LO isolation degrees of down-frequency conversion to IF and RF are more than 20 dB and 15 dB, respectively.

3.1.6 Design of IF filter

In order to reduce the size, the IF filter adopts the film bulk acoustic resonator (FBAR) filter chip, and the FBAR filter is constructed by the body acoustic resonator with high Q values [17]. Its fractional bandwidth can be in 1% to 5%, with the frequency range covering 1 950 MHz to 2 050 MHz. It is suitable for applications requiring low insertion loss, small size, large power capacity and fast roll-down of stopband [18].

Design indexes include a bandwidth of 100 MHz, a central insertion loss of no more than 5 dB, a far-end out-of-band suppression of no less than 15 dBc, and a near-end out-of-band suppression of no less than 40 dBc, with a size to be set within 8 mm×4.5 mm×0.8 mm.

In order to verify the IF filtering condition of the FBAR filter, the test curve results are shown in Fig. 11 within the bandwidth of 1.80 GHz to 2.20 GHz.

Because the FBAR filter can be utilized as a low frequency and narrow band filter, it is widely used in frequency conversion networks and successfully realizes the chipping of the filter [19].

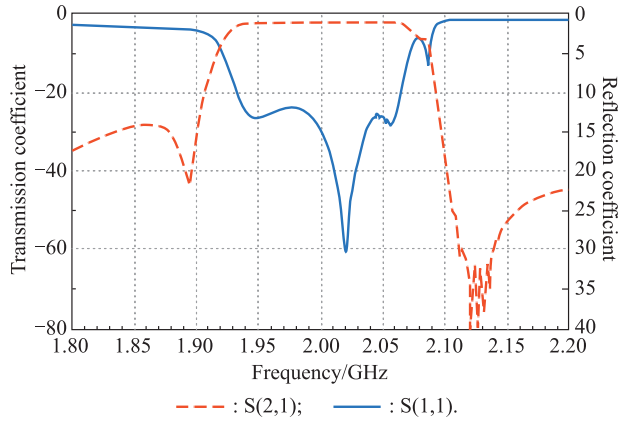


Fig. 11 S-parameter curve of medium frequency filtering of the FBAR filter

3.1.7 Design of IF amplifier

The amplifier chip is used for bi-directional amplification. The gain with the stability of temperature needs to be compensated by the temperature-compensating attenuator [20], which can guarantee the output power requirement of P-1 after adding the attenuator to the IF amplifier. The amplifier gain is designed as 24 dB. The VSWR of input and output is not more than 2.

3.2 Design of LO circuit

In order to completely drown the noise bottom signal, a drive amplifier with a gain of 14 dB is added at the back-end of the input signal to amplify the −2 dBm signal input from the signal source. Since the mixing chip is integrated with RF amplifiers and LO amplifiers, the LO isolation degree to RF is 40 dB, and the reverse isolation of the amplifier is more than 20 dB, which can ensure the leakage of RF signals through LO is less than −60 dB, thus ensuring the isolation between channels [21].

3.3 Design of power supply and circuit control

The control signal is low-voltage transistor-transistor logic (LVTTL) level, and the high level amplitude of the LVTTL

level is 3.3 V. The output driving capacity is good. The control circuit of positive-intrinsic-negative (PIN) switch also uses chip devices, so that all the devices used in the module are chip devices, greatly reducing the module size.

3.4 Design of structural layout

The BGA structure is designed to realize electrical interconnection by welding tin balls in regular arrays between the upper substrate and the lower substrate [22]. Microwave mixed pressure multilayer boards are generally adopted to mount the mother board, and the spacing of tin balls can be appropriately increased [23,24], as shown in Fig. 12.

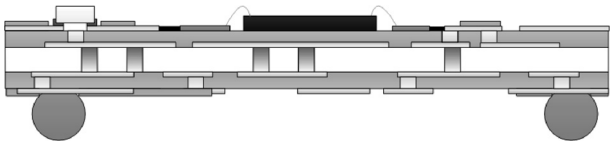


Fig. 12 Design structure of tin ball packer

Tin balls can play a shielding effect between devices with high integration [25]. In order to verify this theory, the lower layer of the circuit board is simulated in HFSS, as shown in Fig. 13.

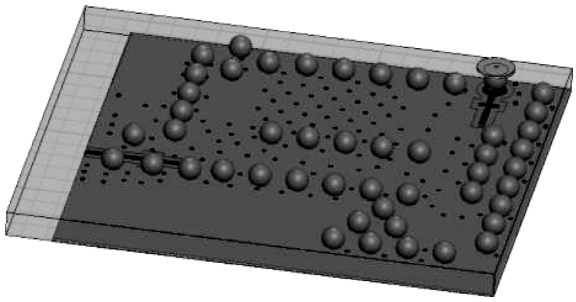


Fig. 13 HFSS model of tin ball packer shielding

Fig. 13 approximates the lower board of the circuit board [26]. The two enclosed dark parts in the figure are simulation test points, and the crosstalk between them is reflected by S parameter, as shown in Fig. 14.

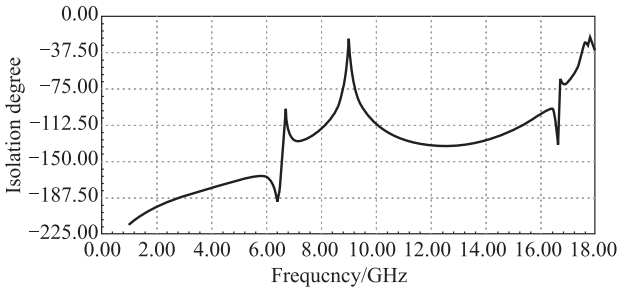
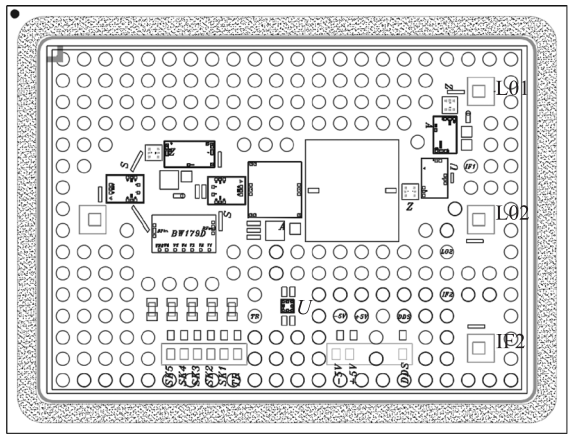


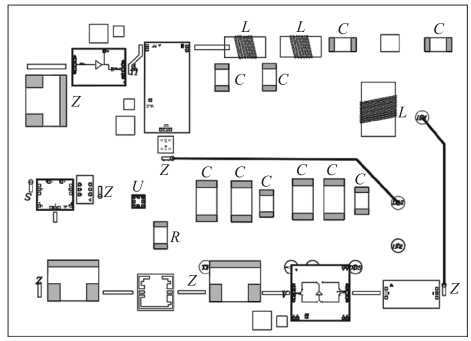
Fig. 14 Simulation results of shielding isolation degree S(1,2) of tin ball packer

It can be seen that the introduction of tin balls makes the isolation degree much greater than 25 dB, which meets the design requirements of electromagnetic compatibility and achieves high integration and miniaturization on the premise that the performance is not deteriorated [27].

In AutoCAD, the layout of components and the physical connection of circuits are designed in advance, and the design results are shown in Fig. 15.



(a) Components distribution of lower board



(b) Components distribution of upper board

Fig. 15 Component arrangement and physical connection of the circuit

4. Module processsing and testing

After processing, the object photo of the module is presented in Fig. 16.

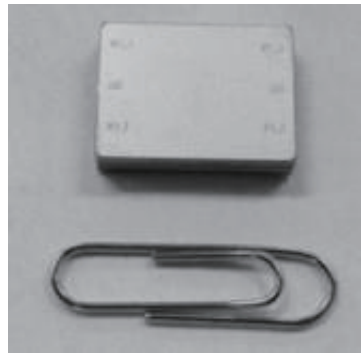


Fig. 16 Photo of module appearance

The noise test results of the receiving channel through signal input and DC power supply are shown in Fig. 17.

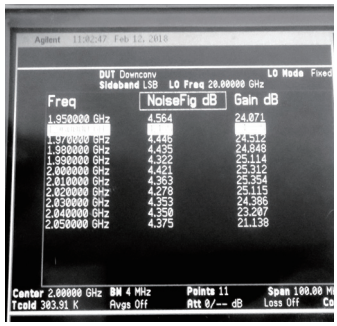


Fig. 17 Result of receiving channel noise test

It can be seen that the noise figure of the receiving channel is about 4.43 dB within the range of 1.95 GHz to 2.05 GHz, while the simulation results require the noise figure to be less than 4 dB. The noise deterioration is caused by the pipe and shell transition loss [28], along with the contact loss of the test fixture [29].

The P-1 of the receiving circuit of the module is tested by using the spectrum meter and the power meter. The test results are shown in Fig. 18.

It can be seen that the input power is -20 dBm, and the output power reaches the saturation state. Here, P-1 = 5.05 dBm $>$5 dBm, and the test results meet the requirements of the index. Fig. 19 shows P-1 of the transmitting channel.

Thus, when the input power is -8 dBm, the output power is 2.03 dBm, and the gain reaches 10.03 dB, which is more than 9 dB required by the design index.

The measured result of P-1 is 10.52 dBm, 2.48 dB smaller than the design requirement of 13 dBm. The actual measured line loss at about 17 GHz is about 1.5 dB, and the estimated test fixture loss is about 1 dB. Within the allowable error range, the results basically meet the design requirements.

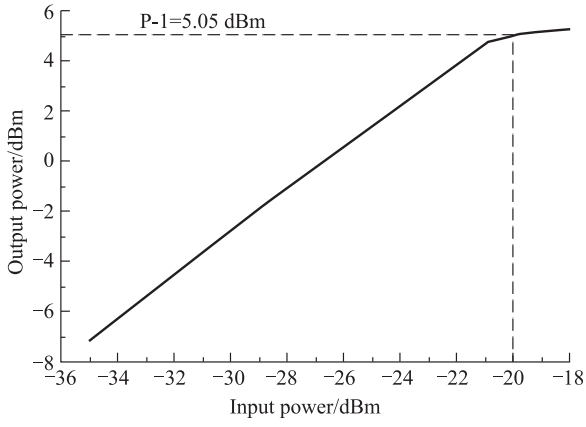


Fig. 18 P-1 curve of the receiving path

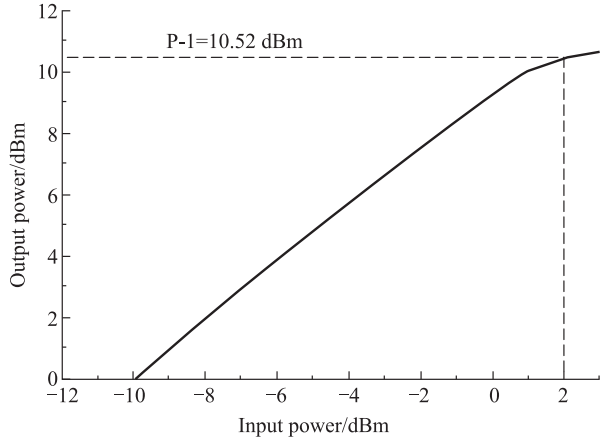


Fig. 19 P-1 curve of the transmitting path

Fig. 20 and Fig. 21 show the results of the gain, gain flatness and standing wave tests of the receiving and transmitting paths respectively.

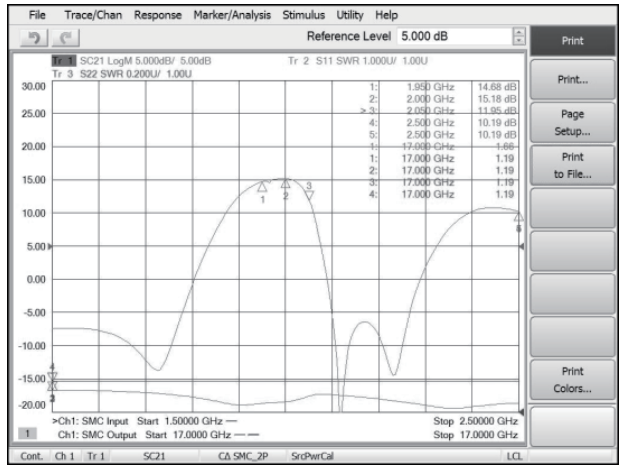


Fig. 20 Measured results of receiver input, output VSWR (VSWRi, VSWRo) and gain S(2,1) curves

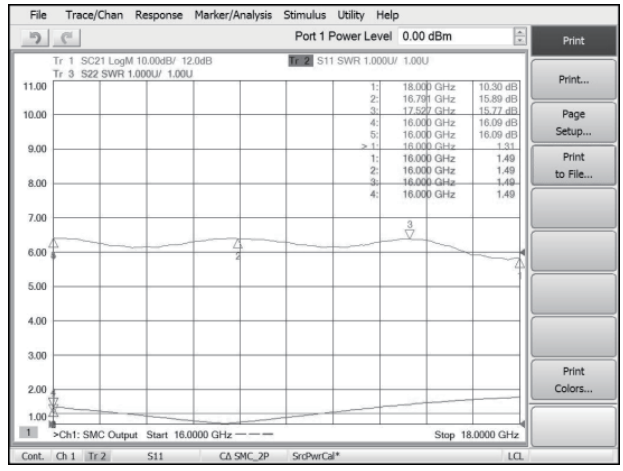


Fig. 21 Measured result of transmitter input, output VSWR (VSWRi, VSWRo) and gain S(2,1) curves

The gain shown in S(2,1) meets the requirement of more than 20 dB mentioned in the index. The standing wave at the input and output ends of the receiving channel meets the expection well.

As seen from Fig. 21, the gain S(2,1) in the range of the RF emission frequency is larger than the index requirement, 10 dB, and the gain flatness reaches the requirement with less than 2 dB after calculation.

5. Conclusions

This paper constructs and designs a new 3D vertically connected BGA structure module [30], and adopts micropackaging and integrated packaging technology to improve the integration, meeting the requirements of miniaturization design, and achieving good electromagnetic compatibility [31,32]. The link indexes such as P-1, gain, power flatness and noise all reach the expected requirements. Because the module is multifunctional, the test of each index is convenient and accurate [33]. Aiming at the core electromagnetic interference problem, the design of the special physical structure minimizes the electromagnetic interference [34], and realizes the function of the minimized transceiver of Ku-band 3D vertical interconnection with excellent performance [35].

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Biographies

LIU Boyuan was born in 1991. He received his master's degree from University of Electronic Science and Technology, China. Now he is pursuing his Ph.D. degree in National University of Defense Technology. He is now engaged in projects including Compound Electromagnetic Material and Cross-Eye Jamming. His research interests include microwave and millimeter wave circuits and system, radar guidance, electronic countermeasures and electromagnetic technology.
E-mail: 233933183@qq.com

WANG Qingping was born in 1988. He received his Ph.D. degree from National University of Defense Technology (NUDT), China, in 2015. He is currently a lecturer with the Department of Electrical Science and Engineering, NUDT, Changsha, China. His current research interests include high-resolution radar signal processing and anti-jamming technology.
E-mail: wangqingping@nudt.edu.cn

WU Weiwei was born in 1981. She received her Ph.D. degree from National University of Defense Technology (NUDT), China, in 2011. She is now an associate professor with the Department of Electronic Science and Engineering, NUDT, Changsha, China. Her research interests include electromagnetic properties of new metamaterials and their applications in antennas and radomes.
E-mail: wuweiwei@nudt.edu.cn

YUAN Naichang was born in 1965. He received his Ph.D. degree from University of Electronic Science and Technology, Chengdu, China, in 1994. From that on, he has stayed in National University of Defense Technology (NUDT) for ten years, where he became a senior research officer and group leader. He is currently a full professor with the Department of Electrical Science and Engineering, NUDT, Changsha, China. His current research interests include antenna and radome technology, electromagnetic analysis, high-resolution radar signal processing and anti-jamming technology.
E-mail: yuannaichang@nudt.edu.cn