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A Brief Review of Design and Simulation Methodology in Silicon Photonics

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Abstract: Powerful electronic design automation tools have enabled the rapid development of electronic Integrated Circuits (ICs). Similar to electronic ICs, silicon photonics technology has sufficiently matured, and large-scale photonic circuits can now be implanted into a single chip. Design tools have also evolved from primary devices to complex photonic circuits. In this paper, we review the current state of photonic design automation in terms of device modeling methods and circuit simulation methodologies, and compare the photonics design flow with mature electronic design automation design flows. Key challenges and opportunities are also discussed.

Key words: photonic design automation; compact model; circuit simulation; complex modes

1 Introduction

The evolution of CMOS technologies toward nanometer-scale devices has resulted in incredibly complex modern electronic Integrated Circuits (ICs). Chip-level design is a high-tech, high-investment, high-risk, and high-return business. Without powerful tools, designers cannot construct integrated chips bearing billions of transistors. Electronic Design Automation (EDA) is a rugged design tool that helps designers render their initial ideas on physical silicon films.

The development of EDA has undergone several stages of development[1]. In the Computer Aided Design (CAD) stage, which began in the 1960s and ended in the 1980s, computers were used to draw layouts; however, the technologies available at this time could not offer advanced features. As the number of required components increased, a strong need for physical design automation tools emerged. The Computer Aided Engineering (CAE) stage, which began in the 1980s and lasted until the 1990s, provided a number of advanced design methodologies, such as design description, synthesis, optimization, and verification. However, the design flow in this stage featured poor automation. The EDA stage, which began in the 1990s, is characterized by the availability of a large set of tools to use in all design abstraction levels. At this stage, the hardware descriptive language, system-level simulation, and synthesis techniques featured high automation and intelligence.

Some efficient methods to increase chip performance in the presence of physical limitations include improving the chip architecture, shutting down unused gates, and applying advanced packaging methods. The development trend of EDA tools is to enhance the mixed-signal processing capability of specific ICs[2–5], such as analog electronic circuits and photonic ICs. The circuit simulation accuracy relies on how EDA tools and models handle nonidealities and process variations. As the transistor size continuously decreases, modeling and simulation operations are becoming increasingly challenging.

Another development trend of chips involves the hybrid integration of electronics and photonics. Many photonics platforms, such as III–V[6–8], Si3N4[9–11], lithium niobite[12–14], and SOI, are available for communication, sensing, and other specific applications. Silicon photonics are fabricated in the same manner

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as electric ICs via CMOS technology. The CMOS technology is regarded as the most promising platform for the hybrid integration of electronics and photonics. The material index contrast between the core and cladding is quite high in these platforms, which means the resultant devices have tight structures. Thus, the high-density integration of photonic circuits composed of those materials is realizable.

The fabrication processes of silicon photonics are considered sufficient for various applications in the fields of communications and sensing. Precision fabrication processes have produced many high-performance integrated devices over the last few decades[15]. Silicon single-mode waveguides with a propagation loss of only 1–2 dB/cm may be obtained from standard fabrication processes. The coupling loss between single-mode fibers and photonic chips is 2–3 dB for grating couplers and 1–2 dB for end couplers. High-performance devices, such as power splitters[16–18], polarization splitters[19–21], microring filters[22, 23], couplers[24, 25], modulators[26–29], and detectors[30, 31], have been proposed and fabricated with CMOS or Electron Bean Lithography (EBL) technology.

Silicon photonic and electronic ICs share the same fabrication platform[32–34]. Photonic ICs require the use of electric circuit design tools for modeling and layout[35]. However, the main difference between photonic and electric ICs is that the design, simulation, and synthesis tools of electric EDA cannot be directly and efficiently used in the former. For example, the primary cell of electric integrated chips is the transistor, which is generally assigned a rectangular shape in layout tools. By contrast, photonic circuits may feature various primary components with different functions and structures. Today, silicon photonic circuits in communication applications include dozens of devices. While estimating circuit performance by manually calculating the device transfer matrix is possible, the available estimation methods may be limited for more complex circuits, such as machine learning photonics. At present CAD stage, there are no efficient synthesis tools and descriptive languages, which are essential to EDA tools, to simplify the design process.

This paper presents a review of silicon photonics design methodologies, including the design flow, device modeling, the compact model, and circuit modeling. Challenges and opportunities in PDA are also provided to highlight potential research directions for the photonic design community[36].

2 Photonic Circuit Design Flow

In electric IC designs, millions of functional logics is implanted into spaces as small as a square millimeter by using mature design flow and design tools. Similar to the development of microelectronic chips, the design of photonic ICs also follows a design flow. Because photonic ICs resemble analog electric ICs in architecture, the photonic IC design flow is designed according to the design flow of analog chips, as shown in Fig. 1[37].

The design flow contains the following four aspects:

(1) Logical design: The desired function of a photonic integrated chip is achieved by sublogical circuits and functional devices. The use of various sublogical circuits and devices provides the photonic circuit with different implementation forms. The accuracy of the simulation results depends on the accuracy of the sub-circuit and device models. Logic design and simulation could be used to verify the feasibility of the initial idea and is the primary step for further processes.

(2) Layout and physical simulation: The logical circuit is converted into a physical mask by using a series of layout steps and rules. Thereafter, a physical simulation is performed to verify the actual performance of the photonic chips. High-accuracy device and circuit modeling methods are employed to represent the complexity of optical signal propagation in the circuit.

(3) Design rule check and functional verification: The physical mask consists of several polygons on different layers. These polygons include circles, triangles, and arbitrary shapes, and are much more complicated than electric ICs; thus, the design rule check is a challenging process. Typically, the design rules are provided by Fabs to ensure that the mask is

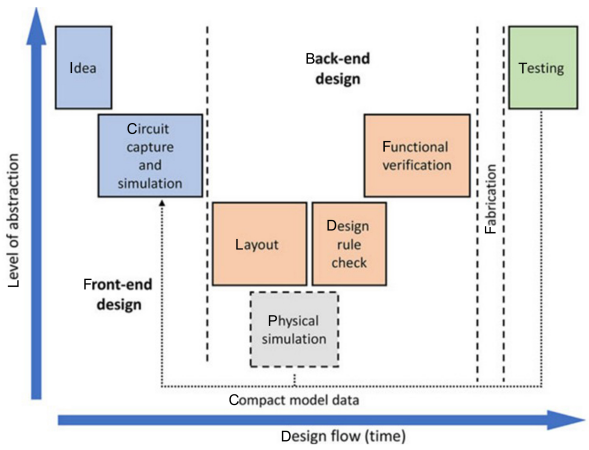

Fig. 1 Photonic IC design flow.

compatible with the fabrication process. After Design Rule Check (DRC), functional verification or Layout-Versus-Schematic (LVS) evaluation is conducted. In this step, the consistency between the layout and the intended logic circuit is checked.

(4) Fabrication and testing: The taper-out mask is delivered to the Fabs. After several processing steps, the photonic chip is fabricated. The fabricated chip is then tested to ensure that its function is consistent with the design intent. The parameter extraction method is an essential means to evaluate the performance of fundamental devices within a chip. The testing and extracted parameters are then used to redesign or improve the circuits.

Identifying and separating these abstraction steps in the design is essential to the scaling of circuits. The circuit design is based on the logical individual sub-circuit and device rather than the physical architecture devices. The sub-circuit and device models are well designed, tested, and supplied by Fabs in a Process Design Kit (PDK) or other libraries. The PDK, which contains information on the fabrication process and compact model of devices, is the interface between the Fab and the designer.

The complexity of photonic signals prevents the development of an effective modeling method for building compact models of photonic integrated devices. A logical circuit can be simulated by improving traditional optical fiber communication methods. However, dispersion, polarization, coupling, and other optical signal propagation characteristics in ICs impede the construction of accurate physical simulation methods for these circuits.

Compact model extraction and circuit physical modeling methods are discussed in the next sections; these two aspects are currently the most difficult challenges in the PDA industry.

3 Device Simulation and Compact Model

The smallest unit of an electric integrated chip is the transistor. The compact model of a microelectronic device is relatively simple. However, numerous types of devices may be found in optoelectronic integrated chips. Optical signals have more state attributes than electrical signals, such as polarization or radiation, and extracting integrated optical devices into simple models is quite challenging[38]. The most common means to simulate components is the finite difference time-domain algorithm, the results of which can be used to extract the guided-mode characteristics of ports. Because the radiation fields at ports cannot be fully expressed using guided modes, more accurate and efficient modeling methods are strongly needed.

This section reviews the current modeling methods for typical passive and active optical devices, and then discusses the most promising modeling method for these devices.

3.1 Waveguides

Strip and ridge waveguides are the most commonly used optical waveguides in integrated chips. The waveguide features can be analyzed by mode theory. Mode propagation and bending losses caused by the discontinuity of the waveguide surface are the two most important parameters characterizing the performance of optical waveguides. Imperfections in the processing technology result in surfaces that are rougher than expected. Thus, the propagation loss and phase could deviate from the design values. Some works have been proposed to model the transmission error caused by the fabrication process[39, 40]. However, these device modelling methods are based on the guided-mode theory and do not consider the radiation field. No complete compact model of integrated optical waveguides is currently available, and more accurate models must be developed to address this issue.

3.2 Splitters

Silicon-based integrated devices include a number of optical splitters, such as Y branch optical splitters, MultiMode Interference (MMI) power splitters, Directional Coupler (DC) power splitters, and other polarization beam splitters. Because of imperfections in the fabrication processes of these components, however, Y branch optical splitters are rarely used in silicon photonic integrated chips. MMI and DC splitters are commonly used in coupler structures. Multimode interference and coupled-mode theories are used to analyze MMIs and DCs[18, 41, 42]. However, these analytical methods do not consider the radiation field of the devices; as such, these methods cannot accurately calculate device performance and require the use of other numerical methods, such as the finite difference time-domain algorithm.

3.3 Filters

The most commonly used filters are based on micro-ring and grating structures, as shown in Fig. 2. Similar to those of splitters, the analytical device models of these

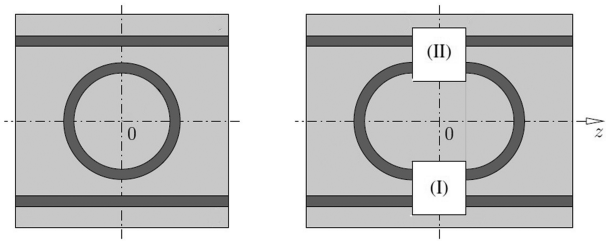

Fig. 2 Microring resonator compact model.

devices are based on analytical theory, such as coupled-mode theory and phase-matching conditions[43, 44]. However, only the guided mode is considered in these models. The simulation results in some cases are relatively more accurate compared with those obtained from numerical algorithms, such as Finite-Difference Time-Domain (FDTD).

3.4 Couplers

Grating and edge couplers are two commonly used devices that couple optical signals in and out of photonic ICs. Because edge couplers are fairly large in size (i.e., lengths of a hundred micrometers), the calculation ability of computing workstations is low; the most efficient modeling method for edge couplers is the eigenmode expansion method, which is also known as the mode-matching method[45]. The calculated result is typically different from the FDTD result. Grating couplers can be modeled by the mode-matching method with the help of complex modes[46–49]. An accurate compact model of the grating coupler has been proposed and compared with FDTD[49], as shown in Fig. 3.

3.5 Modulators

The structure of modulators is much more complicated than that of the passive devices described above. Performance analysis of the modulator includes two aspects: optical analysis and electrical analysis. The

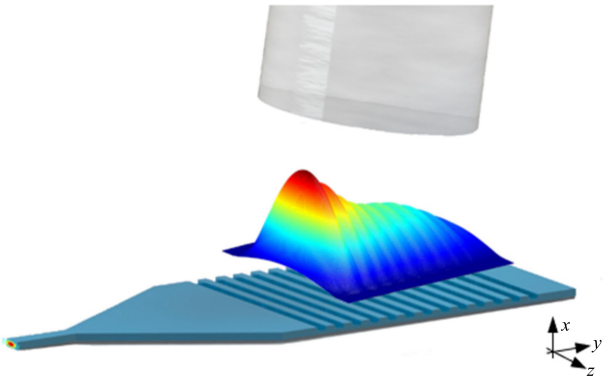

Fig. 3 Grating coupler compact model.

modeling of the thermal-optical modulator[50] is relatively simpler than that of PN junction modulators, because the electrical component can be regarded as a resister. The compact model of this type of modulator is identical to that of passive devices of the Mach-Zehnder interferometer or microring resonator. The modeling of the PN junction modulator is more complicated than that of thermal-optical modulators, because the electrical component cannot simply be regarded as a resistor. The capacitance and equivalent resistance of the PN junction and the parasitic capacitance, resistance, and inductance of the optical modulator electrode should be comprehensively analyzed. Several modulator models were proposed in the Verilog-A and SPICE forms to study photonic integrated circuits with mature EDA tools[28, 51, 52].

3.6 Detectors

Silicon materials are transparent in the communication band, and silicon-based detectors are usually realized by the epitaxial growth of germanium on silicon waveguides. Simulation of the germanium detector involves passive and active phases. The passive phase of the simulation is realized by the finite difference time-domain method, while the active phase is simulated in the same manner as PN junction modulators[53, 54].

No accurate compact mode of integrated devices has been proposed because of the lack of approaches with which to deal with radiation fields. At present, the finite difference time-domain method in combination with the waveguide port modeling method is the most effective way to extract devices performance. However, because of the missing radiation mode, this model cannot fully represent the features of the device. Complex-mode analytical theory is a promising method in device modeling that can calculate radiation fields accurately. It can use complex-mode ports instead of guided-mode ports, and apply complex-mode-matching methods and complex coupled-mode theory to model devices. The modeling of active devices can be learned from the modeling methods of microelectronic devices. The parameter extraction method is relatively mature. However, because the phase change observed as a function of voltage is nonlinear, some approximation methods are necessary.

4 Circuit Simulation

Given their relatively small size, photonic integrated devices may be modeled using a number of precise

numerical simulation methods, such as the finite difference time-domain method. However, photonic ICs usually consist of dozens, maybe even thousands, of devices; in this case, the numerical simulation methods used in device simulation may no longer be applicable[38]. Accurate circuit simulation methods can improve the estimation of system performance and increase circuit complexity.

Traditional optical communication system simulation software, makes use of optical IC simulation algorithms that can be classified as frequency-domain algorithms and time-domain simulation algorithms. If the characteristics of the device do not change over time, such as those of most passive devices, the features of this device may be conveniently expressed using frequency-domain characteristics. The scattering matrix method is the most effective means to describe device characteristics in the frequency domain.

However, the guided-mode feature scattering matrix cannot completely express device characteristics, because the radiation field at the ports is not included in the matrix. The most accurate modeling method in this case involves the use of complex modes, instead of guided mode for device modeling and simulation. A complex matrix can be obtained from the expanded field at the port with complex modes or the direct modeling of the devices using complex-mode analytical methods, such as the complex-mode-matching method and complex coupled-mode theory. For example, Huang et al.[55] proposed a complex-mode analytical method to model and simulate a circuit consisting of passive devices, as shown in Fig. 4. This technique could divide a complicated device structure, such as a microdisk resonator, into subcomponents for efficient simulation.

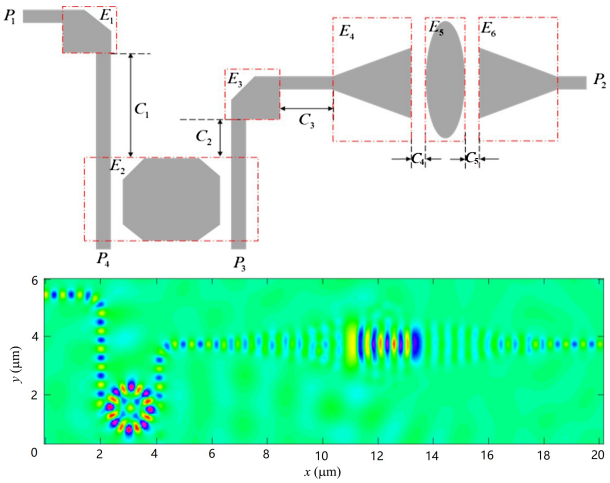

Fig. 4 Complex-mode circuit simulation model. *E* is the basic element, *P* is the port, and *C* indicates coupling.

Time-domain circuit simulation enables the analysis of a circuit's response to time-varying stimuli by passing signals between circuit blocks and calculating the response of each block at each time step. Unlike the frequency-domain algorithm, which only analyzes the characteristics of a single wavelength, the time-domain simulation algorithm can simultaneously calculate multiple wavelengths and modes. Passive components can also be considered filters and conveniently applied to time-domain simulations by using Fourier transform.

After frequency- and time-domain simulation, the robustness of the circuit must be estimated. The most commonly used methods for checking robustness in electric ICs are the Monte-Carlo and corner analytical methods[37, 56, 57]. However, finding the best and worst results, which is essential for corner analysis, is fairly challenging. Thus, the Monte-Carlo analytical method, which requires a large number of circuit simulations with various basic element models, is more suitable for photonic ICs. For example, the impact of propagation phase variation can be described by Monte-Carlo simulations. Because of imperfections in the processing technology, phase changes are usually difficult to estimate in a simulation.

The optical circuit simulation method is similar to the classical fiber communication simulation method. Follow-up work should be conducted to improve the algorithm according to the properties of silicon-based integrated devices.

5 Challenge and Opportunity

Current photonic circuits are relatively simple, and designing systems by using paperwork has not shown real disadvantages. As the number of devices increases, using powerful design tools to achieve complex circuit designs becomes increasingly imperative. As discussed in the previous two sections, the main challenge in circuit design is the building of an efficient and accurate compact model of devices with a mature descriptive language, and the challenge in circuit simulation is the improvement of primary simulation methods with integrated optical devices.

Optimization of the design flow also presents a number of challenges. To date, no mature design flow for the design of photonic chips is yet available. The present paper only describes the front-end design flow; work on end-front design flows remains immature. The descriptive language and synthesis method, which could

convert functional descriptions into a logical circuit, remain lacking. The radiation field of a device could interfere with other devices, and no efficient method to address this problem has yet been developed. In contrast to electric ICs, the circuit layout is composed of polygons. The design rule check method for electric ICs should be improved for photonic structures. Moreover, efficient tools with which to verify a potential layout against the intent-designed function are unavailable. Finally, the parameter extraction method used to characterize the performance of the functional element in the circuits after chip testing remains flawed.

These challenges reveal ample opportunities in the research and industrial applications of PDA. More collaboration among stakeholders is necessary to promote the development of the optoelectronic industry and superior design tools.

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