TSINGHUA SCIENCE AND TECHNOLOGY
ISSN 1007-0214 05/16 pp495–511
DOI: 10.26599/TST.2021.9010035
Volume 27, Number 3, June 2022

Review of Technologies for High-Voltage Integrated Circuits

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Abstract: High-Voltage power Integrated Circuits (HVICs) are widely used to realize high-efficiency power conversions (e.g., AC/DC conversion), gate drivers for power devices and LED lighting, and so on. The Bipolar-CMOS-DMOS (BCD) process is proposed to fabricate devices with bipolar, CMOS, and DMOS modes, and thereby realize the single-chip integration of HVICs. The basic integrated technologies of HVICs include High-Voltage (HV) integrated device technology, HV interconnection technology, and isolation technology. The HV integrated device is the core of HVICs. The basic requirements of the HV integrated device are high breakdown voltage, low specific on-resistance, and process compatibility with low-voltage circuits. The REduced SURFace field (RESURF) technology and junction termination technology are developed to optimize the surface field of integration power devices and breakdown voltage. Furthermore, the ENhanced DIelectric layer Field (ENDIF) and REduced BULk Field (REBULF) technologies are proposed to optimize bulk fields. The double/triple RESURF technologies are further developed, and the superjunction concept is introduced to integrated power devices and to reduce the specific on-resistance. This work presents a comprehensive review of these technologies, including the innovation technologies of the authors' group, such as ENDIF and REBULF, substrate termination technology prospective integrated technologies and HVICs in wide band gap semiconductor materials are also discussed.

Key words: High-Voltage ICs (HVICs); high-voltage integrated technology; Bipolar-CMOS-DMOS (BCD) process; integrated power semiconductor devices; superjunction

1 Introduction

Electric energy is expected to remain one of the most widely used energy sources of mankind. More than 75% of electric energy needs to be converted by power devices before its application to electric equipment. The principle of increased integration is also suitable for power semiconductors. Therefore, High-Voltage power Integrated Circuits (HVICs) are widely used in power systems to realize high-efficiency power conversions. The development of HVICs is based on the innovations of HV integration technologies to realize high breakdown voltage V_B, low cost, and High Voltage (HV) and Low Voltage (LV) integration. The current work reviews the important HV integrated technologies and their developments.

1.1 Fundamental structures of power devices

The fundamental structures of power devices are shown in Fig. 1. A power device can be simply treated as a series connection of a Voltage Sustaining Layer (VSL) and a corresponding low-voltage device. VSLs come in three typical forms. The first one comprises resistance-type VSLs with single doping, such as those in VDMOS. This VSL type is restricted by the well-known $R_{\text{on,sp}} \propto V_B^{2.5}$ relationship[1]. The second one comprises the conductivity enhancement-type VSLs, such as those in IGBTs[2]. The forward injection of the PN junction is introduced to the VSL to realize conductivity

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Manuscript received: 2021-02-28; accepted: 2021-04-08

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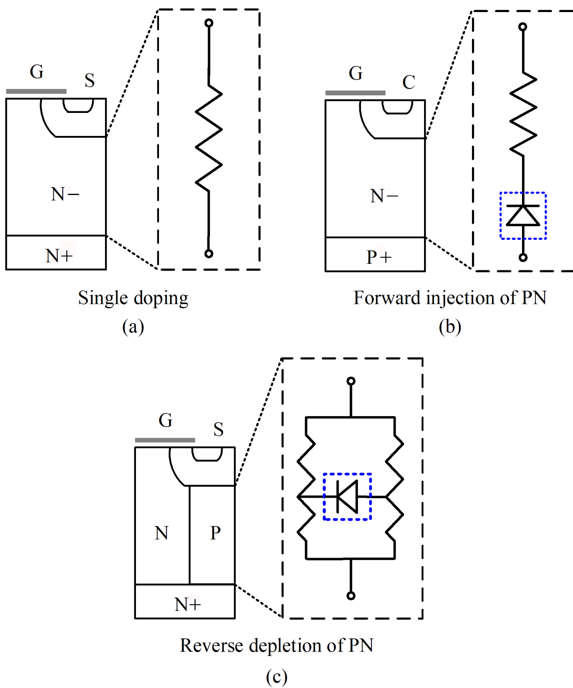


Fig. 1 Power devices with (a) resistance-type, (b) conductivity enhancement-type, and (c) junction-type voltage sustaining layers.

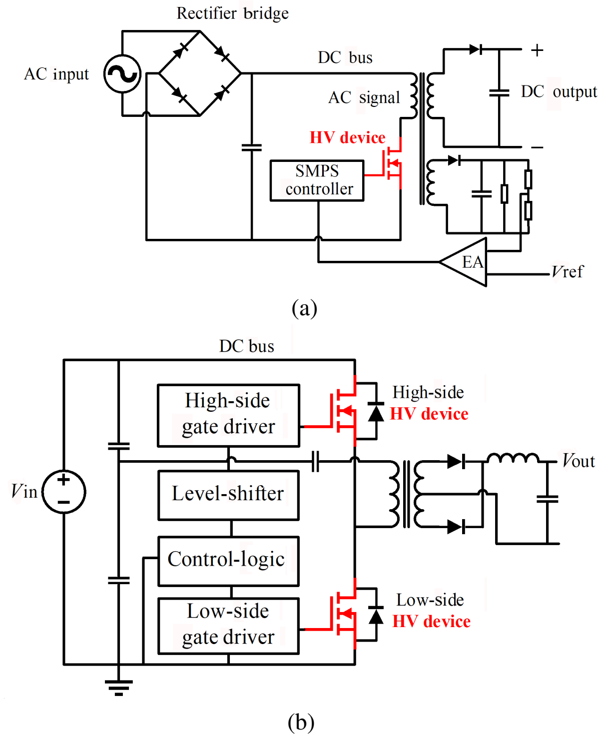


Fig. 2 Simplified circuit schematic of (a) AC/DC converter[8] and (b) half-bridge converter[9].

enhancement. The injected nonequilibrium carriers in the on-state also cause a current tail in the off-state. The third form comprises the junction-type VSLs, such as those in SuperJunction (SJ)[3–5]. In junction-type VSLs, the reverse depletion of the PN junction is introduced into the VSL to increase the doping dose. The SJ concept breaks the conventional relationship of $R_{\mathrm{on,sp}} \propto V_B^{2.5}$, and shows $R_{\mathrm{on,sp}} \propto V_B^{1.32}$[6], which is further developed into the quasilinear $R_{\mathrm{on,sp}} \propto V_B^{1.03}$relationship[7]. These VSLs are widely studied in the context of HV integrated devices.

1.2 HVICs and BCD process

HVICs are widely used in electric systems, such as Alternating Current to Direct Current (AC/DC) converters, HV gate drivers, Light-Emitting Diode (LED) drivers, and inverters for motor control. Figure 2 shows the typical schematics of an AC/DC converter and a half-bridge converter[8, 9]. Obviously, most of the electric energy must be transmitted by the HV integrated device. The AC/DC converter requires a low-side HV integrated device as an HV switch, whereas the half-bridge converter requires high-side and low-side HV integrated devices. As the root mean square of the AC input worldwide is approximately 90–265 V[8], the V_B value of HV integrated devices is usually in the range of 500–900 V when considering surge voltage and inductance in circuits.

Single-chip integration is an important development direction of HVICs. Integrated HV devices are usually voltage-controlled lateral devices, such as LDMOS or LIGBT, because of their superior performance and easy-to-drive feature. The main challenge is fabricating devices that function under different applied voltage levels and modes. The Bipolar-CMOS-DMOS (BCD) processes (Fig. 3) are proposed to solve this problem[10, 11]. Figure 3a shows a silicon-based BCD process platform, which integrates 40–700 V HV LDMOS devices, LV CMOS devices, and bipolar transistors[12–15]. All these devices can be fabricated under the same process. The SOI-based BCD process with full dielectric isolation technology (Fig. 3b) further reduces the modulations and crosstalk among all types of devices[16]. The superior isolation performance of the SOI-based BCD process also makes it a proper platform to integrate high-performance LIGBTs[17, 18]. Figure 4 shows a micrograph of an AC/DC converter fabricated by BCD technology. Most of the chip area is determined by the HV integrated device. Therefore, HV integrated devices are the core of HVICs, the basic requirements of which are high V_B, low $R_{\mathrm{on,sp}}$, and process compatibility.

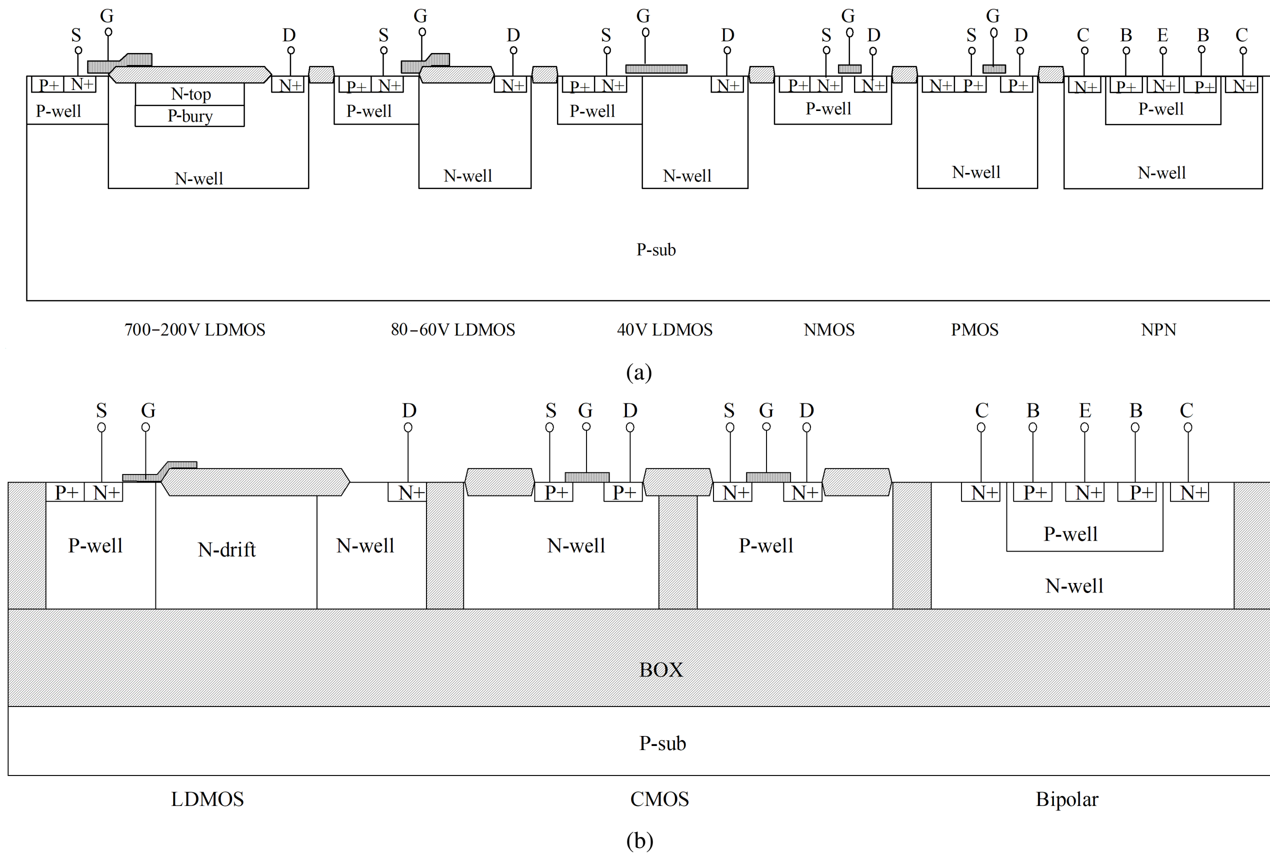


Fig. 3 Schematic cross-section of (a) BCD process on silicon and (b) BCD process on SOI.

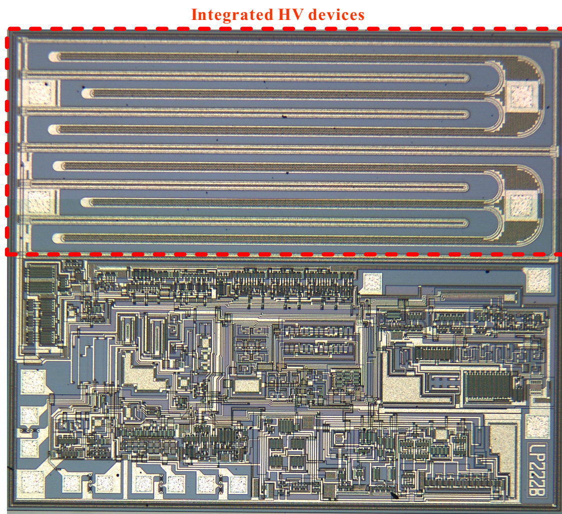


Fig. 4 Micrograph of AC/DC converter fabricated by BCD technology.

1.3 Summarization of HV integrated technologies

The development of HV integrated technologies is the cornerstone of the BCD process. This work reviews some of the most important HV integrated technologies. Section 2 provides the basic integration technologies, including the REduced SURFace field (RESURF) technology, Junction Termination Technology (JTT), and High-Voltage Interconnection (HVI) technology. Section 3 reviews the ENhanced DIelectric layer Field (ENDIF) technology for integrated HV SOI devices and the REduced BULk Field (REBULF) technology for integrated HV silicon-based devices. Section 4 discusses HV integrated SJ devices. Section 5 explains the prospects of new integrated technologies and HVICs in wide band gap semiconductor materials.

2 Basic Integrated Technologies

As shown in Fig. 4, HV integrated devices have an interdigitated structure to realize high current ability. Therefore, basic integration technologies focus on high breakdown voltages at the drift and termination regions. Moreover, circuit topologies cause the HVI between HV and LV devices, and thereby cause a reduction in V_B. This part introduces several integrated technologies to solve these problems.

2.1 RESURF technology

HV integrated devices are usually fabricated at the surface of a wafer, hence their long and thin drift regions. As the impact ionization rate in semiconductors strongly depends on the electric field, premature breakdown may occur at the peak field point at the surface. The schematic views of LDMOS devices using RESURF technology[19] are shown in Fig. 5. For the single RESURF LDMOS, shown in Fig. 5a, the possible peak field occurs near the drain or the source with the variation of drift doping concentration. The maximum V_B is realized when the peak fields near the source and the drain are equal. Such equality indicates an optimized vertical doping dose D_{op} of almost 10^{12} cm^{-2}.

In further reducing $R_{\text{on,sp}}$, the additional reverse depletion of the PN junction discussed in Section 1.1 is introduced into the single N-type doped drift region to form double and triple RESURF structures, as shown in Figs. 5b and 5c[20, 21, 24, 25]. As the number of depletion junctions increases from 1 to $2-3$, the D_{op} values of the double and triple RESURF devices also increase to about $2 \times 10^{12} - 3 \times 10^{12}$ cm^{-2}, respectively[21].

The D_{op} value of the RESURF technology appears proportional to the number of depletion junctions. This conclusion includes an implicit assumption that all vertical PN junctions have vertical peak electric fields with the same value. In fact, the optimized doping dose can be significantly increased by reducing the depletion length of the local PN junction. Figure 5d shows a RESURF LDMOS with surface local charge-balanced N-top and P-bury layers[22, 23], whose D_{op} increases to 5×10^{12} cm^{-2}[26]. Furthermore, a sandwich N-P-N structure is proposed for a high D_{op}[27].

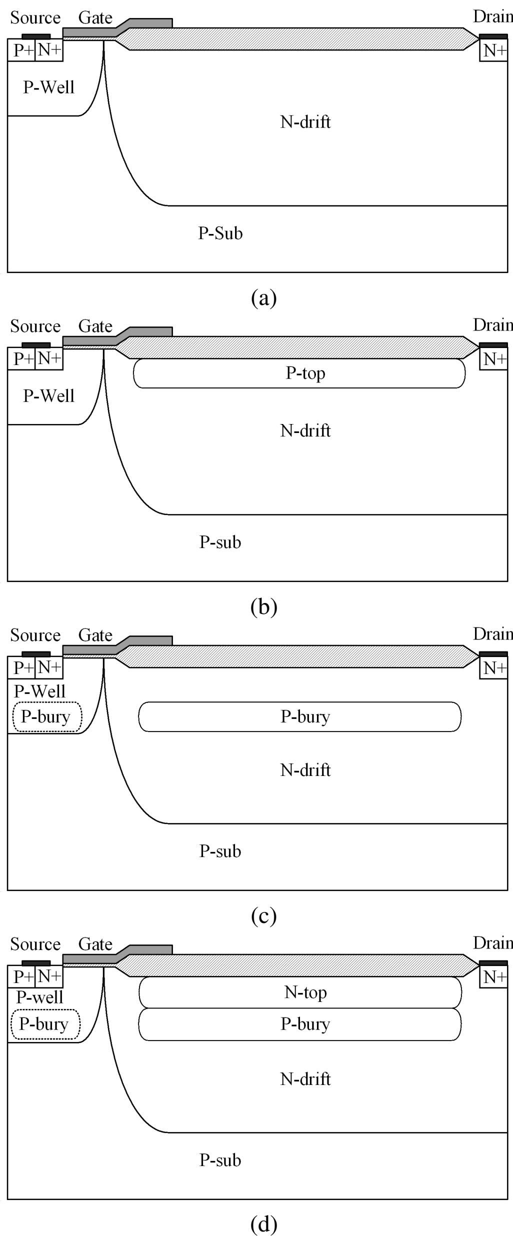


Fig. 5 Schematic views of (a) single RESURF LDMOS[19], (b) double RESURF LDMOS[20], (c) triple RESURF LDMOS[21], and (d) local charge-balanced RESURF LDMOS[22, 23].

2.2 Junction termination technology

The breakdown points of an HV integrated device with an interdigitated structure always occur at the fingertip region. As a result of the curvature effect, the peak electric field is located at the PN junction with a small curvature radius[28, 29]. In realizing a high V_B, the termination region should be designed very carefully. The cylindric PN junction can be used for the qualitative analysis of the curvature effect (Fig. 6). r_j, r_d, and W_d are the curvature radii of the PN junction, depletion edge, and width of the depletion region, respectively. The maximum electric field $E_{\max}$ is expressed as

$$E_{\max} = \frac{qNW_d}{\varepsilon_s}\left(1 + \frac{W_d}{2r_j}\right) \tag{1}$$

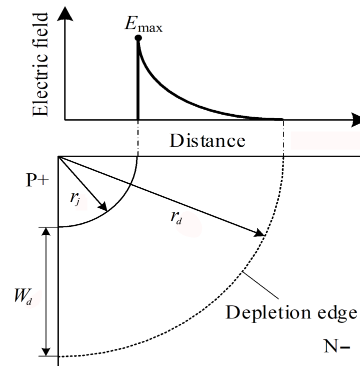


Fig. 6 Electric field distribution of curvature junction. The maximum field $E_{\max}$ is increased by the curvature effect.

where q, N, and ε_s are the electron charge, doping concentration of the N-region, and dielectric constant of the silicon, respectively.

The curvature effect obviously causes an increased $E_{\max}$ with the reduction of r_j. All JTTs focus on the reduction of $E_{\max}$. Equation (1) comprises three main variables r_j, N, and W_d. Accordingly, the mechanisms of the three types of JTT can be deduced as follows: (1) JTT with increased r_j, (2) JTT with reduced N, and (3) JTT with reduced W_d.

2.2.1 JTT with increased r_j

The first method for alleviating the curvature effect is to increase the curvature radius. Figure 7 shows two structures with increased r_j[30, 31]. The curvature radius of the fingertip region is increased to reduce $E_{\max}$ at the curvature junction. Equation (1) indicates that the low $E_{\max}$ can only be realized by adopting a large r_j. Therefore, this type of JTT results in a large chip area.

2.2.2 JTT with reduced N

The second method for alleviating the curvature effect is to reduce N. This approach can be realized by introducing opposite-type doping into the termination region or reducing a part of drift doping. Figure 8 shows

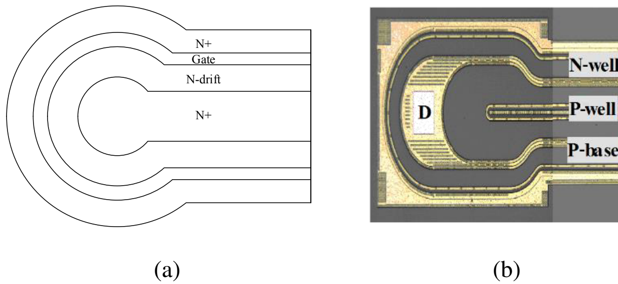


Fig. 7 JTT with increased curvature radii[28–31].

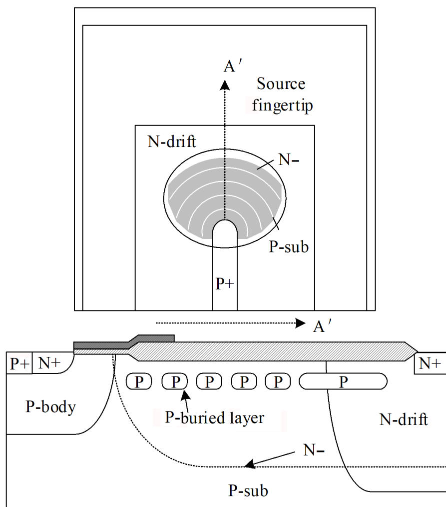


Fig. 8 JTT with P-islands and N-compensations[32].

a JTT with P-islands and N-compensations[32]. $E_{\max}$ is reduced by the opposite-type doping compensation. An additional doping process is needed in this structure.

Figure 9a shows a structure that uses Substrate Termination Technology (STT)[33, 34]. A part of the P-type substrate is introduced at the surface of the fingertip region by removing a part of the N-drift region. The STT structure can realize an HV device with drain and source fingertip radii below 10 μm without additional compensation doping. Figures 9b and 9c show that the STT is a universal technology that can be used for the integrated RESURF[35], SJ[33], N-top devices[36, 37], etc.

2.2.3 JTT with reduced W_d

The third type of JTT is reducing the depletion width W_d. In the first two methods, W_d is determined by V_B. The high V_B results in a large W_d. Thus, reducing

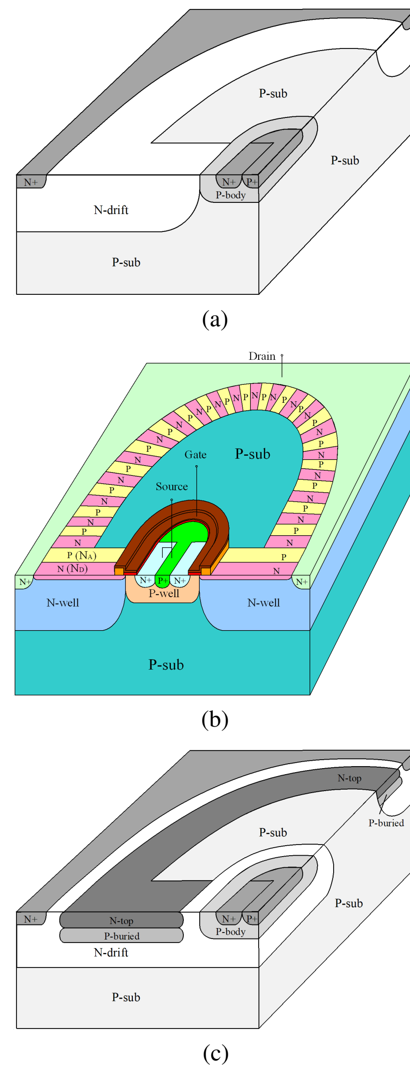


Fig. 9 Substrate termination technology: (a) basic structure, (b) SJ LDMOS with STT[33], and (c) *N*-top LDMOS with STT[34, 35].

$E_{\max}$ by reducing W_d and maintaining a high V_B is difficult. Figure 10 shows the schematic of the Dielectric Termination Technology (DTT)[38]. The fingertip region in Fig. 10a is surrounded by n trench dielectric rings. The potential difference ΔV between the adjacent rings is reduced from V_B to $\Delta V \approx V_B/n$. Therefore, the depletion width W_d of the curvature PN junction is reduced significantly. The voltage sustaining distance along AA′ can be further reduced to a full dielectric termination structure to realize a small termination length (Fig. 10b). The LDMOS using DTT realizes a V_B of 600 V with a small termination length of 25 μm.

2.3 HVI technology

HVI is necessary for HVICs because of its circuit topologies. Take nLDMOS as an example. The HVI needs to be extended across the entire drift region because the integrated HV device always has a closed structure with HV at the inner drain. The HVI line may cause a significant reduction in V_B because of the strong field modulation effect[39, 40], which may also induce hot carrier injection in power devices[41]. The physical essence of HVI may be equivalent to the introduction of positive charges Q_E on the surface of a device and $Q_E = C_E \Delta V_I$, where C_E is the equivalent capacitance under the HVI line and ΔV_I is the potential difference between the upper and lower interfaces of the insulator. Hence, two main mechanisms of HVI technology have been reported: (1) reducing Q_E by reducing C_E or ΔV_I; and (2) introducing opposite-type charges to keep a new charge balance with Q_E.

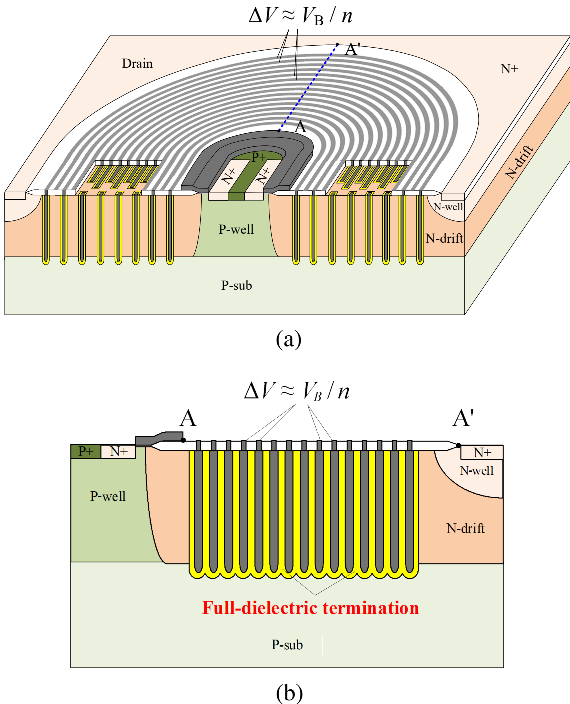


Fig. 10 Schematic cross-sectional view of (a) proposed DTT structure and (b) 2D cross-sectional view of full-dielectric termination structure along AA′[38].

2.3.1 HVI technology with thick insulator

The simplest way to avoid the impact of HVI is to increase the thickness of the insulator under the HVI line. As a result of the low C_E from the thick insulator, Q_E is reduced to alleviate the impact of HVI. A possible approach to realizing a thick insulator is shown in Fig. 11[42], in which the step height from the thick insulator at the surface of the device is reduced by the wet etching of silicon before field oxidation.

In a real process, the thickness of an insulator film is usually limited to less than 5 μm. Applying this structure solely to HV devices with an interconnect voltage of over 600 V is unrealistic. On the basis of the same mechanism, a bonding wire is used as the HVI line[43]. As the bonding wire is separated from the silicon by a passivation layer and a thick air region, this HVI structure could efficiently avoid the impact of HVI without the limitation of a thick insulator. However, the wire bonding outside the device requires an extra chip area.

2.3.2 HVI technology with the self-shielding capability

Another way to reduce Q_E is to reduce ΔV_I. Figure 12a shows the HVI technology with self-shielding capability[44, 45]. The inevitable crossing of HVI is eliminated by changing the topology of the HVJT region. In the self-shielding HVI structure, the high ΔV_I is removed from the circuit, and the low Q_E reduces the impact of HVI. Figures 12b and 12c show that the HV nLDMOS and pLDMOS use the self-shielding HVI technology. The double RESURF mechanism is

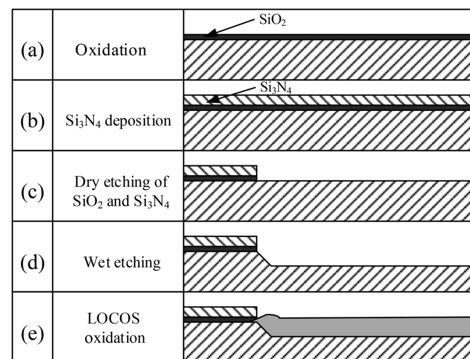
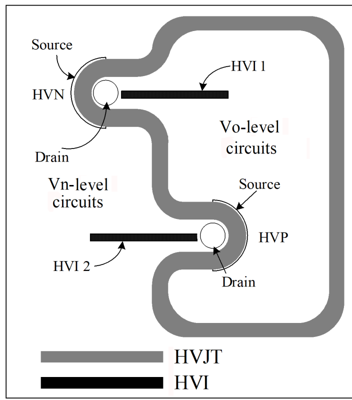
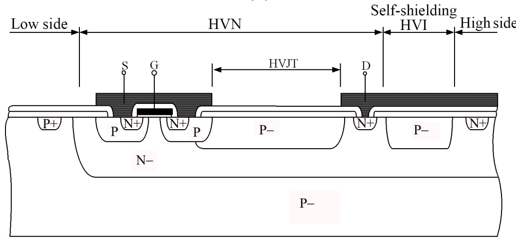


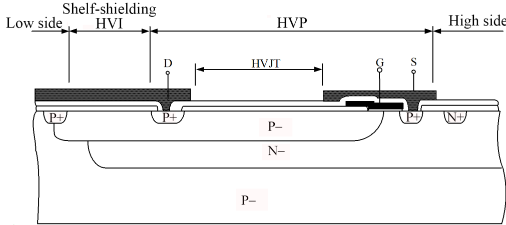
Fig. 11 Processing of thick insulator[42].



(a)



(b)



(c)

Fig. 12 Integrated nLDMOS and pLDMOS with self-shielding HVIs: (a) top view[44, 45], (b) cross section of nLDMOS[46, 47], and (c) cross section of pLDMOS[46].

observed in both devices. As ΔV_I in the self-shielding HVI structure is independent of V_B, 1200 V gate drivers can be realized. The divided RESURF technology is further developed to reduce the crosstalk between two-level shifters[46, 47].

2.3.3 HVI technology with new charge balance

The HVI technology breaks the perfect charge balance developed by the RESURF technology. Opposite-type charges are introduced to maintain the new charge balance with Q_E. Figures 13 and 14 present two typical HVI structures designed with this mechanism. In the HVI structure in Fig. 13, an additional JT extension P-region is introduced at the surface of the device[40, 48]. The ionized acceptors from the P-region keep a new charge balance with Q_E. As shown in Fig. 14, the new charge balance is introduced by the single-layer or double-layer floating field plate[49]. As the charge

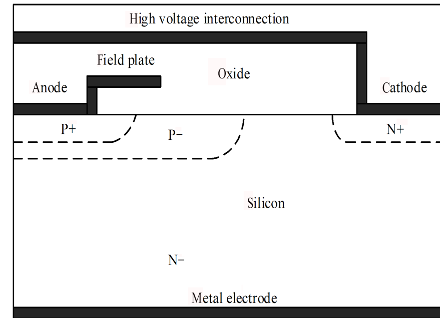


Fig. 13 Junction termination extension structure in HVI structure. Ionized negative charges from the surface's P-region are introduced to keep a new charge balance with Q_E[49].

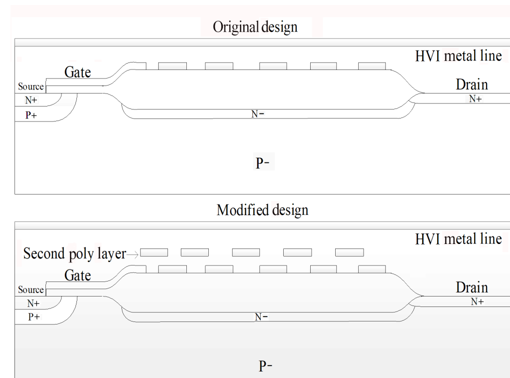


Fig. 14 Cross section of LDMOS using HVI structures with single- and double- layer floating field plate[49].

balance is developed mainly in the insulator layer and is almost independent of the depletion in the drift region, the HVI structure in Fig. 14 can realize a better characteristic than that in Fig. 13.

3 Bulk Field Optimization Technology

The surface electric field of an integrated HV device is optimized by RESURF and JTT. If the premature breakdown at the surface is eliminated, then the vertical breakdown in the bulk becomes the main limitation of the device in achieving high V_B.

Bulk field optimization technologies are proposed to increase the vertical V_B of HV integrated devices, including the ENDIF and REBULF for SOI- and silicon-based devices, respectively.

3.1 ENDIF

The schematic diagram of the ENDIF rule is shown in Fig. 15[50, 51]. The structure of an HV SOI device is shown in Fig. 15a. The vertical V_B is given by $V_B = 0.5t_s E_C + E_I t_I$, where t_s and t_I are the thicknesses of the silicon and insulator layers, respectively. E_C and E_I

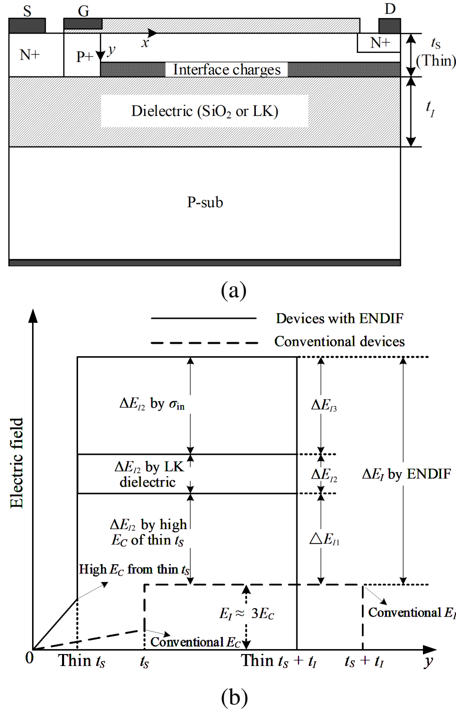


Fig. 15 Schematic diagram of ENDIF rule: (a) typical structure of SOI device and (b) three approaches to increase EI based on ENDIF[50].

are the critical electric field of silicon and the electric field of the insulator layer, respectively. In a conventional HV SOI device, E_I is only about 100 V/μm, which is much lower than the critical electric field (i.e., 600–1000 V/μm). The concept of ENDIF is to improve the vertical V_B of the SOI device by enhancing E_I. Given the continuity of electric displacement, including the interface charge σ_{in}, E_I is expressed as Ref. [50],

$$E_I = \frac{q}{\varepsilon_I}\sigma_{\text{in}} + \frac{\varepsilon_s E_C}{\varepsilon_I} \quad (2)$$

where ε_I is the dielectric constant of the insulator.

The qualitative enhancement effects of E_I are illustrated in Fig. 15b. According to Eq. (2), ENDIF gives three approaches to increase E_I: (1) ΔE_{I1} by using a thin silicon layer with a high E_C[52–56]; (2) ΔE_{I2} by introducing a low-k (low permittivity) dielectric buried layer[57, 58]; and (3) ΔE_{I3} by implementing interface charges[59–61].

σ_{in} and ε_I are determined by the device structure and material of the insulator. E_c of the silicon is determined by the integral of the impact ionization rate α with $\int_0^{t_s} \alpha \mathrm{d}s = 1$[62]. It can be expressed as a function of t_s,

$$E_{\text{C}} = 4.7\exp\left[\frac{19.64}{\ln(3227.4 t_s)}\right] \quad (3)$$

where t_s is in micron.

The maximum deviation of Eq. (3) is smaller than 2% in the range $0.05\,\mu\text{m} \leqslant t_s \leqslant 100\,\mu\text{m}$. In Eq. (3), t_s of the SOI under a given E_C can be directly calculated by $t_s = 1/3227.4\exp[19.64/\ln(E_C/4.7)]$, which is also a simple design guide of the thickness of an HV SOI device. Figure 16 shows E_C of the silicon as a function of t_s. E_c varies very slowly in the thick silicon structure with $1\,\mu\text{m} \leqslant t_s \leqslant 100\,\mu\text{m}$, which can be treated as a constant. E_C is increased dramatically in the submicron scale, e.g., E_C is up to over 100 V/μm at $t_s < 0.19\,\mu\text{m}$. Analytical E_c from Eq. (3) is in good agreement with simulations and experiments.

Typical HV SOI devices based on the three approaches of the ENDIF rule are illustrated in Fig. 17. Figure 17a shows a thin-layer SOI device[53]. The E_C value of the silicon is increased according to Eq. (3) to realize high E_I. Figure 17b shows an SOI device with an LK insulator under the drain[57]. E_I is increased by reducing ε_I of the insulator. In Figs. 17c and 17d, interface ionized charges[59] or holes[60] are introduced at the interfaces of the silicon and insulator to enhance E_I. Other reported devices can also be included in these three approaches.

3.2 REBULF

For a bulk silicon-based HV device, the vertical V_B is restricted by the planar junction breakdown at the interface of the N-drift and P-substrate. The RESURF technology can realize an optimized surface electric field. The vertical V_B is the main limiting factor to further

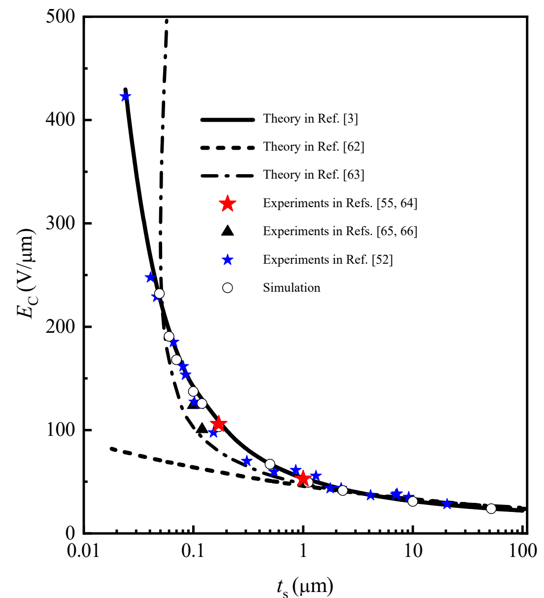


Fig. 16 Critical electric field E_C of silicon as a function of t_s. E_C is increased dramatically in the thin silicon layer (t_s < 1 μm).

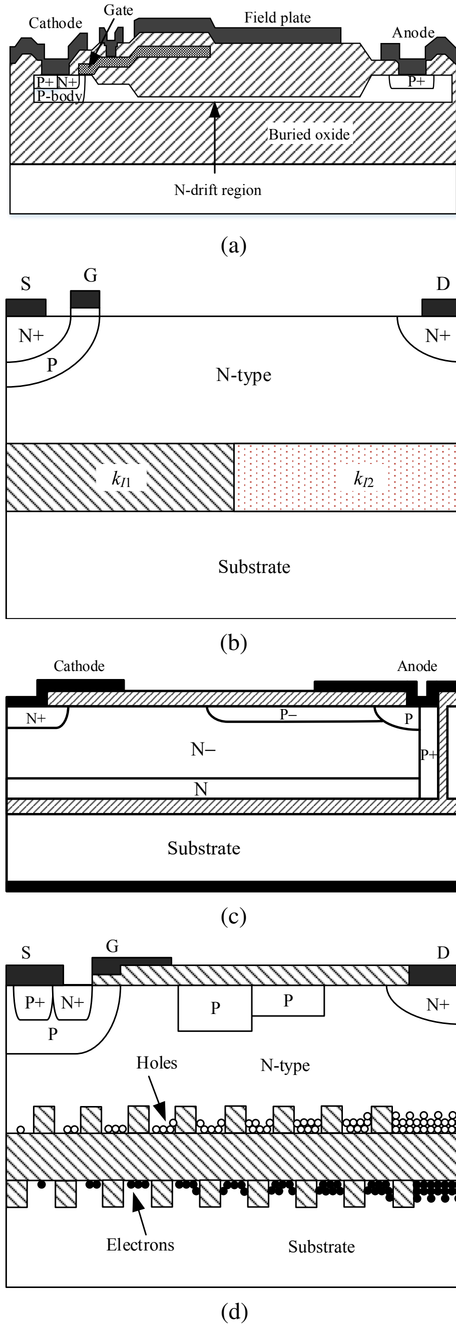


Fig. 17 Typical HV SOI devices based on ENDIF rule with (a) thin silicon layer and high E_c[53]; (b) LK dielectric buried layer[57]; (c) Reference [59] interface charges, and (d) Reference [60] interface charges.

improve the voltage handling capability, especially for a high V_B of over 1000 V.

The basic structure of REBULF involves the introduction of an N-type floating layer in the P-substrate. Thus, the vertical V_B in the new structure is sustained by multiple PN junctions. The electric field at the main junction between the N-drift and the P-substrate is thus reduced to improve the vertical V_B.

Figure 18 shows typical REBULF devices. An N+ floating layer is introduced into the P-substrate, as shown in Fig. 18a[67, 70]. The vertical V_B is sustained by the main junction D_1 and the subjunction D_2. The new peak field of D_2 decreases the peak field at D_1. The V_B value of the REBULF LDMOS is 75% greater than that of the conventional RESURF device. Figure 18b shows another REBULF structure with a partial N floating layer[68]. The similar additional D_2 also helps to deplete the P-substrate to improve V_B. In obtaining the best

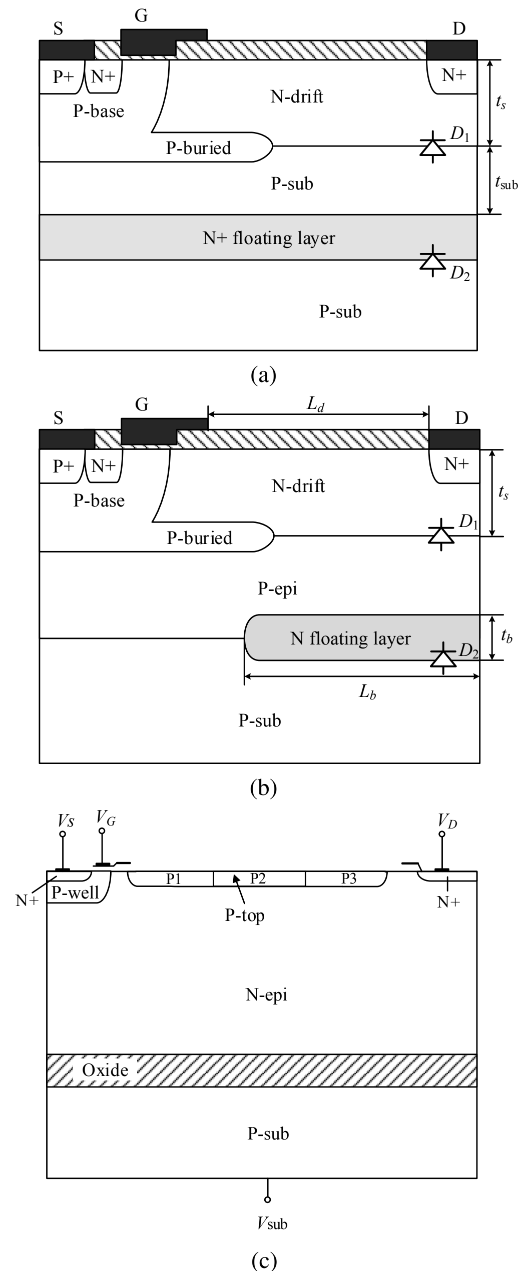


Fig. 18 Typical HV devices based on REBULF rule with (a) N+ floating layer[67]; (b) partial N floating layer[68]; and (c) substrate bias voltage V_{sub} for SOI[69].

tradeoff between V_B and $R_{\text{on,sp}}$, the following REBULF condition should be satisfied:

$$\begin{cases} N_{\text{sub}} t_{\text{sub}} \leqslant 1\times10^{12}\ \text{cm}^{-2}, \text{for N+ floating layer;} \\ N_d t_s + N_b t_b \dfrac{L_b}{L_d} = \text{const1}, \text{for partial N floating layer} \end{cases} \quad (4)$$

where N_{sub} and t_{sub} are the doping concentration and depth of the P-substrate layer above the N+ floating layer, respectively. N_d, t_s, and L_d are the doping concentration, the thickness, and the length of the drift region, respectively. N_b, t_b, and L_b are the doping concentration, the thickness, and the length of the N floating layer, respectively. "const1" is between 1.5×10^{12} and $2.5\times10^{12}\ \text{cm}^{-2}$.

The bulk electric field of the HV SOI device can also be reduced by applying a substrate bias voltage V_{sub}, as shown in Fig. 18c[69]. If a positive V_{sub} is applied at the substrate, then the high drain voltage is supported not only by the drain side, but also by the depletion layers between the source electrode and the substrate electrode. Thus, V_B of the SOI REBULF device is improved.

4 Integrated SJ Technology

SJ is the most important innovation concept in power MOSFETs, and it has been introduced into HV integrated devices to further reduce $R_{\text{on, sp}}$. However, the Substrate-Assisted Depletion (SAD) effect[71] reduces the vertical V_B of integrated SJ devices. The essence of the SAD effect is revealed by the Equivalent Substrate (ES) model[72]. This part introduces the ES mode, SJ realization technology, and typical integrated SJ devices.

4.1 ES model

The schematic diagram of the ES model is shown in Fig. 19[72]. Figure 19a illustrates the structure of the integrated SJ with a Charge Compensation Layer (CCL). The CCL and depleted substrate region are defined as the ES to analyze the impact of the substrate on the surface SJ layer, as shown in Fig. 19b. The ES model reveals the essence of the SAD effect: the charge balance between the N- and P-regions of the surface SJ is interrupted because of the ionized negative charges of the P-sub that lead to the non-full depletion of the P-pillars and decreased V_B of the conventional integrated SJ. If the SAD effect is fully eliminated, then the optimized and integrated SJ has a similar V_B to that of the vertical SJ with the same L_d, as shown in Fig. 19c. On the basis of the ES model, the optimized substrate conditions, including the equivalent charge density QES and surface electric field EES of the ES layer, is deduced as[72]

$$\begin{cases} Q_{\text{ES}} \to 0; \\ E_{\text{ES}} = \text{const2} \end{cases} \quad (5)$$

The physical means of Eq. (5) include two aspects: (1) The electrical neutrality is satisfied in the ES model, with Q_{ES} being zero. Then, the charge balance of SJ is ensured. (2) A uniform E_{ES} of the ES is realized, and thus, the premature breakdown caused by the substrate is avoided.

4.2 SJ realization technology

The key process steps of integrated SJ devices are the realizations of the surface N- and P-regions. Figure 20 shows the simplified schematics of two typical SJ realization technologies. The lateral SJ may be realized by a CMOS-compatible process with N- and P-type implantations. The SJs realized by one-time surface implantation[73, 74] or multiple implantations with the same implantation dose and different implantation energies[64] are shown in Figs. 20a and 20b, respectively. In alleviating the influences of mutual impurity diffusion and compensation, the implantations should be performed after all the

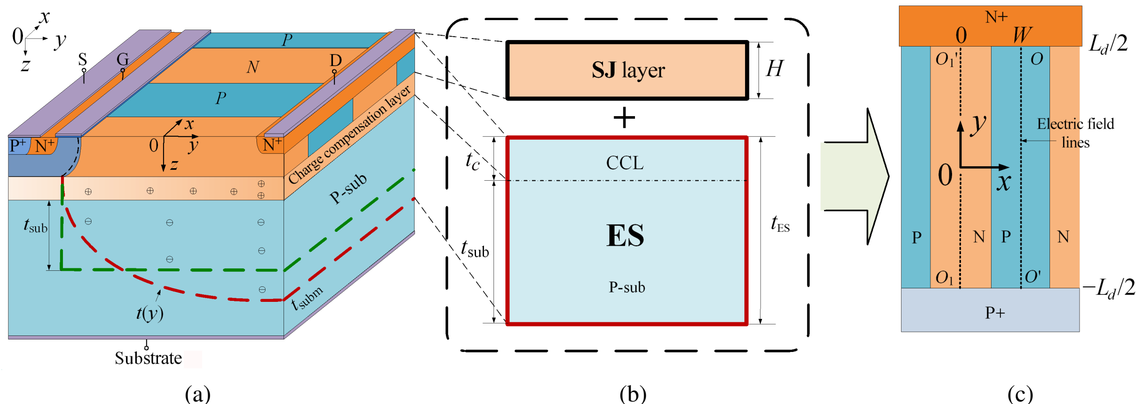


Fig. 19 Schematic diagram of ES model: (a) integrated SJ, (b) ES concept, and (c) optimized integrated SJ[72].

high-temperature processes. Moreover, the maximum implantation depth is restricted by the photoetching accuracy because of thick photoresists.

The surface SJ can also be realized by silicon trench etching and P-type epitaxy filling process[75]. Figures 20c and 20d show the simplified schematics. With this process, the SJ with a high aspect ratio in the bulk of the drift can be realized. The high quantitative etching and epitaxy filling abilities are essential in this process.

4.3 Typical integrated SJ devices

Extensive research has focused on the suppression of the SAD effect. As the SAD effect is from the unbalanced charges in the substrate, two main technologies are proposed: (1) removal of unbalanced charges in the substrate, and (2) introduction of opposite-type charge compensation.

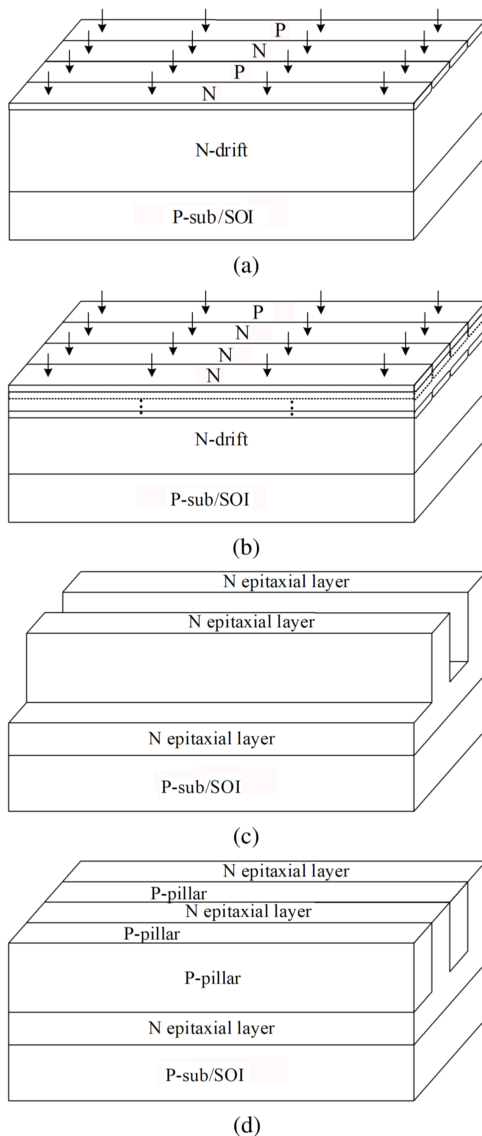


Fig. 20 Simplified schematics of integrated SJ realization technology. SJ realized by (a) one-time surface implantation[73, 74], (b) multiple implantations[64], (c) silicon trench etching, and (d) P-type epitaxy filling process[75].

Figure 21 shows the integrated SJ structures removing the unbalanced charges in the substrate via the sapphire substrate[71] or via substrate etching[76]. The optimized substrate Formula (5) is satisfied because the substrate material for generating charges is removed. However, the process compatibility is weakened by special substrates.

Typical integrated SJ structures with opposite-type charge compensations are shown in Fig. 22. N-type compensations could be introduced in different directions.

Figures 22a and 22b show the SJ structure in the x-direction[73, 74, 77, 83, 84]. An N-well or N-buffer layer is introduced under the surface SJ layer to improve V_B. Figures 22c and 22d show the SJ struture in the y-direction[58, 78, 85]. The SJ structure is only fabricated near the source, and the N-type compensation is near the source. For the SOI structure, a thin silicon layer may be adopted to enhance EC[58]. Figures 22e and 22f show the SJ struture in the z-direction[79, 86, 87]. The N-region is designed with an increased width from the source to the drain. The P-region can also be replaced by a high K material[80]. Figures 22g and 22h show the SJ structure in y- and z-directions[81, 82]. The above compensations in two directions may realize a good charge balance in the ES.

5 Conclusion and Prospect

HVICs are widely used to realize high-efficiency power conversions. HV integrated devices are the core of HVICs. This work presents a comprehensive review of the important HV integrated technologies to realize high V_B, low $R_{\text{on,sp}}$, and process compatibility. The main development directions of HV integrated technologies are new integrated technologies and HVICs in wide band gap semiconductor materials.

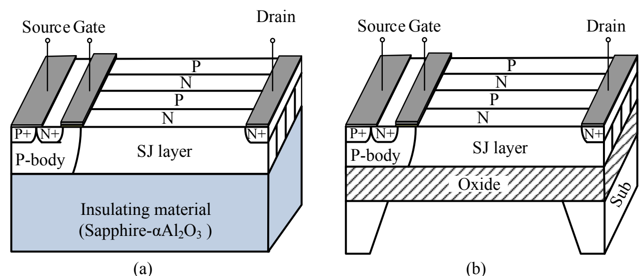


Fig. 21 Integrated SJ structures removing the unbalanced charges in the substrate, (a) with the sapphire substrate[71] and (b) with substrate etching[76].

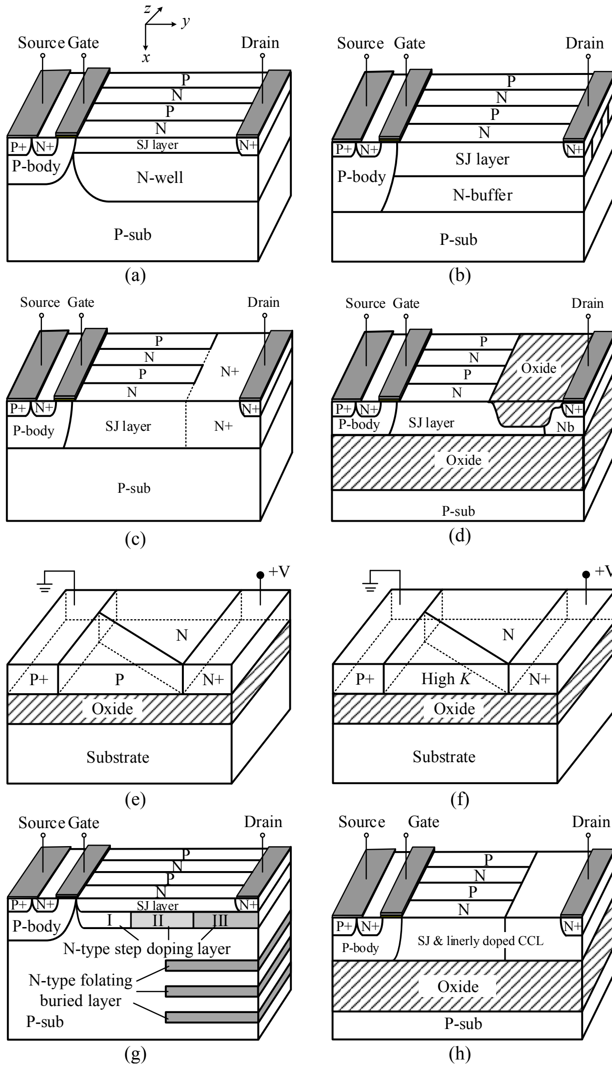


Fig. 22 Integrated SJ structures with charge compensations. Compensations in (a) and (b) in *x*-direction[77], (c) and (d) in *y*-direction[78], (e) and (f) in *z*-direction[79, 80], and (g) and (h) in *y*- and *z*-directions[81, 82].

5.1 New HVICs integrated technology

First, new integrated technologies are proposed to realize superior performance. For example, Fig. 23a shows a novel HOmogenization Field (HOF) technology for HV integrated devices[88, 89]. Periodically discrete Metal Insulator Semiconductor (MIS) structures are introduced to resistance-type VSLs. Full-region MIS depletion develops a new self-charge balance between the ionized donors in the drift and the electrons and holes in the floating electrons, as shown in Fig. 23b. The HOF technology homogenizes the surface and bulk electric fields. Therefore, the new device harvests higher V_B and lower $R_{on,sp}$ than those of the conventional RESURF technology in a much higher and wider

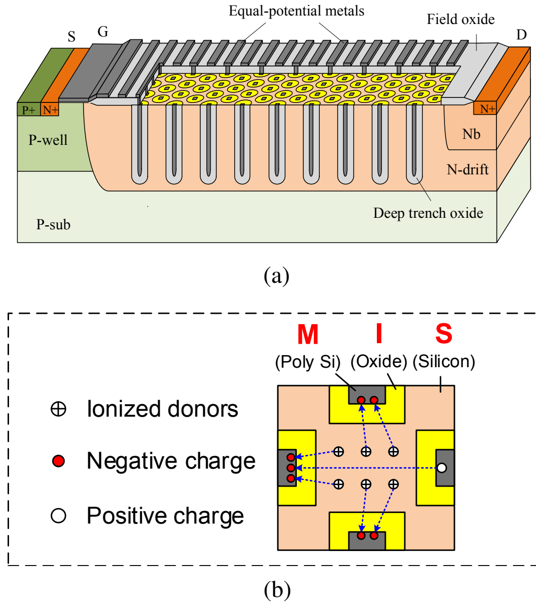


Fig. 23 New integrated technologies of (a) HOF technology for HV integrated devices[88] and (b) self-charge balance by MIS depletion.

doping dose range. Furthermore, these HV devices can be integrated with new control circuits such as the small-size AC/DC circuits[90], new functions such as ElectroStatic Discharge (ESD) protection[91], or designed by new tools such as the Asynchronous Neural Network (ANN)[92].

5.2 HV integration beyond silicon

Second, HV integrated technologies are extended to other materials, such as the wide band gap semiconductor materials GaN and SiC. Figure 24 shows the HVIC process platform based on GaN material[93–95]. The power transistors and LV peripheral devices are integrated into a single chip. Figure 25 shows the HVIC BCD process platform based on SiC material[96, 97]. BCD devices are formed by the same compatible process.

The development trend of HV integrated technology is summarized in Fig. 26. HVICs integrate HV and LV devices with multiple BCD modes to realize high integration levels and low power dissipation. Many integrated technologies, such as RESURF, ENDIF, HOFT, and JTT, are proposed to realize high performances. These technologies have been extended from silicon to SOI, SiC, GaN, etc. Single-chip heterogeneous integrations[98, 99] for HVICs may be an important development direction to combine the advantages of different materials.

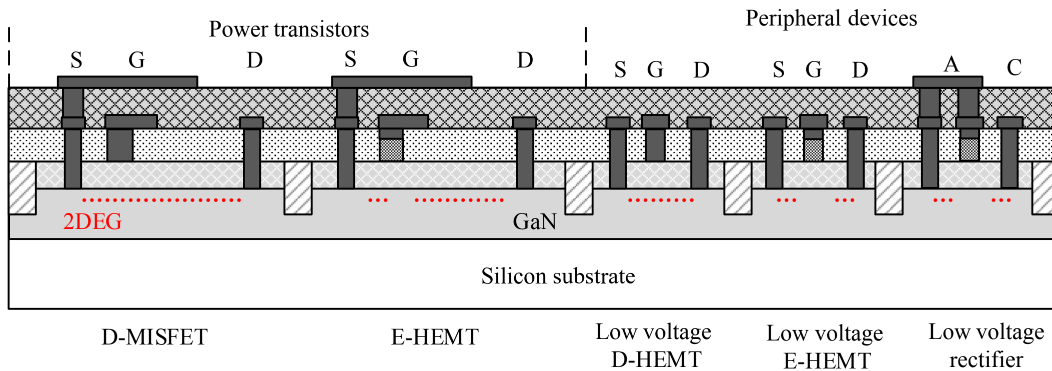


Fig. 24 HVIC process platform based on GaN material: Power transistors and LV peripheral devices[90, 91].

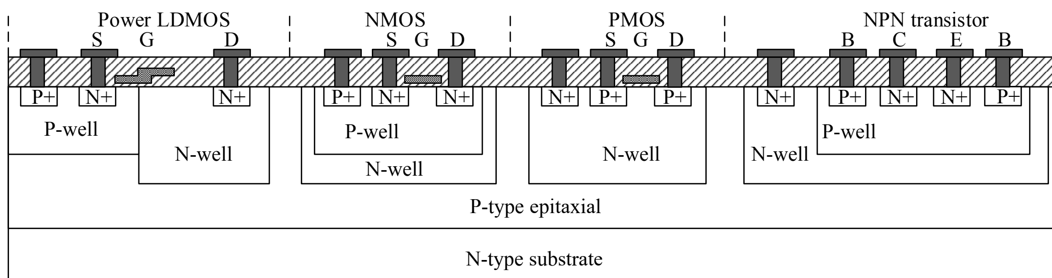


Fig. 25 HVIC process platform based on SiC material: BCD integration[96].

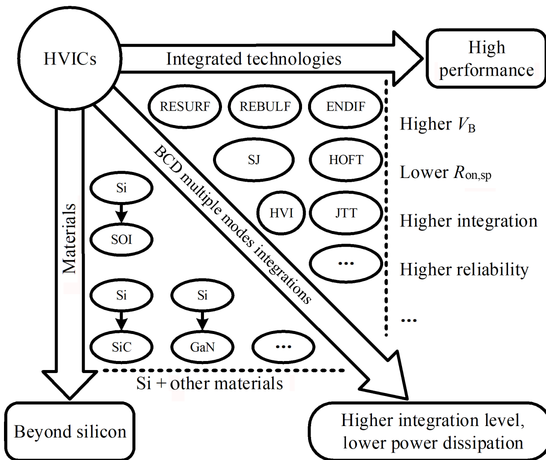


Fig. 26 Development trend of HV integrated technology.

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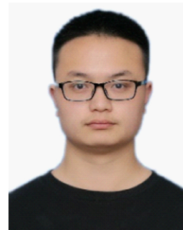

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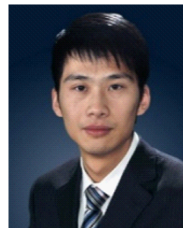

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