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A Survey of Voltage-Controlled-Oscillator-Based ΔΣ ADCs

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Abstract: The benefits of technology scaling have fueled interest in realizing time-domain oversampling (ΔΣ) of Analog-to-Digital Converters (ADCs). Voltage-Controlled Oscillators (VCO) are increasingly used to design ΔΣ ADCs because of their simplicity, high digitization, and low-voltage tolerance, making them a promising candidate to replace the classical Operational Transconductance Amplifier (OTA) in ΔΣ ADC design. This work aims to provide a summary of the fully VCO-based ΔΣ ADCs that are highly digital and scaling-friendly. This work presents a review of first-order and high-order VCO-based ΔΣ ADCs with several techniques and architectures to mitigate the nonidealities introduced by VCO, achieving outstanding power efficiency. The contributions and drawbacks of these techniques and architectures are also discussed.

Key words: Voltage-Controlled Oscillator (VCO); Analog-to-Digital Converter (ADC); oversampling (ΔΣ) ADC; time-domain signal processing; VCO-based ΔΣ ADC

1 Introduction

Analog-to-Digital Converters (ADCs) play a crucial role in many electronic systems as the bridge between the analog and digital worlds. In the era of the Internet of things, oversampling (ΔΣ) ADCs are well known for their high accuracy, despite their use of inaccurate components and relaxed analog anti-aliasing filters, making them key building blocks in many systems, such as sensors, radars, and wireless communications. However, Operational Transconductance Amplifiers (OTAs), comparators, and other key building blocks of conventional ΔΣ ADCs, which are active analog circuits, have suffered from transistor scaling in several ways. First, the intrinsic gain $g_m r_o$ of the transistor drops with a short channel length. Second, the supply voltage scaling leads to a decrease in the signal swing, which leads to a drop in the Signal-to-Noise Ratio (SNR). Under such circumstances, analog circuits rely more on high-power, multi-stage amplifiers and complicated digital calibration techniques to compensate for the drawbacks introduced by CMOS scaling. For this reason, a more "digital" solution is needed for replacing these traditional analog blocks.

Alternatively, CMOS scaling in both the transistor dimension and supply voltage leads to gate delay reduction in digital circuits. In other words, the timing resolution increases with CMOS scaling. Therefore, it is possible to process signals in the time-domain rather than in the voltage domain. Time-based ADCs have recently drawn a lot of attention, especially in the field of ΔΣ ADCs, where a Voltage-Controlled Oscillator (VCO) can be used as an integrator or quantizer. VCO-based integrators, which are simple, power-efficient, and highly digital, are promising candidates to replace power-hungry active-RC integrators in advanced processes. With ideal voltage-frequency integration, VCO-based integrators have a pole at DC, and thus, mitigate the finite gain error of traditional OTA-based integrators. With the inherent multilevel quantization of the ring VCO,

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both the reference generation and comparator design requirement are relaxed. Additionally, the VCO-based quantizer consists of only digital logic gates, which are scaling friendly and power efficient. As a result, the performance of VCO-based ADCs improves naturally with CMOS scaling.

This paper presents a review of several emerging techniques for realizing energy-efficient VCO-based ΔΣ ADCs. This paper is organized as follows. Section 2 provides a basic introduction of a VCO-based integrator and quantizer. Section 3 introduces first-order VCO-based ΔΣ ADCs with techniques for addressing the issues of VCO nonlinearity and the input parasitic pole. Section 4 presents a review of high-order VCO-based ΔΣ ADCs that effectively increases the noise shaping order of ΔΣ ADC, thereby significantly boosting the signal-quantization noise ratio of the ADCs. Section 5 concludes the paper.

2 Basic Principle

2.1 VCO-based integrator

The VCO-based integrator consists of multiple inverters. To understand the operation of the VCO, as shown in Fig. 1, five inverters are used to form a ring oscillator. The output of these five inverters corresponds to $V_{out_{1-5}}$, respectively. The gate delay of each ring stage is assumed identical and set to T. In the initial state $t = 0$, $V_{out_{1-5}}(0) = [1,0,1,0,1]$. At this time, the input and output of the first inverter are both "1". Therefore, at $t = T$, the output of inverter 1 flips to "0", which results in the input and output of the second inverter being both "0". Similarly, at $t = 2T$, the output of the inverter "0" flips to "1". With ten flipping operations ($t = 10T$), V_{out} returns to the initial state: $V_{out_{1-5}}(10T) = V_{out_{1-5}}(0) = [1,0,1,0,1]$. As a result, each output of this inverter chain is a periodic signal with a signal period of $10T$, such that this inverter chain constitutes a ring oscillator. Because T depends on the power supply voltage of the inverter, this voltage can be treated to be proportional to the output frequency of the ring oscillator. When the power supply nodes of all inverters are connected and defined as the input node of the ring oscillator, this inverter chain structure in Fig. 1 is a voltage-controlled ring oscillator, VCO. The voltage-controlled gain K_{VCO} can be expressed as the change in VCO frequency Δf_{VCO} to the change in the supply voltage ΔV_{in} ratio,

$$K_{VCO} = \frac{\Delta f_{VCO}}{\Delta V_{in}} \tag{1}$$

where the unit of K_{VCO} is Hz/V.

As shown in Fig. 1, the output of the VCO has ten different states that can be evenly represented in the phase domain from 0 to 2π. For example, if $V_{out_{1-5}} = [1,0,1,0,1]$ is defined as the phase output $\phi_{out} = 0$, the next state $V_{out_{1-5}} = [0,0,1,0,1]$ can be defined as $\phi_{out} = 1/10 \cdot 2\pi$, the next state $V_{out_{1-5}} = [0,1,1,0,1]$ can be defined as $\phi_{out} = 2/10 \cdot 2\pi$, and so on. The VCO output phase ϕ_{out} can be expressed as

$$\Delta\phi_{out} = 2\pi \cdot f_{VCO} \cdot t \tag{2}$$

Combining Eqs. (1) and (2), the Laplace transformation of $\frac{\phi_{out}(s)}{V_{in}(s)}$ can be represented as

$$\frac{\phi_{out}(s)}{V_{in}(s)} = \frac{2\pi \cdot K_{VCO}}{s} \tag{3}$$

Equation (3) proves that the VCO is an ideal integrator with infinite DC gain.

2.2 VCO-based quantizers

Because the VCO output phase is an integral of its control voltage, differentiation of the quantized phase output of the VCO is necessary to quantize the control voltage of VCO. For the realization of the quantizer and differentiator, the most direct implementation is the calculation of the number of edges of the VCO output in each sampling period[1]. As shown in Fig. 2,

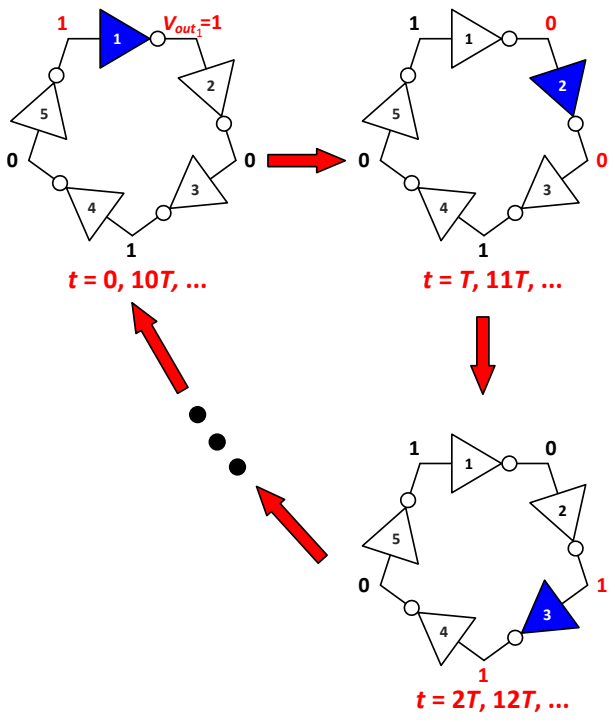

Fig. 1 Inverter-based VCO operation diagram.

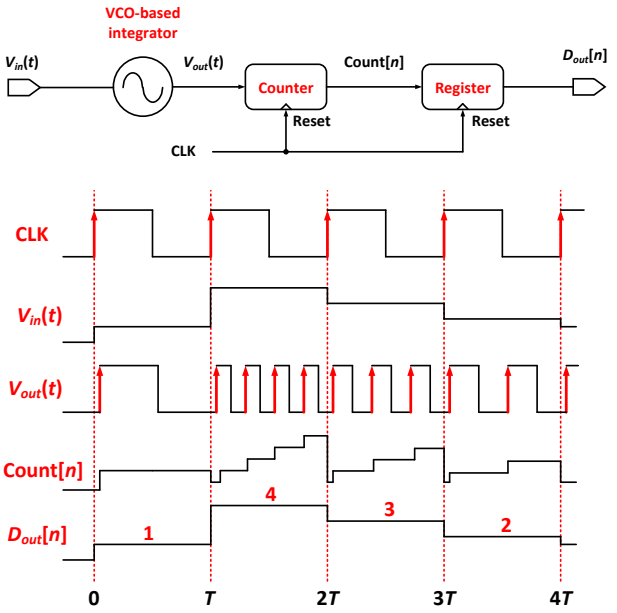

Fig. 2 Edge-counting-based V-F phase quantizer.

the quantization result was obtained by counting the number of edges of the VCO output in each clock cycle. This edge-counting-based quantization converts the phase information into a digital output. Every time the rising edge of the master clock passes, it will trigger the counter and register to be cleared, which is equivalent to a differential operation in the digital domain. Notably, the edge-counting-based quantizer also performs a first-order differentiation during reset by effectively subtracting the previously quantized VCO phase. As shown in the timing diagram of Fig. 2, the sampled counting number is proportional to the oscillation frequency of the VCO, and therefore, the input signal. Therefore, this voltage-frequency-digital quantization is called V-F quantization.

Another implementation method[2] of V-F quantization is to sample each output phase of the VCO. Each VCO output is sampled by a D Flip-Flop (DFF) and then sent to a differentiator to produce the final digital output. The first traditional implementation method[2] is to sum all phase outputs and convert them to binary code, and then subtract the previous binary code through a digital subtractor to get the final output. The disadvantage of this is that the implementation of a multi-bit subtractor is more complicated; its complexity especially grows with the increase in the output resolution. An improved phase-encoding method[3] is shown in Fig. 3. Using an XOR gate array to perform a first-order differentiation, the output of each bit is added to produce the final output. With full use of the multiple phase outputs, the phase-encoding method increases the quantizer resolution by $\log_2(M)$, where M is the number of VCO phases.

Figure 3 is an example where the VCO is assumed to have five inverters. In the first clock cycle when the input voltage is relatively small, only one inverter is flipped (i.e., the output of the first bits is changed from "0" to "1"). The other four outputs remain unchanged. By summing the XOR gate array output "10000", the output of the quantizer is 1. Similarly, as a larger input comes in the second clock cycle, four inverter outputs

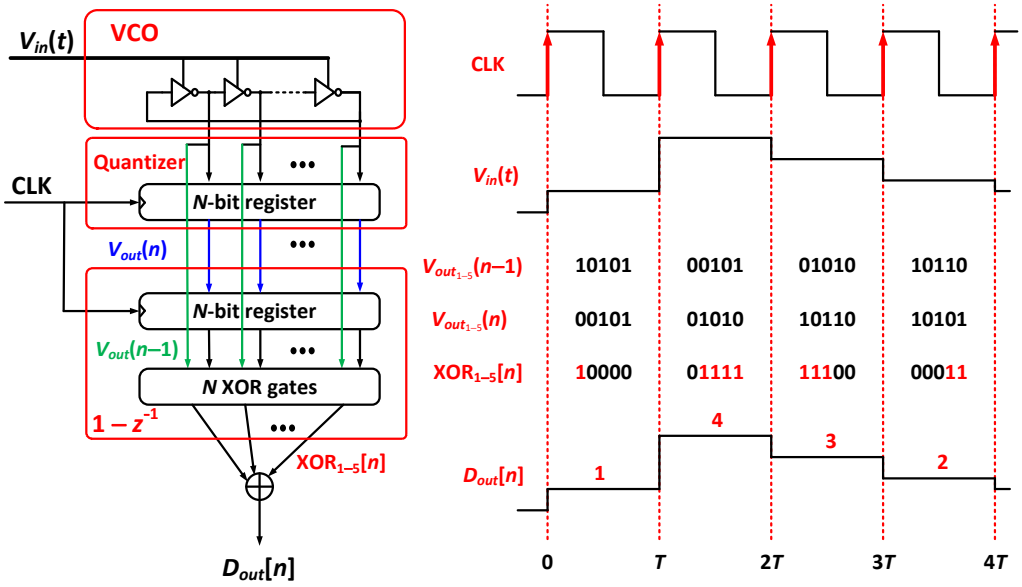

Fig. 3 Phase-encoding-based V-F phase quantizer.

are flipped. Thus, the output of the XOR gate array is "01111", resulting in a quantizer output of 4.

It is also possible to use the quantized phase output as the desired output, which is called "V-P" quantization, without differentiation. Unlike "V-F" quantization, the XOR gate performs as a phase differentiation of the VCO output and reference phases. As shown in Fig. 4, the phase difference of the VCO and reference is generated as a Pulse Width Modulation (PWM) waveform. Using the XOR gate array to access all VCO output nodes, a series of evenly delayed PWM waveforms can be captured. Therefore, "V-P" quantization naturally provides a thermometer code that represents a quantized spatial average of the phase difference. Because the VCO integrator has a very high gain in the signal bandwidth, the extraction of the phase information is possible by feeding back the phase to the input of the VCO to mitigate the VCO nonlinearity issue (more details are provided in Section 3).

3 First-Order VCO-Based ΔΣ ADC

3.1 Open-loop ΔΣ ADC

As discussed in Section 2.2, both edge-counting-[1] and phase-encoding-[2, 4] based quantizers convert the input signal from the voltage domain to the digital domain, and offer intrinsic first-order noise shaping. Thus, these quantizers can be directly used as an open-loop first-order VCO-based ΔΣ ADC. The edge-counting quantizer only obtains one output phase information of the VCO, and thus, wastes the phase information of the other outputs. As a result, the counter hardware complexity and VCO speed, which are proportional to the power consumption, are exponentially increased with the quantizer resolution. The multi-edge-counting[2] technique relieves the requirement of VCO speed; however, the counter complexity is not improved. An improved method[4] with phase-encoding shows great power efficiency. However, the nonlinear tuning response of the VCO then becomes an issue. Despite the even-order harmonics that can be eliminated using a pseudo-differential scheme, based on Ref. [2], the linearity of the VCO becomes less than 7 bits with an input amplitude of 150 mV.

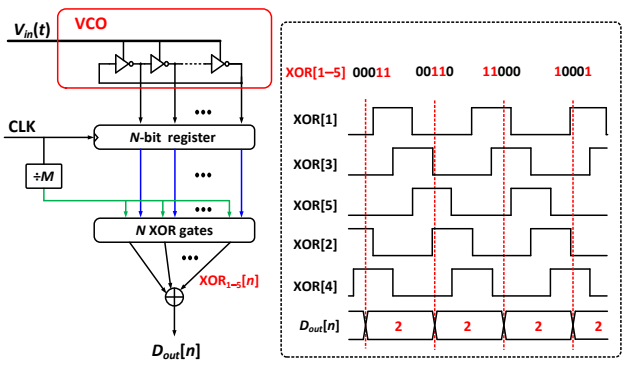

Fig. 4 Phase-differentiator-based V-P phase quantizer.

In recent years, several directions are used to solve the nonlinearity issue of the VCOs. The most straightforward method is to make the tuning curve "straightened" with the aid of calibration. As shown in Fig. 5, Kim et al.[5] and Daniels et al.[6] proposed foreground calibration in the open-loop ΔΣ ADC. By applying a ramp signal to the VCO-based quantizer, the nonlinear coefficients can be extracted and stored in a LookUp Table (LUT). As a result, the inverse transfer function of the VCO tuning curve can be generated based on the LUT. The hardware complexity of these foreground calibrations is relatively low. However, these calibrations cannot track the Process-Voltage-Temperature (PVT) variation or coefficient drift during equipment aging.

Instead of using foreground calibration, background calibration techniques adopting a replica VCO-based quantizer as a calibration unit to correct VCO nonlinearity in the open-loop architecture have been proposed, as shown in Fig. 6[4, 7, 8]. Taylor and Galton[4, 7] used jitter to extract nonlinear terms, while Rao et al.[8] used background ramping, which is similar to the work of Kim et al.[5]. However, these techniques rely on replica matching, which is nontrivial in guaranteeing over-process variations. Additionally, to ensure that the nonlinearity of the VCO is not too large, the input signal swing is still limited, leading to an overall SNR loss.

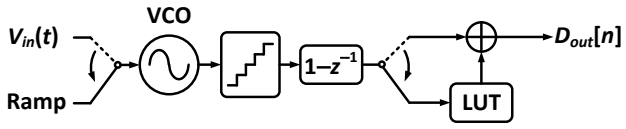

Fig. 5 Block diagram of the foreground calibration for VCO nonlinearity.

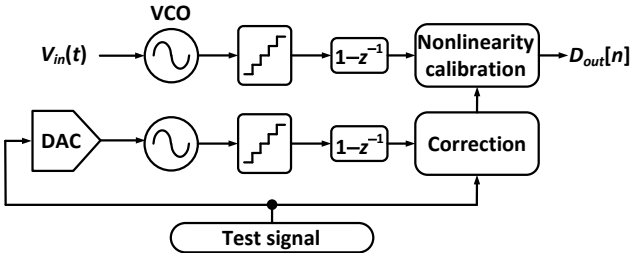

Fig. 6 Block diagram of the background calibration for VCO nonlinearity.

Apart from digital calibration, Babaie-Fishani and Rombouts[9] proposed an analog calibration to improve the VCO linearity. As shown in Fig. 7, two resistors are added in front of VCO to perform a mixture of the current and voltage mode controls. The input current of VCO can be mathematically expressed as

$$I_{VCO} = V_{ctrl} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{in}}{R_1} \tag{4}$$

Because the tuning curve of the current control of VCO (I_{VCO} versus VCO frequency) and control voltage versus the input voltage curve (V_{ctrl} versus V_{in}) exhibits an opposite curvature, both nonlinear effects will cancel out each other by carefully adjusting the proportion of the resistors R_1 and R_2.

3.2 Close-loop ΔΣ ADC

Another scenario of addressing the VCO nonlinearity issue is minimizing the signal swing of the VCO input by putting VCO into a closed loop. The system-level architecture is shown in Fig. 8. A V-P quantizer captures the VCO phase information and then converts it to digital output, which controls the feedback path to suppress the signal swing of the VCO input. Notice that the phase quantizer discussed in Section 2.2[10] can be used in this closed-loop structure. However, the need for a reference clock requires a fixed VCO running frequency. Additionally, the multi-bit VCO-based quantizer renders the multi-bit DAC sensitive to element mismatch.

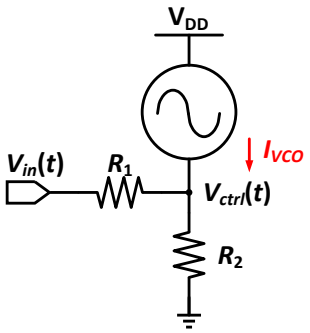

Fig. 7 Schematic of the analog calibration for VCO nonlinearity.

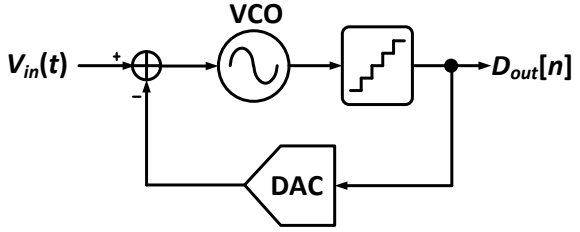

Fig. 8 Closed-loop first-order VCO-based ΔΣ architecture.

To address these issues, a pseudo-differential dual-VCO structure is adopted to relieve the speed constraint of VCOs[11], leading to power and noise reduction of VCOs, as shown in Fig. 9. Additionally, the output pattern of this dual-VCO structure has intrinsic Clock Level Averaging (CLA), which modulates DAC mismatch away from the signal band. In this case, a dynamic element matching circuit is eliminated, which further reduces the power and circuit complexity.

One drawback of the XOR-based quantizer is that it can only detect the phase difference of the dual-VCO between 0 to π without the lead-lag status, leading to a small detecting range and resolution. Figure 10 shows the Phase-Extended Quantizer (PEQ) technique[12] based on the XOR method. By accessing all output nodes of the VCO, the lead-lag information can be extracted by extra digital logics, thus doubling the phase detecting range and resolution. Additionally, the lead-lag signal can be converted to a tri-level pattern of DAC control, which retains the intrinsic CLA mechanism and simultaneously enables power reduction for the DAC.

Another method that naturally extracts the lead-lag status is to employ a Phase/Frequency Detector (PFD) as the quantizer, as is shown in Fig. 11[13]. Unlike the XOR gate, the PFD-based quantizer outputs the phase

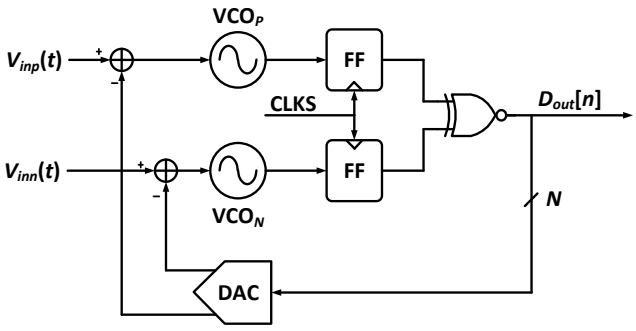

Fig. 9 Dual-VCO architecture with an XOR-based quantizer.

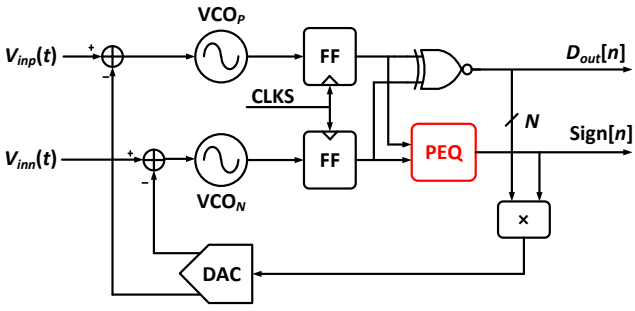

Fig. 10 Dual-VCO architecture with a phase-extended quantizer.

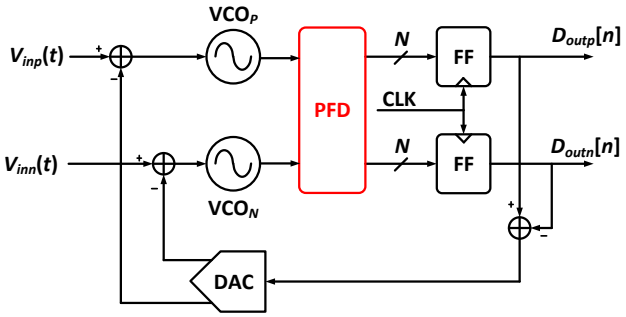

Fig. 11 Dual-VCO architecture with a PFD-based quantizer.

difference by detecting the rising edge of the inputs in each oscillation cycle, and thus ensures full range (-2π to 2π) detection of the VCO phase information. The delay of the PFD is treated as a PVT-sensitive Excess Loop Delay (ELD), and this configuration may not work for high-speed applications.

A potential issue of the closed-loop structure in Fig. 8 is that the parasitic pole of the VCO input may cause ELD, thereby degrading the loop stability, especially in high-speed applications. As shown in Fig. 12, Mukherjee et al.[14] introduced a distributed-input VCO topology that inherently alleviates the effect of the parasitic pole while retaining the benefits of the fully differential operation. By splitting the input transconductor into a set of distributed transconductors to isolate internal nodes, the parasitic pole is moved to a very high frequency, which has a negligible effect on the ADC.

Instead of using a feedback loop to address the VCO nonlinearity issue, an alternative for closed-loop operation is to use the feedforward architecture. As shown in Fig. 13, Xing and Gielen[15] proposed a two-step structure by separately employing two VCO-based quantizers acting as coarse and fine quantizers. Although distortion error exists at both coarse and fine VCO-based quantizers, the nonlinearity of the first stage VCO (VCO_1) will be ideally canceled out when the outputs of coarse and fine quantizers are summed. The second stage VCO (VCO_2) will not suffer from VCO

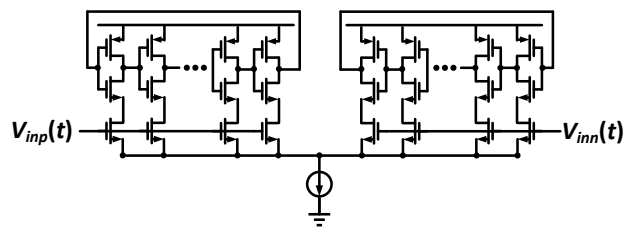

Fig. 12 Diagram of the distributed-input VCO topology at the transistor level.

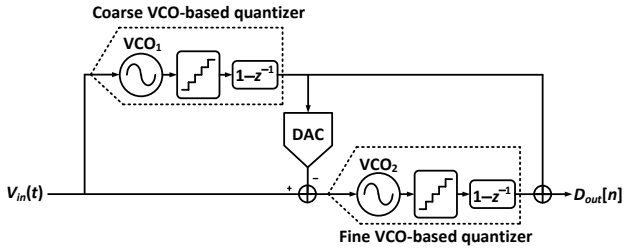

Fig. 13 Two-step feedforward VCO-based ΔΣ ADC.

nonlinearity as the input swing of the quantizer is very small. Unfortunately, the gain mismatch of the coarse and fine quantizers and delay of the coarse quantizer will cause noise leakage, leading to performance degradation. Additionally, the first-order noise-shaping nature of this architecture is insufficiently power efficient because it uses two VCO-based quantizers.

4 High-Order VCO-Based ΔΣ ADC

Higher noise shaping order is required to realize higher resolution or bandwidth for ΔΣ ADC. Cardes et al.[16] cascaded additional VCOs to realize the second-order ΔΣ ADC that is illustrated in Fig. 14a. Using two feedback loops with up-down counters, the Cascade of Integrators with FeedBack (CIFB) structure is built to make the system stable. The output bits of the up-down are only 2, as long as the VCOs running frequency is less than sampling frequency and the maximum running frequency of VCO_2 is greater than the running frequency of VCO_1. In this case, as the schematic shows in Fig. 14b, the up-down counter consists of only

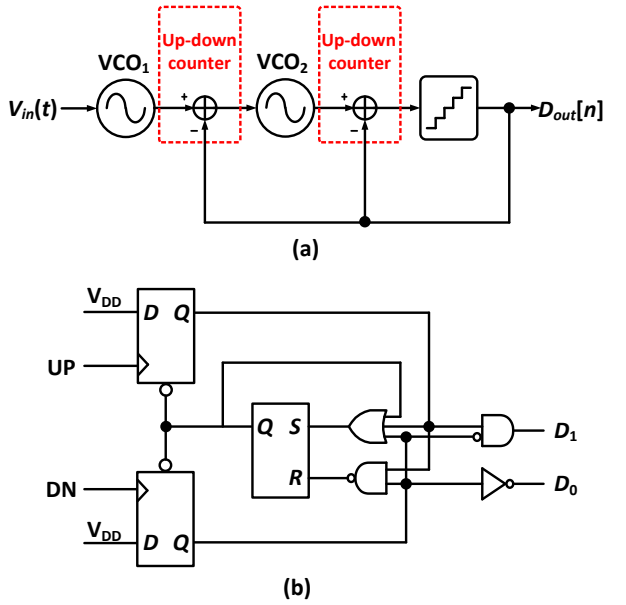

Fig. 14 Architecture of the second-order VCO-based ΔΣ ADC with time-domain feedback.

three flip-flops and few digital gates compared with the conventional counter. Notice that the feedback paths are connected to the VCO output, but not to the input. In this case, the first stage VCO operates in an open-loop manner that still suffers from the VCO nonlinearity issue.

Zhong et al.[17] and Jayaraj et al.[18] proposed a VCO-based second-order ΔΣ ADC by cascading two VCOs in one ΔΣ loop. This closed-loop structure minimizes the ripple of the first VCO input node, thereby addressing the nonlinearity issue of the front end. Interestingly, the loop mechanism of a Digital Phase-Locked Loop (DPLL) was leveraged, in which any perturbation of the VCO input node will be forced to cancel[17, 18]. Based on this idea, an input is inserted as an intentional disturbance to the VCO. Because the control voltage tracks the disturbance, the quantizer output can easily be used as a digital representation of the input signal, as shown in Fig. 15a. Because the phase-encoding quantizer provides an extra order of noise shaping, the quantization noise of the ΔΣ ADC is shaped in the second-order. Notably, as shown in Fig. 15b, the loop filter consists of two integrators and one differentiator (one integrator and one differentiator cancel each other). From the system-level perspective, the ΔΣ loop is similar to a first-order system; however, it provides second-order noise shaping because of the discrete-time nature of the quantizer, leading to improved system stability. Unlike the single-PFD by Jayaraj et al.[18], a multi-PFD was applied for spatial averaging[17]. This technique greatly increases the information update rate of the VCO, and thus reducing the requirement of a VCO center frequency, resulting in a significant reduction of VCO power and noise. Similar to Ref. [12], the work done in Ref. [17] facilitated a tri-level pattern of DAC control, which leads to a thermal noise

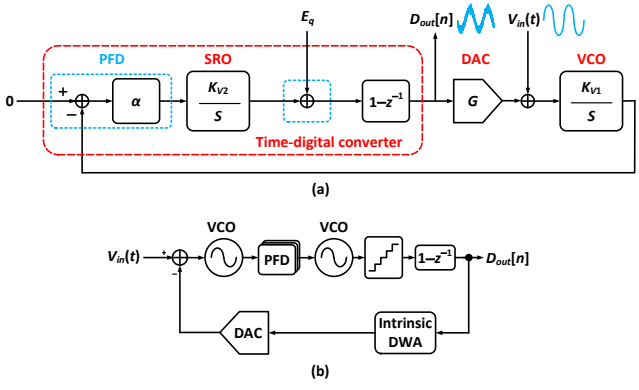

Fig. 15 Architecture of the second-order VCO-based ΔΣ ADC from (a) DPLL and (b) ΔΣ ADC perspectives.

reduction/linearity improvement, and simultaneously retains the intrinsic data weighted averaging mechanism.

To further extend the noise shaping order, Babaie-Fishani and Rombouts[19] cascaded three VCOs in the loop, building a third-order VCO-based ΔΣ ADC. Figure 16 presents the block diagram of the architecture. Similar to Cardes et al.[16], the feedback operations are mostly processed in the digital domain using 1-bit up-down counters and DFFs, which is very scaling friendly and easy to design. The open-loop manner of the first VCO-based integrator still suffers from the nonlinearity of the VCO control curve because of the high input swing. In this work, the analog calibration[9] mentioned in Section 3.1 is used to mitigate this issue.

Another interesting implementation of second-order VCO-based ΔΣ ADC is the use of a hybrid passive RC and VCO architecture[20], which is shown in Fig. 17. Instead of suppressing the undesired parasitic VCO input node[14], this hybrid architecture utilized the inherent parasitic effect to form a passive integrator. Therefore, second-order noise shaping is achieved and the need for parasitic cancellation is eliminated. Additionally, only a negligible noise penalty is introduced by the passive integrator.

An alternative to realizing a high-order VCO-based ΔΣ ADC is to use a Multi-stAge noise-SHaping (MASH) structure. Maghami et al.[21] realized second-order noise shaping using a 1-1 MASH VCO-based ADC with two VCO-based ΔΣ ADCs. As shown in Fig. 18, the first stage is a closed-loop VCO-based ΔΣ ADC that addresses the nonlinearity issue of the

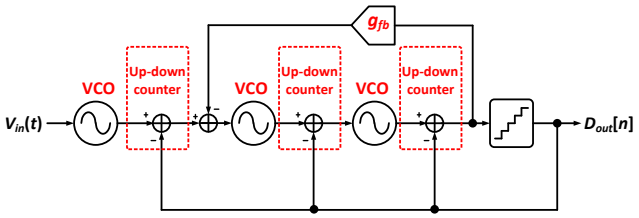

Fig. 16 Architecture of the third-order VCO-based ΔΣ ADC with time-domain feedback.

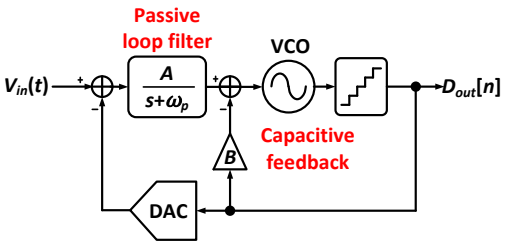

Fig. 17 Architecture of the second-order VCO-based ΔΣ ADC using a passive integrator.

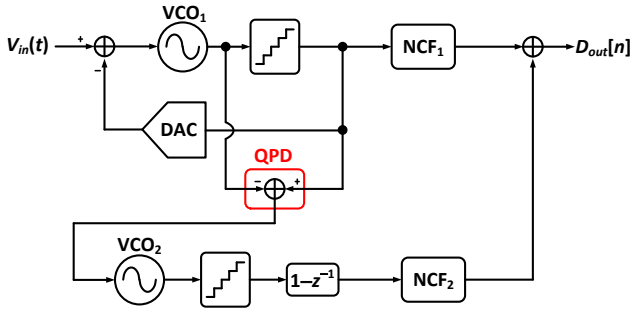

Fig. 18 Architecture of 1-1 MASH second-order VCO-based ΔΣ ADC using a QPD.

VCO. The quantization noise is extracted as a PWM signal using a Quantization Phase Detector (QPD) block and applied to the second stage for fine quantization. Because the PWM signal only has two levels, VCO_2 only runs at two frequencies, which is highly linear. Thus, the open-loop second stage is immune to VCO nonlinearity. Notably, this architecture still suffers from noise leakage because of the gain mismatch between the first and second stages. Gain calibration or quantization level enhancement, which consumes more digital power, are two options to address this issue.

5 Conclusion

Over the past two decades, VCO-based ΔΣ ADCs have benefited tremendously from technology scaling and have become one of the most popular ADC architectures for energy-efficient applications. This paper reviewed several emerging techniques that can effectively suppress major nonidealities, thereby realizing power-efficient, scaling-friendly VCO-based ΔΣ ADCs. Both foreground and background calibration techniques are first introduced, which effectively mitigates the nonlinearity issue of the VCO. The VCO can also be placed in a closed loop to minimize the VCO input swing, suppressing the VCO nonlinearity. Cascading VCOs in one ΔΣ loop and employing a MASH architecture can be used to effectively increase the noise shaping order of ΔΣ ADC, thereby significantly boosting the resolution or bandwidth of the VCO-based ΔΣ ADCs while maintaining the high energy efficiency and scaling friendliness. Table 1 presented a summary of the state-of-the-art VCO-based ADC implementations. With the continuous technical innovations, the VCO-based architectures are expected to be a promising candidate for realizing energy-efficient and scaling-friendly ADCs.

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Table 1 Performance summary and comparison of state-of-the-art VCO-based ADC implementations.

Reference	Year	Noise shaping order	Process (nm)	Fs (MHz)	OSR	BW (MHz)	Power (mW)	SNDR (dB)	DR (dB)	FoM_s1* (dB)	FoM_s2** (dB)
[7]	2013	1st	65	1600	64.0	12.50	17.5	74.0	77.0	162.5	165.5
[8]	2014	1st	90	640	64.0	5.00	4.10	74.7	77.0	165.6	167.9
[12]	2017	1st	130	250	62.5	2.00	1.05	74.7	77.6	167.5	170.4
[19]	2017	3rd	65	1600	80.0	10.00	3.70	65.7	71.0	160.0	165.3
[16]	2018	2nd	130	20	500.0	0.02	0.56	76.6	98.5	152.1	174.0
[20]	2020	2nd	40	330	27.5	6.00	0.52	68.6	70.8	169.2	171.4
[17]	2020	2nd	40	260	25.0	5.20	0.86	69.4	72.3	167.2	170.1
[21]	2020	2nd	65	125	31.3	2.00	1.25	79.7	92.7	171.7	174.7

Notes: *: FoM_s1 = SNDR + $10\log_{10}$ (BW/Power).
**: FoM_s2 = DR + $10\log_{10}$ (BW/Power).

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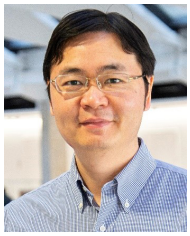

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