TSINGHUA SCIENCE AND TECHNOLOGY
ISSN 1007-0214 01/18 pp1–12
DOI: 10.26599/TST.2020.9010030
Volume 27, Number 1, February 2022

Anti-Interference Low-Power Double-Edge Triggered Flip-Flop Based on C-Elements

Zhengfeng Huang, Xiao Yang, Tai Song, Haochen Qi, Yiming Ouyang, Tianming Ni, and Qi Xu*

Abstract: When the input signal has been interfered and glitches occur, the power consumption of Double-Edge Triggered Flip-Flops (DETFFs) will significantly increase. To effectively reduce the power consumption, this paper presents an anti-interference low-power DETFF based on C-elements. The improved C-element is used in this DETFF, which effectively blocks the glitches in the input signal, prevents redundant transitions inside the DETFF, and reduces the charge and discharge frequencies of the transistor. The C-element has also added pull-up and pull-down paths, reducing its latency. Compared with other existing DETFFs, the DETFF proposed in this paper only flips once on the clock edge, which greatly reduces the redundant transitions caused by glitches and effectively reduces power consumption. This paper uses HSPICE to simulate the proposed DETFF and other 10 DETFFs. The findings show that compared with the other 10 types of DETFFs, the proposed DETFF has achieved large performance indexes in the total power consumption, total power consumption with glitches, delays, and power delay product. A detailed analysis of variance indicates that the proposed DETFF features less sensitivity to process, voltage, temperature, and Negative Bias Temperature Instability (NBTI)-induced aging variations.

Key words: Double-Edge Triggered Flip-Flop (DETFF); glitch; low-power; C-element

1 Introduction

With the continuous progress of integrated circuit technologies, the scale of integrated circuits is also constantly expanding. On the one hand, more advanced processes bring integrated circuit technologies to the deep sub-micron stage, on the other hand, the degree of integration is getting higher with multiplying the number of transistors. These changes have made the problem of integrated circuit power consumption more prominent[1]. In recent years, the rapid increase in portable consumer electronic equipment and circuit operating clock frequency has enlarged the need to reduce power consumption in the circuit design[2]. Therefore, low-power consumption is one of the key challenges in modern integrated circuit designs.

For a digital integrated circuit, the power consumption of its sequential circuits accounts for a very large proportion of the total power consumption. In the design of sequential circuits, the clock system is mainly composed of a clock tree circuit and sequential units. The power consumption on the sequential circuits is the main source of all power consumption[3, 4]. As sequential elements in an integrated circuit, flip-flops are widely used in finite-state machine controllers, pipeline circuits, or storage elements, and their power consumption can account for 20%–45% of the total power consumption of

• Zhengfeng Huang, Xiao Yang, Tai Song, Haochen Qi, and Qi Xu are with School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei 230601, China. E-mail: huangzhengfeng@139.com; yangxiao@mail.hfut.edu.cn; baikediguo@163.com; ammyqi@hfut.edu.cn; xuqi@hfut.edu.cn.
• Yiming Ouyang is with School of Computer and Information, Hefei University of Technology, Hefei 230601, China. E-mail: oyymbox@163.com.
• Tianming Ni is with School of Electrical Engineering, Anhui Polytechnic University, Wuhu 241000, China. E-mail: timmyni126@126.com.
∗ To whom correspondence should be addressed.
Manuscript received: 2020-07-30; accepted: 2020-09-01

the circuit[5]. A low-power flip-flop designed as a basic component can provide huge advantages for reducing the total power consumption of integrated circuits.

The clock tree circuit provides the clock signal for the entire sequential circuit, so its output load is relatively large, resulting in a relatively large transistor size, which results in a greater power consumption, and can usually account for approximately 40% of the total power consumption of the circuit, so an effective control is needed[6–8]. There are many ways to reduce the power consumption of the clock tree, such as reducing the clock load capacitance and reducing the frequency of the clock signal. This study uses clock gating technology. When the signal at the input of the flip-flop remains unchanged, we temporarily turn off the corresponding transistors to reduce their dynamic power consumption. This study also uses improved static C-elements, which can block the glitches on the input signal due to various aspects of interference. When there is a glitch on the input signal and it is passed inside the flip-flop, redundant transitions of internal nodes may occur, resulting in additional power consumption overhead. Reducing the redundant transitions of internal nodes can reduce the power consumption of the circuit.

In Complementary Metal Oxide Semiconductor (CMOS) circuits, the power consumption of the circuit mainly comes from dynamic power consumption, that is, the frequent charging and discharging of circuit nodes. Dynamic power consumption is expressed as[9]

$$P_d = C_L V_{\mathrm{dd}}^2 f_{\mathrm{clk}} \alpha \tag{1}$$

where P_d is the dynamic power consumption; α is the switching activity, that is, the number of output transitions in each clock cycle; C_L is the node capacitance; V_{dd} is the power supply voltage; and f_{clk} is the clock frequency. In addition, in digital integrated circuit signal transmission, massive glitches are usually generated due to various interferences. Although these glitches may not affect the function of the circuit, it will cause massive redundant transitions and generate additional power consumption, approximately 20%–70% of the total power consumption[10]. Blocking glitches due to signal interference can effectively reduce circuit power consumption.

Flip-flops can be divided into Single-Edge Triggered Flip-Flops (SETFFs) and Double-Edge Triggered Flip-Flops (DETFFs). Because traditional SETFFs have half the clock edges that are not sampled, DETFFs appear. To take advantages of other idle clock edges for sampling, ideally, given the same clock frequency, a double-edge flip-flop can double the throughput or maintain the same throughput when working at half the clock frequency of an SETFF[9–12].

This paper is divided into the following parts: Section 2 outlines three typical DETFFs, namely, multiplexer-type DETFFs, C-element-type DETFFs, and pulse-type DETFFs. Section 3 describes the proposed DETFF, including the circuit structure, working principle, and simulation results. Section 4 comprehensively analyzes the circuit performance of the proposed structure and other 10 DETFFs. Section 5 discusses the variance analysis. Section 6 presents a summary of this paper.

2 Existing DETFF

2.1 Multiplexer-type DETFFs

Figure 1 shows a multiplexer-type DETFF LM1[13], which includes a multiplexer (MUX), and a clock tree consisting of two inverters and two internal latches (LA1 and LA2). The input signal is D and the output signal is Q.

LM1 uses two latches and a multiplexer. The first and second latches sample data when the clock signal CLK is high and low, respectively. The multiplexer will be in the logic value selection of the hold mode latch for the output.

The disadvantage of LM1 is that the state of the latch in the transparent mode will change with the change in the input signal, resulting in redundant transitions. When the input signal has glitches due to various interferences, the latch in the transparent mode will generate more redundant transitions, which increases the power consumption of the circuit. The more glitches the input signal has, the higher the power consumption overhead is.

Figure 2 shows the structure proposed in Ref. [13]. LM2 is also composed of two latches, a clock tree composed of two inverters, and a multiplexer. Compared

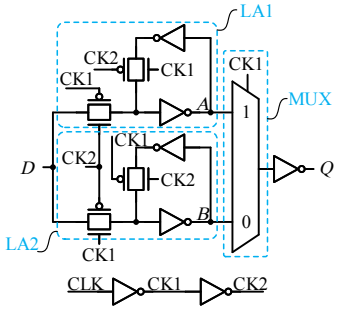


Fig. 1 Structure of DETFF LM1.

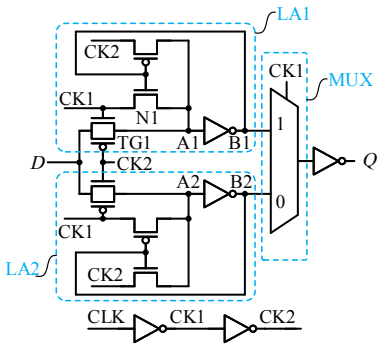


Fig. 2 Structure of DETFF LM2.

with LM1, LM2 uses two transistors instead of the transmission gate and inverter in two latches.

There are two main problems with LM2. First, in the feedback path of the two latches of LM2, the input signal controls the transmission of the clock signal, causing the output load of the clock tree to be large[14, 15], and the overall power consumption will be relatively large. Second, LM2 also encounters the level conflict problem[7]. For example, when CLK is 0, CK1 is 1, CK2 is 0, and the transmission gate TG1 turns on. When D is 0, A1 switches to 0 and B1 switches to 1, causing transistor N1 to turn on. Therefore, node A1 will be simultaneously written with 0 and 1, causing a level conflict. Similarly, when CLK and D are both 1, another latch node A2 will also have a level conflict problem. This problem will greatly increase the power consumption of LM2. Finally, LM2 encounters redundant transitions caused by glitches in the input signal, which leads to excessive power consumption.

A multiplexer-type DETFF TCRFF was introduced in Ref. [16], whose structure is shown in Fig. 3. The TCRFF uses stacking technology and includes a multiplexer, a clock tree composed of two inverters, two latches of stacked MOS transistors, and multiplexed MOS transistors P1 and N3 controlled by the input signal D.

The TCRFF uses stacking technology at the clock

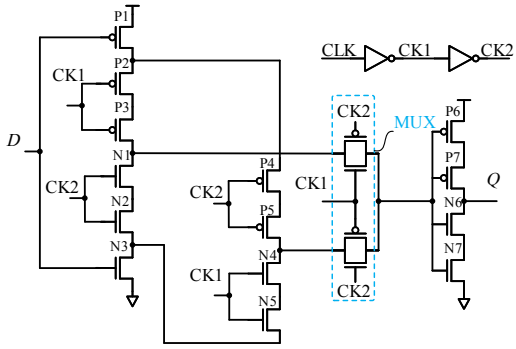


Fig. 3 Structure of DETFF TCRFF.

signal input ends of the two latches to reduce its leakage current. When input $D = 0$, if CLK is high, CK1 = 0 and CK2 = 1. At this time, P1, P2, and P3 are turned on. When the CLK edge arrives and CLK becomes low, then CK1 = 1 and CK2 = 0. At this time, P1, P4, and P5 are turned on. When the clock signal CLK switches, the multiplexer selects again[17].

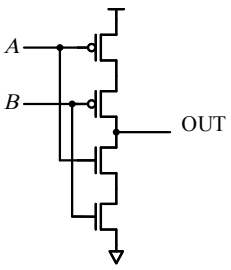
The disadvantage of the TCRFF also comes from the use of Metal–Oxide–Semiconductor Field-Effect transistor (MOSFET) stacking technology. Compared with the structure without stacked transistors, the driving current using stacked MOSFET will be much smaller, resulting in a higher propagation delay.

2.2 C-element-type DETFFs

The C-element introduced in Ref. [18] is usually a three-terminal device with two inputs and one output. When both inputs are the same, the output will switch to the input value. When the inputs are not the same, the previous output is retained. The device can act as a latch that can be set and reset with the appropriate combination of signal levels at the inputs.

At the same time, the C-element has the function of blocking glitches. The circuit structure of the two-input C-element and its truth table are shown in Fig. 4. When the two-input states of the C-element are the same, the function of the C-element is to reverse the input signal. When the two inputs of the unit are not the same, the output of the C-element remains unchanged. When there is a glitch in one of the data inputs in the C-element and the other data are correctly inputted, it can be known from the truth table of the C-element that the glitch will not affect the C-element. The output of the device is not affected, and the glitch is not transmitted to the next stage circuit[19, 20].

Figure 5 shows the C-element-type DETFF LM_C. LM_C contains a clock tree, transmission gates, keepers, and a C-element. Compared to the multiplexer-type DETFF, LM_C uses two inputs of C-elements to reduce the clock load of the circuit and clock tree power



A	*B*	OUT
0	0	1
1	1	0
0	1	Hold
1	0	Hold

Fig. 4 Two-input C-element circuit and the truth table.

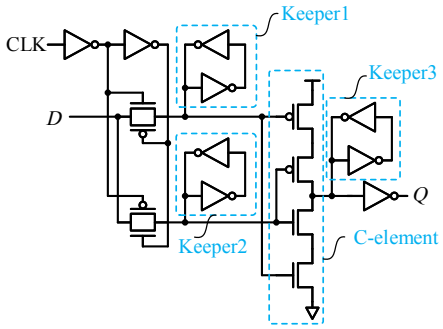


Fig. 5 Structure of DETFF LM_C.

consumption.

A DETFF LG_C based on the C-element proposed in Ref. [19] is shown in Fig. 6. LG_C contains internal latches LA and LB and an output C-element. The internal latches LA and LB are each composed of a C-element and a keeper, and the output stage is also composed of a C-element and a keeper. Unlike LM_C that also uses the C-element as the output stage, the two internal latches of LG_C are composed of the C-element instead of the transmission gate and keeper, which solves the problem where the internal nodes of the circuit generate redundant transitions with input glitches.

The working principle of LG_C is as follows: When the states of A and B are the same, the input D propagates to output Q. When the states of A and B are different, the output signal Q remains the previous state. When the input signal D is in the phase with the clock signal CLK at the same time, the state of A is DB (DB is the reverse of D), and B remains in the previous state. After the clock edge arrives, A is still in DB. At this time, the state of B is also DB, and the output Q will output D. The disadvantage of LG_C is that regardless of how the clock signal CLK and input signal D are inverted, the three keepers are in the working state, which increases the power consumption of the flip-flop. In addition, because LG_C uses the C-element, compared to the traditional latch, its circuit delay is too large.

A DETFF FN_C proposed in Ref. [19] is shown in Fig. 7, which can be used to solve the power consumption problem caused by the state changes of A and B with each clock edge. In the FN_C flip-flop, by introducing floating node F, the state of Q can be introduced into the internally cross-coupled weak C-element, then the states of A and B do not change after each clock transition, but if the level of A or B is maintained by the strong transistor input to the C-element, the other node remains floating. The level of the floating node will not change with the clock transition, which reduces the power consumption caused by the clock signal transition. At the same time, because the internal latch uses the C-element, FN_C can also block the glitch from the input signal to reduce redundancy transitions.

Compared with LG_C, FN_C has three disadvantages: First, the number of transistors used is larger. Second, the delay of FN_C is also relatively large because of the high number of stacked MOSFETs. Third, in FN_C, the floating nodes and feedback of internal node F increase the parasitic capacitance at nodes A and B, causing its voltage to exceed V_{dd} at the moment, which has an adverse effect.

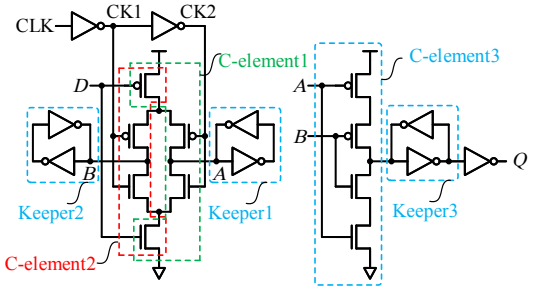


Fig. 6 Structure of DETFF LG_C.

2.3 Pulse-type DETFFs

The circuit shown in Fig. 8 is a pulse-type DETFF EP1, which was proposed in Ref. [21]. It consists of a pulse generator and a latch. The pulse generator is based on the exclusive OR logic of the transmission gate[7]. The rising and falling edges of the clock generate a sampling

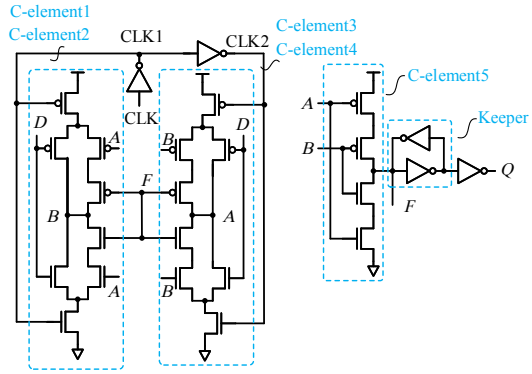


Fig. 7 Structure of DETFF FN_C.

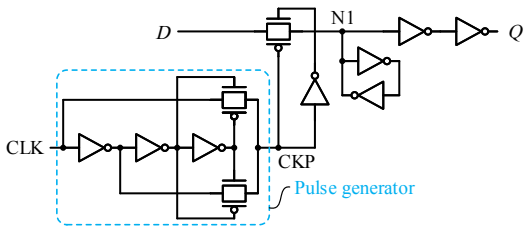


Fig. 8 Structure of DETFF EP1.

pulse. The latch collects data when the sampling pulse arrives, and it is in hold mode at other times.

Although the structure of EP1 is simple, it can also share explicit double-edge pulse generators, but it also increases the clock activity factor. Moreover, the clock tree circuit composed of pulse generators and the overall circuit power consumption are relatively large. In addition, two transmission gates of the pulse generator have a competitive relationship and will also increase the overall power consumption of the circuit.

The pulse-type DETFF EP2 proposed in Ref. [22] is shown in Fig. 9, and it includes a clock tree composed of four inverters, a pulse generator composed of six transistors, and a latch part.

EP2 also delays the clock signal CLK and then generates sampling pulses through the pulse generator so that the latch samples on each clock edge can achieve the function of double-edge triggering. The transistor size requirements are relatively large. The size of the two Positive MOSFETs (PMOSFETs) is much larger than the size of the two Negative MOSFETs (NMOSFETs), which will introduce a big power consumption.

3 Proposed DETFF

3.1 Circuit structure

First, we improved the traditional C-element to get the improved static C-element used in the structure of this paper, as shown in Fig. 10. We added the feedback loop of the C-element and made the improved C-element composed of a latch through the feedback loop. Such a structure can effectively latch the output state and maintain its static characteristics. At the same time, the additional transistor enhances the pull-up and pull-down capabilities of the C-element, which significantly reduces the data transmission delay[23].

Analyzing the advantages and disadvantages of the existing DETFFs, this paper proposes an anti-interference low-power DETFF based on the C-element, and its circuit structure is shown in Fig. 11. The DETFF includes the clock tree consisting of inverters INV1 and INV2, two internal latches LA and LB using the improved C-element, and output stages consisting of three C-elements. The clock tree circuit is used to generate the clock signal and inverted clock signal. Internal latches LA and LB latch the value of input signal D when the clock is high and the clock is low. The output stage outputs the value of D latched from the internal latch to Q.

3.2 Working principle

The working principle is shown in Fig. 12. Between the clock edges, when the input signal D changes, the output signal Q remains unchanged. Between the first falling edge and the first rising edge of CLK, LA keeps in the high-impedance state, the logic state is 1, and B is in state 1. At this time, the output Q is 1; D is flipped, A is flipped to state 0, B is kept in the high-impedance state, and the logic state is 1. Through the C-element, the output Q is still 1. When the input signal D remains

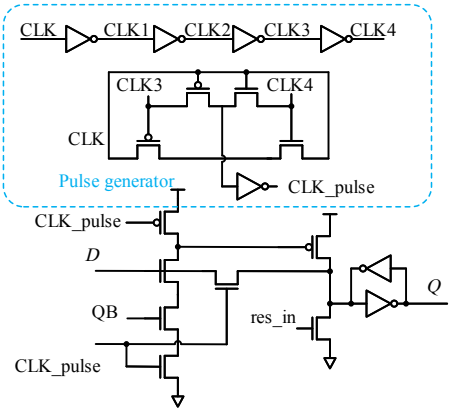


Fig. 9 Structure of DETFF EP2.

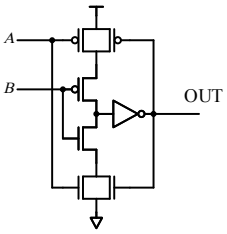


Fig. 10 Static C-element.

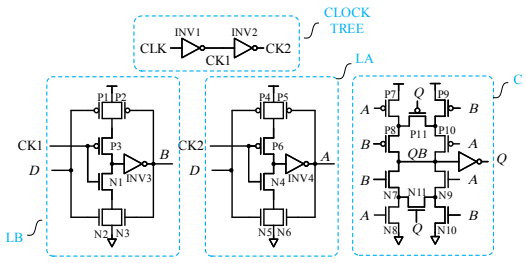


Fig. 11 Proposed DETFF.

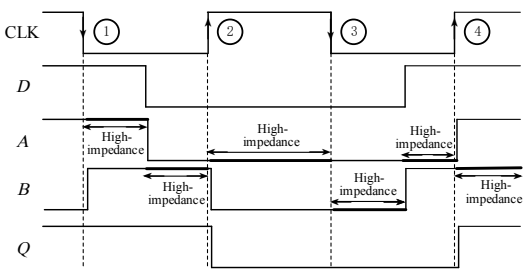


Fig. 12 Working principle waveform.

unchanged, the clock signal will not flip anyway, and the output signal Q will not flip. Before the second falling edge of CLK, D and B are 0, A is in the high-impedance state, the state is the previous 0, and the output Q is 0 at this time. After the second falling edge of CLK, D remains 0. At this time, A is 1, B is in a high-impedance state, and the state is the previous 0, so the output Q remains at 0. The output Q will only flip to D when the clock edge arrives and Q is different from D.

The state of either node A or B always remains D, and the remaining node will maintain the previous state. When the clock edge arrives, the node that is not in D will flip to D. At this time, A and B's state is the same as D, so the state of output Q will become D, which achieves the effect of triggering on both edges. Among them, the high-impedance state is the state that latch LA or LB is in the turn-off state, and it will not affect the static characteristics of the flip-flop, which is the effect achieved by the use of the improved C-element. At the same time, redundant transitions in the circuit are reduced and the power consumption of the circuit is reduced.

Table 1 is the truth table of internal nodes A and B and output Q. The hold in the Table 1 indicates that output state Q maintains the previous clock level, and the high-impedance state represents that the latch is in the turn-off state. The input signal D feeds latches LA and LB. Thus, whether the clock signal CLK is switched or not, at most, one of the output states of nodes A and B is in a high-impedance state. From the function of the C-element introduced earlier, we can know that an input signal in a high-impedance state does not affect the state of the output. At this time, the output of the C-element is held. Only when the output states of latches LA and LB are the same, the output of the DETFF Q is the same as the input signal D.

3.3 Working principle

This study simulated the proposed DETFF based on the HSPICE platform. The Predictive Technology Model (PTM) 32 nm process[24] is used. The power supply voltage is 0.9 V, the temperature is 25 °C, the clock frequency is 250 MHz, and the clock period is 4 ns.

Table 1 State truth table for nodes A, B, and Q.

A	B	Q
0	0	0
0	1	Hold
1	0	Hold
1	1	1
High impedance	1	Hold
High impedance	0	Hold
1	High impedance	Hold
0	High impedance	Hold

Figure 13 shows a waveform diagram obtained using the HSPICE simulation. In the figure, CLK is the clock signal, D is the input signal, A and B are the values outputted by latches LA and LB, and Q is the output signal. From the simulation waveform diagram, it can be seen that the DETFF proposed in this paper samples the value of the input signal D at the rising and falling edges of the clock and outputs it to the output signal Q, realizing the function of a double-edge triggering.

Figure 14 is a simulation waveform diagram when several glitches are generated on the input signal D due to interference. In Fig. 14, the simulation conditions and clock signal CLK are the same as those in Fig. 13, D is the input signal, and during the high and low levels of each clock, we inject two glitches. That is, there are

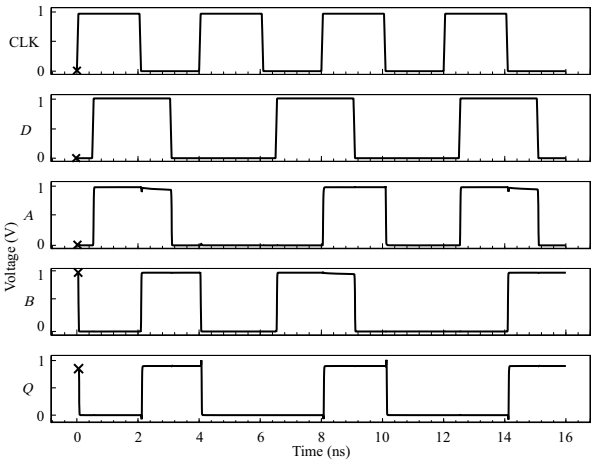


Fig. 13 Normal working simulation waveform.

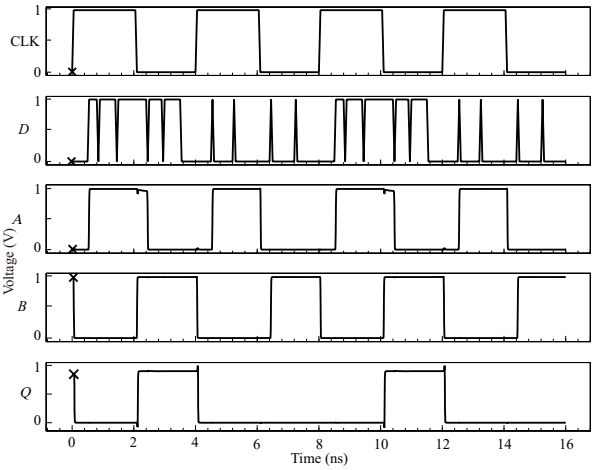


Fig. 14 Simulation waveform with glitches exist.

four glitches on the input signal D in each clock cycle. A and B are the values outputted by latches LA and LB, and Q is the output signal. The simulation waveform diagram shows that between the clock edges, regardless of how the input signal D is flipped, the output state of latch LA or LB is flipped at most once and will not be flipped multiple times. Thus, when there is a glitch in the input signal, it will not cause latches LA and LB to flip simultaneously. For example, between 6 and 8 ns, latch LB flips only once, whereas the state of latch LA remains unchanged.

This shows that the DETFF proposed in this paper can block the glitches caused by interference. The glitches existing in the input signal D will not be transmitted to the two internal nodes of A and B, and the redundant transitions of the internal nodes of the flip-flop will not be increased. Thus, it effectively reduces the probability of node inversion in the circuit and the frequency of transistor charging and discharging and achieves the purpose of reducing the circuit power consumption.

4 Experimental Result and Comparative Analysis

Based on the PTM 32 nm process, this study performed the HSPICE simulation on the relevant DETFF and obtained the experimental data results shown in Table 2. The power supply voltage Vdd=0.9 V, clock frequency CLK=250 MHz, and the temperature is 25 °C.

In Table 2, # T represents the number of transistors; TP represents the Total Power consumption of the circuit; t_{cq} represents the delay from the clock signal CLK to the output signal Q; PDP represents the Power Delay Product of the circuit, which is an important composite index; t_{setup} represents the setup time of the flip-flop; t_{hold} represents the hold time of the flip-flop; CTP represents the Clock Tree Power consumption of the circuit; G2 represents the total circuit power consumption when there are two glitches in a single clock cycle, and G4 represents the total power consumption with four glitches in a single clock cycle.

As shown in Table 2, the total power consumption of the circuits of LM2, EP1, and EP2 is relatively large. LM2 uses a transmission tube instead of a transmission gate and an inverter, and part of the clock signal is directly connected to the source of the transistor, causing a greater power consumption. The level conflict problem of LM2 is also one of the reasons for its excessive power consumption. EP1 and EP2 are both explicit pulse-type DETFFs, and some of the circuits of their pulse generator will introduce a large power consumption, causing the total power consumption of its circuit to be relatively large. Meanwhile, the total power consumption of the DETFF circuit proposed in this paper is the lowest among the 11 types of flip-flops.

In terms of circuit delay, the delays of LM1 and the Solid-State Power Controller (SSPC) are the smallest, whereas the delays of the C-element-type DETFFs, such as LG_C and IP_C, are larger. This is because the design uses C-element, and its driving current is small. Such a condition caused an excessively high delay. Although the DETFF proposed in this paper also uses a C-element, its delay is much lower than that of other C-element-type DETFFs, because it uses an improved static C-element. Having a feedback loop increases the pull-up and pull-down capabilities of the C-element. As a result, this feedback loop has a lower latency than a C-element with the same transistor size.

In terms of the PDP of the circuit, the PDP of the SSPC is the lowest, and the PDP of LM2 is the highest. The PDP of the DETFF proposed in this paper is the second lowest. However, the number of transistors used by the SSPC is 25% higher than that of the proposed flip-

Table 2 Comparison of the DETFF proposed in this paper with other DETFFs.

DETFF	# T	TP (μW)	t_{cq} (ps)	PDP ($\times 10^{-18}$J)	t_{setup} (ps)	t_{hold} (ps)	CTP (μW)	G2 (μW)	G4 (μW)
LM1[13]	26	1.75	37.14	65.18	13.20	28.39	1.14	2.22	2.67
LM2[13]	22	23.80	39.34	936.07	11.22	57.32	22.51	21.60	21.24
TCRFF[16]	22	1.52	80.97	123.34	54.22	45.52	0.81	2.11	2.69
LM_C[15]	26	1.22	72.20	88.11	36.50	66.84	0.23	1.59	1.97
LG_C[19]	28	1.44	84.04	120.66	16.11	167.00	0.26	1.85	2.19
IP_C[19]	26	1.39	77.65	107.65	25.08	148.59	0.29	1.39	1.39
FN_C[19]	30	1.18	74.28	87.28	15.59	101.43	0.32	1.36	1.53
EP1[21]	22	2.29	51.42	117.65	2.42	61.69	1.90	2.25	2.27
EP2[22]	25	3.35	46.42	155.59	18.11	56.42	3.16	3.34	3.34
SSPC[25]	40	1.21	37.28	45.28	30.39	292.58	0.27	1.65	2.09
Proposed	32	1.12	48.91	54.63	33.08	27.81	0.27	1.14	1.12

flop, so the proposed DETFF has a better comprehensive performance.

Because the clock load is large and some of the clock signals are directly connected to the source of the transistor, the power consumption of the clock tree of LM2 is excessively large. In EP1 and EP2, the clock tree formed by the pulse generator costs more and takes up more resources. Therefore, the clock tree power consumption is too large. The flip-flop proposed in this paper uses a C-element, which reduces the clock load and reduces the clock tree power consumption. The clock tree power consumption is thus acceptable.

When the input signal is affected by glitches, LM1 is greatly affected. When the glitches increase, the overall power consumption of the circuit will significantly increase because the input glitches will cause the internal latches to flip, resulting in the increase in power consumption to be relatively large in the data path. Because LG_C uses the C-element and blocks the data path between the input glitch and internal latch, it is not affected by the glitch, but LG_C uses three keepers. Moreover, regardless of how the clock signal and input signal change, these keepers will always be in the working state, resulting in a large power consumption. Because the DETFF proposed in this paper uses an improved C-element, the redundant transitions in the circuit are also reduced, resulting in a lower overall power consumption of the circuit. As shown in Table 2, the power consumptions in the case of G2 and G4 are also the smallest. As the input glitch increases, the power consumption of the proposed DETFF will also be lower than those of other types of DETFFs. Thus, even in the presence of more glitches in the input signal, the DETFF proposed in this paper will have a lower clock tree power consumption and total power consumption.

For the convenience of a visual observation, Table 3 lists the relative total power consumption ΔTP, relative delay overhead Δt_{cq}, and relative PDP overhead ΔPDP of the proposed DETFF and comparison flip-flops, where $\Delta = 100\% \times$ ((Contrast DETFF−the proposed DETFF)/Contrast DETFF). If Δ is positive, this indicator is better than the contrast structure; if Δ is negative, the DETFF proposed in this paper is inferior to the comparative structure. As shown in Table 3, the flip-flop proposed in this paper is superior to all the comparative DETFFs in terms of the total circuit power consumption, saving an average of 251.17% of the total power consumption. Moreover, it improved the average PDP by 44.32% and the delay by 9.71%.

Table 3 Comparison of the relative cost. (%)

DETFF	ΔTP	Δt_{cq}	ΔPDP
LM1[13]	36.18	31.68	16.19
LM2[13]	2267.70	24.34	94.16
TCRFF[16]	26.48	39.59	55.71
LM_C[15]	10.03	32.26	38.00
LG_C[19]	21.99	41.80	54.72
IP_C[19]	19.22	37.01	49.25
FN_C[19]	4.68	34.15	37.41
EP1[21]	51.05	4.88	53.56
EP2[22]	66.58	5.36	64.89
SSPC[25]	7.80	31.21	20.65
Average	251.17	9.71	44.32

We use the same method to compare the total power consumption of the circuit when each DETFF generates glitches on the interfered input signal. The total relative circuit power consumption ΔG2 with two glitches in one clock cycle and ΔG4 with four glitches in one clock cycle are compared, where Δ and the comparison method are the same as described above. The comparison result is shown in Table 4, which also shows the proposed DETFF in the presence of glitches in the input signal. The total power consumption of the circuit is better than those all of the comparative flip-flops, with an average increase of 43.62% and 51.28%, respectively.

In summary, compared with contrast DETFFs, the DETFF proposed in this paper has achieved greater advantages in terms of total power consumption, delay, PDP, and total power consumption with glitches in the input signal.

5 Variance Analysis

With the development of integrated circuit technology and continuous progress in technology, the impact of

Table 4 Comparison of the relative cost of glitches caused by interference. (%)

DETFF	ΔG2	ΔG4
LM1[13]	48.71	58.02
LM2[13]	94.72	94.73
TCRFF[16]	45.86	58.41
LM_C[15]	28.23	43.05
LG_C[19]	38.45	48.95
IP_C[19]	17.95	19.57
FN_C[19]	16.46	26.65
EP1[21]	49.23	50.65
EP2[22]	65.87	66.42
SSPC[25]	30.71	46.38
Average	43.62	51.28

Process, Voltage, and Temperature (PVT) and Negative Bias Temperature Instability (NBTI)-induced aging variations on the reliability of nanoscale integrated circuits has become increasingly serious[26]. This section evaluates the power consumption and delay performance of the DETFF described above under PVT and NBTI-induced aging variations.

We take the gate length as a relative variable, changing from 32 to 42 nm with a step size of 1 nm. The power consumption and delay variations of DETFFs are obtained as shown in Figs. 15 and 16. Particularly, because LM2 power consumption is larger than other DETFFs, it uses the secondary axis on the right side. With the increase in gate length, the power consumption of the circuit shows a downward trend, whereas the delay is steadily rising.

LM_C, LG_C, IP_C, and other three C-element-type DETFFs gradually fail to work as the gate length increases, indicating that they are very sensitive to process variations. Moreover, the DETFF proposed in this paper can work normally under process variations, showing good robustness.

In Figs. 17 and 18, the voltage is increased from 0.75

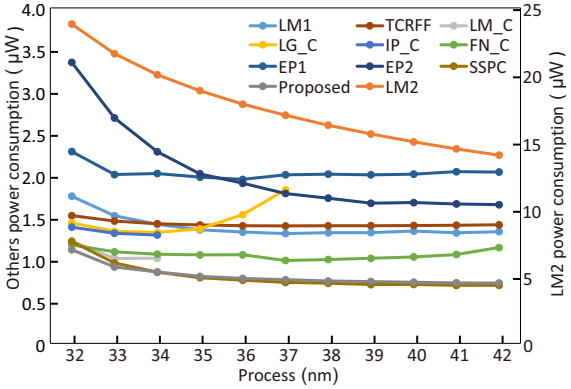


Fig. 15 Effect of process variations on the power consumption of DETTF.

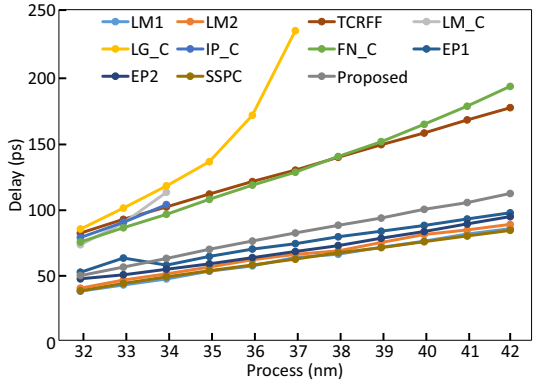


Fig. 16 Effect of process variations on the delay of DETFF.

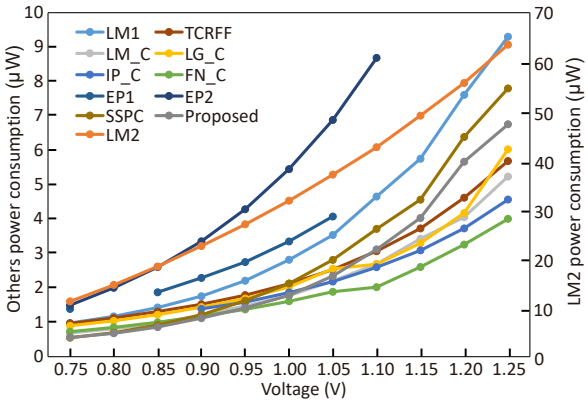


Fig. 17 Effect of voltage variations on the power consumption of DETFF.

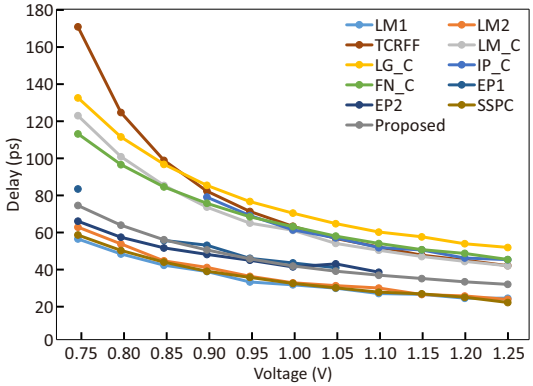


Fig. 18 Effect of voltage variations on the delay of DETFF.

to 1.25 V, with a step size of 0.05 V. Because LM2 power consumption is larger than those of other DETFFs, it uses the secondary axis on the right side of Fig. 17. As shown in Fig. 17, the power consumption of the circuit increases with the voltage. The power consumption is proportional to the square of the voltage. In Fig. 18, the circuit delay continues to decrease as the voltage increases because the larger the supply voltage, the faster the conduction current, and the smaller the delay.

Furthermore, IP_C does not properly work at low voltages, such as 0.75 V, 0.8 V, and 0.85 V, whereas EP1 and EP2 do not work properly at high voltages, such as 1.15 V, 1.2 V, and 1.25 V. The DETFF proposed in this paper can normally work under the voltage fluctuation of 0.75–1.25 V and is not sensitive to its variations.

The effects of temperature variations on the performance of DETFFs are shown in Figs. 19 and 20, where the temperature is from −25 to 75 °C with size steps of 10 °C. Particularly, because LM2 power consumption is larger than those of other DETFFs, it uses the secondary axis on the right side of Fig. 19. Figure 19 also shows that the power consumption

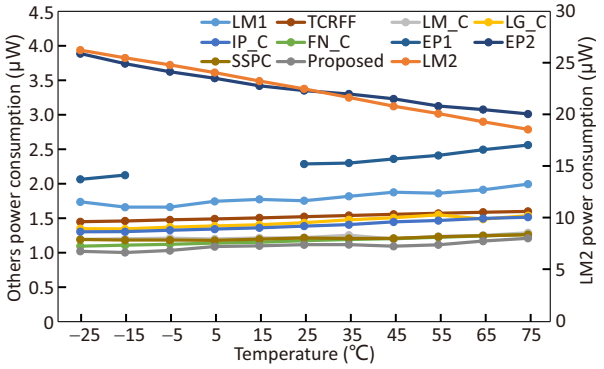


Fig. 19 Effect of temperature variations on the power consumption of DETFF.

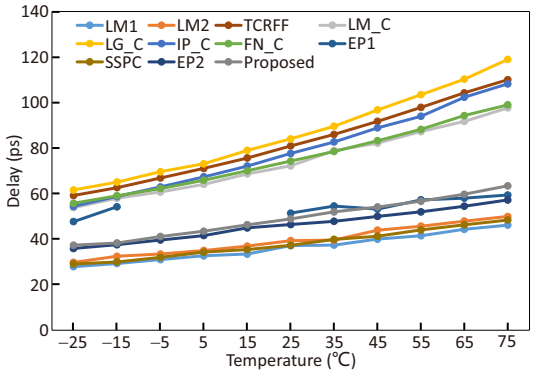


Fig. 20 Effect of temperature variations on the delay of DTEFF.

and delay of the DETFFs gradually increase with the temperature. As the temperature increases, the mobility of the carriers in the drain-source current of a transistor is continuously decreasing, resulting in a decrease in its performance and increases in its power consumption and delay.

Similarly, EP1 does not properly work at −5 °C, 5 °C, and 15 °C, and it is more sensitive to temperature variations. Because it is an explicit pulse-type DETFF, when temperature varies, the performance of the transistor will also change, resulting in the inability to generate a normal pulse signal. The DETFF proposed in this paper is not sensitive to temperature variations and can work normally from −25 °C to 75 °C.

We use the reliability analysis in HSPICE to simulate the aging situation caused by the NBTI. The set aging time is 3×10^8 s, which is approximately equal to 9.5 years. Then, we obtained the experimental data results shown in Table 5. The basic environment settings of the simulation are the same as those presented in Table 2.

In Table 5, Reltotaltime represents the time of aging simulation, Aging TP represents the total power consumption after aging simulation, and Aging t_{cq} represents the delay from the clock signal CLK to the output signal Q after the aging simulation. The decrease of TP and the increase of t_{cq} represent the corresponding reduction and percentage increase of the power consumption and delay after the aging simulation, respectively.

Table 5 shows that almost all the DETFFs have reduced the total power consumption of the circuit after approximately 9.5 years of aging simulation, except for LG_C that has increased. Furthermore, all DETFFs have increased the delay significantly. LG_C has the largest increase, reaching 113.74%, whereas EP1 has the least increased delay, only increasing by 15.50%. Meanwhile, IP_C failed the test in the aging simulation and cannot work normally. The DETFF proposed in this paper performed well in the aging simulation, reaching an average level.

6 Conclusion

To effectively reduce the power consumption of DETFFs, this paper presents an anti-interference low-power DETFF based on a C-element. We use an improved static C-element to reduce the clock load and power

Table 5 Aging performance comparison of the DETFF proposed in this paper with other DETFFs.

DETFF	Reltotaltime (year)	TP (μW)	t_{cq} (ps)	Aging TP (μW)	Aging t_{cq} (ps)	TP reduce (%)	t_{cq} increase (%)
LM1[13]	9.5	1.75	37.14	1.41	48.93	–19.87	31.73
LM2[13]	9.5	23.80	39.34	21.83	52.01	–8.28	32.21
TCRFF[16]	9.5	1.52	80.97	1.36	113.87	–10.92	40.64
LM_C[15]	9.5	1.22	72.20	0.98	104.57	–19.48	44.83
LG_C[19]	9.5	1.44	84.04	1.71	179.63	19.13	113.74
IP_C[19]	9.5	1.39	77.65	Fail	Fail	Fail	Fail
FN_C[19]	9.5	1.18	74.28	1.06	103.40	–9.98	39.21
EP1[21]	9.5	2.29	51.42	1.96	59.39	–14.30	15.50
EP2[22]	9.5	3.35	46.42	1.81	63.23	–46.05	36.22
SSPC[25]	9.5	1.21	37.28	0.79	50.28	–35.21	34.88
Proposed	9.5	1.12	48.91	0.91	64.67	–18.64	32.23

consumption of the clock tree. The use of C-elements can effectively reduce the redundant transitions of the internal nodes of the circuit and further reduce the overall power consumption. Compared with previous DETFFs, the proposed DETFF in this paper has great advantages in terms of total power consumption, clock tree power consumption, PDP, and anti-interference glitch-blocking capabilities, which has a good comprehensive performance. The detailed variation analysis shows that it is not sensitive to variations, such as PVT. Moreover, it can achieve a better performance in the aging simulation and has high reliability.

Acknowledgment

This work was supported in part by the National Natural Science Foundation of China (Nos. 61874156, 61874157, 61904001, and 61904047).

References

[1] B. Yang, Z. Yu, and J. Wei, Design of low-power modern radar SoC based on ASIX, *Tsinghua Science and Technology*, vol. 19, no. 2, pp. 168–173, 2014.

[2] S. Hu, W. Ji, and Y. Wang, Feedback cache mechanism for dynamically reconfigurable VLIW processors, *Tsinghua Science and Technology*, vol. 22, no. 3, pp. 303–316, 2017.

[3] P. Zhao, T. Darwish, and M. Bayoumi, High-performance and low power conditional discharge flip-flop, *IEEE Transactions on Very Large Scale Integration Systems*, vol. 12, no. 5, pp. 477–484, 2004.

[4] B. Kong, S. Kim, and Y. Jun, Conditional-capture flip-flop for statistical power reduction, *IEEE Journal of Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, 2001.

[5] H. Kawaguchi and T. Sakurai, A reduced clock-swing flip-flop (RCSFF) for 63% power reduction, *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, 1998.

[6] Y. Dai and J. shen, An explicit-pulsed double-edge triggered JK flip-flop, in *Proc. of 2009 International Conference on Wireless Communication & Signal Processing*, Nanjing, China, 2009, pp. 1–4.

[7] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcenas, and W. Kuang, Low-power clock branch sharing double-edge triggered flip-flop, *IEEE Transactions on Very Large Scale Integration Systems*, vol. 15, no. 3, pp. 338–345, 2007.

[8] C. Kim and S.-M. Kang, A low-swing clock double-edge triggered flip-flop, *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 648–652, 2002.

[9] S. C. Tiwari, K. Singh, and M. Gupta, A low power high density double edge triggered flip flop for low voltage systems, in *Proc. of International Conference on Advances in Recent Technologies in Communication and Computing*, Kottayam, India, 2010, pp. 377–380.

[10] N. Nedovic and V. G. Oklobdzija, Dual-edge triggered storage elements and clocking strategy for low-power systems, *IEEE Transaction on VLSI Systems*, vol. 13, no. 5, pp. 577–590, 2005.

[11] C. C. Yu, Low-power double edge-triggered flip-flop circuit design, in *Proc. of 3rd Innovative Computing Information and Control International Conference*, Washington, DC, USA, 2008, p. 566.

[12] S. Kim, J. Kim, and S. Y. Hwang, New path balancing algorithm for glitch power reduction, *IEEE Proceedings–Circuits, Devices and Systems*, vol. 148, no. 3, pp. 151–156, 2001.

[13] M. Pedram, Q. Wu, and X. Wu, A new design of double edge triggered flip-flops, in *Proc. of Asian and South Pacific Design Automation Conference*, Yokohama, Japan, 1998, pp. 417–421.

[14] A. Khan, D. Shaikh, and M. T. Beg, 2 GHz low power double edge triggered flip-flop in 65 nm CMOS technology, in *Proc. 2012 IEEE International Conference on Signal Processing, Computing and Control*, Waknaghat Solan, India, 2012, pp. 1–5.

[15] S. V. Devarapalli, P. Zarkesh-Ha, and S. C. Suddarth, A robust and low power dual data rate (DDR) flip-flop using C-elements, in *Proc. of 11th International Symposium on Quality Electronic Design* (*ISQED*), San Jose, CA, USA, 2010, pp. 147–150.

[16] N. A. Sabu and K. Batri, Design and analysis of power efficient TG based dual edge triggered flip-flops with stacking technique, *Journal of Circuits, Systems and Computers*, vol. 29, no. 8, p. 2050123, 2020.

[17] Y. Ye, S. Borkar, and V. De, A new technique for standby leakage reduction in high-performance circuits, in *Symposium on VLSl Circuits Digest of Technical Papers*, Honolulu, HI, USA, 1998, p. 98CH36215.

[18] D. E. Muller and W. S. Bartky, A theory of asynchro-nous circuits, in *Proceedings of International Symposium on the Theory of Switching*. Cambridge, MA, USA: Harvard University Press, 1959, pp. 204–243.

[19] S. Lapshev and S. M. R. Hasan, New low glitch and low power DET flip-flops using multiple C-elements, *IEEE Transactions on Circuits & Systems I Regular Papers*, vol. 63, no. 10, pp. 1673–1681, 2016.

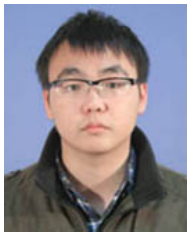
[20] M. Shams, J. C. Ebergen, and M. I. Elmasry, Modeling and comparing CMOS implementations of the C-element, *IEEE Transactions on Very Large Scale Integration Systems*, vol. 6, no. 4, pp. 563–567, 1998.

[21] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors, in *Proc. of International Symposium on Low Power Electronics and Design*, Huntington Beach, CA, USA, 2001, pp. 147–152.

[22] R. Shandilya and R. K. Sharma, High speed low power dual-edge triggered D flip-flop, in *Proc. of 2017 International Conference on Intelligent Computing and Control* (*I2C2*), Coimbatore, India, 2017, pp. 1–5.

[23] I. C. Wey, B. C. Wu, C. C. Peng, C. S. A. Gong, and C. H. Yu, Robust C-element design for soft-error mitigation, *IEICE Electronics Express*, vol. 12, no. 10, p. 20150268, 2015.
[24] Predictive Technology Model (PTM) for SPICE, http://ptm.asu.edu/.
[25] Yongmin Lee and Yoonmyung Lee, A PVT variation-tolerant static single-phase clocked dual-edge triggered flip-flop for aggressive voltage scaling, *IEICE Electronics Express*, vol. 16, no. 20, p. 20190528, 2019.
[26] Y. Zhang, M. Khayatzade, K. Yang, M. Saligane, N. Pinckney, M. Alioto, D. Blaauw, and D. Sylvester, iRazor: Current-based error detection and correction scheme for PVT variation in 40-nm ARM Cortex-R4 Processor, *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 619–631, 2018.

Zhengfeng Huang received the PhD degree in computer engineering from Hefei University of Technology in 2009. He joined Hefei University of Technology as an assistant professor in 2004 and has been an associate professor since 2010. He has been a professor since 2018. His current main research interest is the design for soft error tolerance/mitigation. He is a member of Technical Committee on Fault Tolerant Computing which belongs to China Computer Federation. He worked as a visiting scholar at the University of Paderborn, Germany from 2014 to 2015. He served on the organizing committee of the IEEE European Test Symposium in 2014.



Xiao Yang received the BS degree from Hefei University of Technology in 2018. Currently, he is pursuing the master degree in integrated circuit engineering at Hefei University of Technology. His research interests include radiation hardening by design and low power digital circuit design.

Tai Song received the MEng degree in electrical engineering from Xinjiang University, China in 2010. He is now a PhD candidate at Hefei University of Technology. His current research interests include IC test, machine learning algorithm, and adaptive test.

Haochen Qi received the BEng degree in industrial automation from Anhui University of Technology, China in 2003 and MEng degree in integrated circuit engineering from Hefei University of Technology, China in 2009. She is now a PhD candidate at Hefei University of Technology, China. Her research interests include IC test, quality control in semiconductor process, and biosensors.

Yiming Ouyang received the BEng, MEng, and PhD degrees from Hefei University of Technology in 1984, 1991, and 2013, respectively. He is currently a professor at Hefei University of Technology and a leading expert in research. His research interests include NoC and Systems on-Chip (SoC), integration and testing of embedded systems, and automation of digital system design.

Tianming Ni received the PhD degree from Hefei University of Technology, Hefei, China in 2018. He joined the Key Laboratory of Advanced Perception and Intelligent Control of High-end Equipment, and School of Electrical Engineering, Anhui Polytechnic University in 2018. His research interests include built-in-self-test, design automation of digital systems, design for IC reliability, and 3D IC test and fault tolerance.

Qi Xu received the BEng degree in microelectronics from Anhui University, Hefei, China in 2012 and the PhD degree in electronic science and technology from University of Science and Technology of China, Hefei in 2018. He is currently a lecturer at the School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei. His research interests include physical design automation and design for reliability for 3D integrated circuits.