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A 12-bit 250-MS/s Charge-Domain Pipelined Analog-to-Digital Converter with Feed-Forward Common-Mode Charge Control

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Abstract: A feed-forward Common-Mode (CM) charge control circuit for a high-speed Charge-Domain (CD) pipelined Analog-to-Digital Converter (ADC) is presented herein. This study aims at solving the problem whereby the precision of CD pipelined ADCs is restricted by the variation in input CM charge, which can compensate for CM charge errors caused by a variation in CM charge input in real time. Based on the feed-forward CM charge control circuit, a 12-bit 250-MS/s CD pipelined ADC is designed and realized using a 1P6M 0.18-μm CMOS process. The ADC achieved a Spurious Free Dynamic Range (SFDR) of 78.1 dB and a Signal-to-Noise-and-Distortion Ratio (SNDR) of 64.6 dB for a 20.1-MHz input; a SFDR of 74.9 dB and SNDR of 62.0 dB were achieved for a 239.9-MHz input at full sampling rate. The variation in signal-to-noise ratio was less than 3 dB over a 0–1.2 V input CM voltage range. The power consumption of the prototype ADC is only 85 mW at 1.8 V supply, and it occupies an active die area of 2.24 mm^2.

Key words: pipelined analog-to-digital converter; charge domain; low power; feed-forward control

1 Introduction

Pipelined Analog-to-Digital Converters (ADCs) are widely used in wireless communication fields that require high sampling rates and high resolution[1]. The performance of reported pipelined ADCs has been continuously improved owing to the rapid development of CMOS technology and design methodology over the past decades. Pipeline ADCs based on conventional Switched-Capacitor (SC) circuitry have achieved a resolution of up to 14 bits with sampling rate of over 500 MSPS[2,3]. However, pipeline ADCs consume high power because of their reliance on the high gain-bandwidth operational amplifier (op-amps). Digital calibration assisted SC circuitry is used as a good solution to significantly alleviate the power consumption in the design of high-speed and high-resolution pipelined ADCs[4]. However, its calibration algorithms are complex and consume considerable chip area and power. Other novel attempts at power consumption reduction include using a pipelined SAR structure as an effective way to minimize the number of op-amps in the design of pipeline ADCs[5,6]. Dynamic source follower, zero crossing, or virtual ground reference buffer-based SC pipelined ADCs[7−9] are also effective solutions that eliminate op-amps to achieve low power consumption. However, compared with digital calibration-assisted SC circuitry, these solutions are not mature enough for the design of high-speed and high-resolution pipelined ADCs.

The Charge-Domain (CD) pipelined ADC based on Boosted Charge Transfer (BCT) is a new architecture that achieves high speed and consumes very low power in commercial CMOS processes[10]. However, the charge transfer process of the BCT circuit may be seriously influenced by Process Voltage Temperature

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(PVT) variations and Common-Mode (CM) charge errors. The CD pipeline ADC reported in Ref. [10] adopts power-on calibration and complicated CM control techniques to ensure design precision. However, power-on calibration cannot calibrate the deviations caused by the power supply and temperature variations in real time. The pseudo-differential-assisted and replica-controlled PVT insensitive BCT circuit reported in Refs. [11–14] effectively calibrates the CM charge deviations caused by PVT variations. However, these BCT circuits only control the CM charge errors introduced during the charge transfer process; the input CM charge error from outside the ADC cannot be either processed or controlled. As no op-amp is used at the front end of the CD pipelined ADC, variations in input CM charge will directly cause a CM charge error and restrict the precision of CD pipelined ADCs.

In this study, a feed-forward CM charge control circuit is proposed to eliminate the variations in input CM charge caused by fluctuations from outside the ADC. This circuit can compensate for CM charge errors caused by the variations in CM charge input in real time. Based on the feed-forward CM charge control circuit, a low power 12-bit 250-MS/s CD pipelined ADC was designed and tested after fabrication.

2 CM Analysis of CD Pipelined ADC Sub-stage

The structure of a typical BCT-based CD pipelined stage is shown in Fig. 1a[11,12]. It comprised a charge storage node Xn, two charge storage capacitors C_c and C_s, a sub-ADC, a sub digital-to-analog converter (sub-DAC), a charge transfer circuit St, and a reset switch Sr. Figure 1b illustrates the operation waveform. At t0, Q_i begins to transfer into Xn and the voltage of Xn ($V_{Xn}(0)$) drops gradually. At t1, the charge transfer of Q_i is completed; assuming no charge leakage, the voltage of Xn remains constant and the sub-ADC generates the quantization results $D(n)$. At t2, $D(n)$ is passed to the sub-DAC of this stage to generate voltage V_{dac} for charge subtraction. V_{dac} is then connected to C_s and results in the residue charge Q_{out}. At t3, St is open and Q_{out} will be transferred to the next pipelined stage. At t4, St is closed, charge transfer process is completed, and the voltage of Xn ($V_{Xn}(4)$) is kept constant. At t5, Sr resets Xn to $V_{Xn}(0)$. At t6, after the resetting of Xn is completed, the whole clock period for CD pipelined stage is finished.

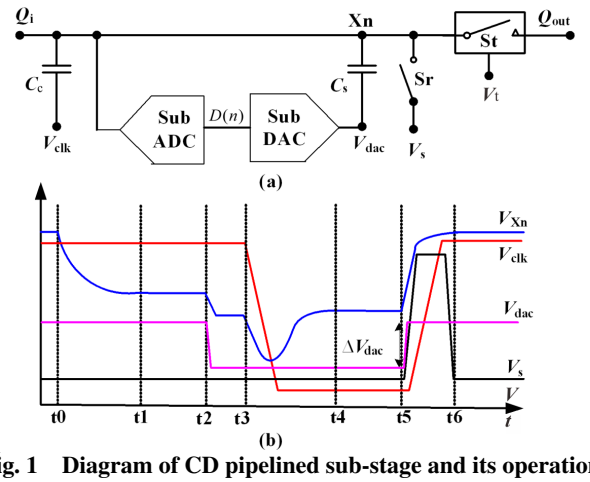


Fig. 1 Diagram of CD pipelined sub-stage and its operation waveform.

The charge relation of the circuit in Fig. 1a is

$$Q_{out} = Q_i + C_s \cdot \Delta V_{dac} + (C_c + C_s) \cdot (V_{Xn}(0) - V_{Xn}(4)) + C_c \cdot (V_c(4) - V_c(0)) = Q_i + C_s \cdot \Delta V_{dac} + Q_c \quad (1)$$

where $Q_c = (C_c + C_s) \cdot (V_{Xn}(0) - V_{Xn}(4)) + C_c \cdot (V_c(4) - V_c(0))$ is a constant that has no relation with Q_i. When Fig. 1a is implemented in fully differential form, the output CM charge of the CD pipelined stage is

$$Q_{cmout} = (Q_i + C_s \cdot \Delta V_{dac} + 2Q_c + 2Q_{icm} - Q_i + C_s \cdot (V_{Fdac} - \Delta V_{dac}))/2 = Q_{icm} + C_s \cdot V_{Fdac}/2 + Q_c \quad (2)$$

where V_{Fdac} is the full output range of sub-DAC and Q_{icm} is the input CM charge. Equation (2) shows that the output CM charge comprised three parts, namely, the input CM charge, the sub-DAC incremental charge $C_s \cdot V_{Fdac}/2$, and the constant charge Q_c introduced during the charge transfer process.

Ideally, the output CM charge Q_{cmout} of all sub-stages in the CD pipelined ADC should be kept constant; however, owing to the PVT variation, the CM charge Q_{cmout} fluctuates and extensively reduces the input signal range of the ADC. Assuming that the sub-stage shown in Fig. 1 is the N-th stage of a CD pipelined ADC, the CM charge can then be rewritten as

$$\begin{aligned} &Q_{cmout}(N) = Q_{icm}(N-1) + C_s \cdot \Delta V_{Fdac}/2(N) + Q_c(N) = \\ &Q_{icm}(N-1) + Q_{dac}(N) + Q_c(N) = \\ &Q_{icm}(N-2) + Q_{dac}(N-1) + Q_c(N-1) + Q_{dac}(N) + \\ &Q_c(N) = Q_{cmout}(SH) + Q_{dac}(1) + Q_c(1) + \cdots + \\ &Q_{dac}(N-1) + Q_c(N-1) + Q_{dac}(N) + Q_c(N) = \\ &Q_{icm} + Q_c(SH) + Q_{dac}(1) + Q_c(1) + \cdots + \\ &Q_{dac}(N-1) + Q_c(N-1) + Q_{dac}(N) + Q_c(N) \end{aligned} \quad (3)$$

where $Q_{cmout}(SH)$ is the CM output of the sample and holds (SH) circuit of the CD pipelined ADC, Q_{icm} is

the CM charge corresponding to the analog input CM voltage before the SH, and Q_c(SH) is the constant charge introduced by the charge transfer process from the SH circuit to first stage of the CD pipelined ADC.

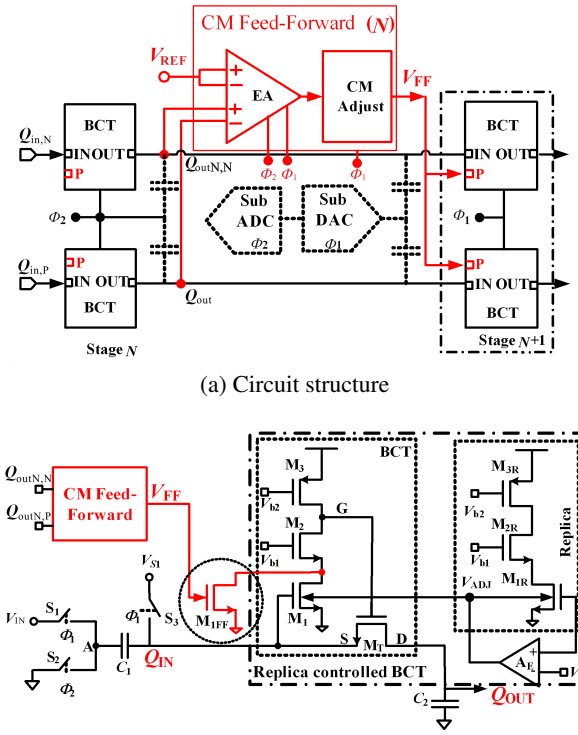
As C_s is constant and V_{Fdac} is provided by the voltage reference of sub-DAC, the variation in Q_{dac} in all sub-stages can be ignored. The PVT insensitive BCT circuit reported in Refs. [11–14] can be used to accurately control the variation in CM charge caused by the variation in Q_c in the SH circuit and the $N-1$ CD pipelined sub-stages. Q_{icm} is determined by the analog input CM voltage and the sampling capacitors. Op-amps with very good CM rejection ratios, which must be used in the SC circuitry, are eliminated from the SH circuit. The CM rejection ability of the input front end in the CD pipelined ADC is very poor. To control the variation in Q_{icm} and improve the resolution of CD pipelined ADCs, a feed-forward CM charge control circuit is proposed in this study.

3 Feed-Forward CM Charge Control Circuit

3.1 Circuit structure

The circuit structure of the proposed feed-forward CM charge control circuit used in N-th stage of the CD pipelined ADC is shown in Fig. 2a. When a variation in CM output charge from the BCT circuit in the N-th stage circuitry is detected, it is compensated in real time in the BCT circuit in (N+1)-th stage circuitry using the feed-forward CM charge control circuit. A dynamic compensation relation is formed by the variation in CM charge between the BCT circuits in the two connective stage circuits. The feed-forward CM charge control circuit comprised an Error Amplifier (EA), and CM adjusts the circuit. EA is used to detect the variation in CM output voltage of the (N-th) stage circuitry and compare it with the reference voltage to get the input CM error. Then, the CM adjust circuit generates the control voltage V_{FF} according to the input CM error. V_{FF} is used to change the bias condition of the BCT circuit in the (N+1)-th stage circuit and compensate for the CM charge error caused by the variation in input CM voltage.

The control scheme of the feed-forward CM charge control circuit to the replica-controlled BCT circuit is shown in Fig. 2b. The status of charge transfer in the BCT circuit is changed by the newly added NMOS M_{1FF}, which is controlled by V_{FF}. In BCT circuits, the



(a) Circuit structure

(b) Control scheme in BCT

Fig. 2 Circuit structure of the feed-forward circuit and its control scheme in BCT.

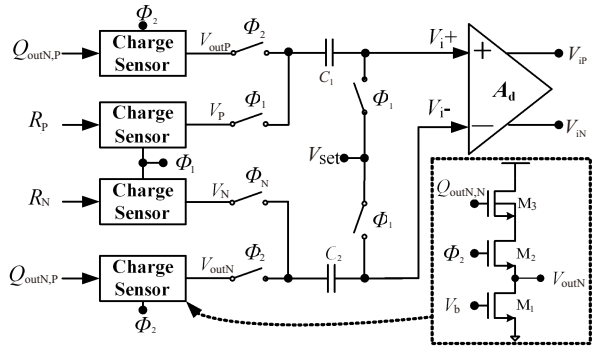
status of the charge transfer MOSFET M_T is determined by its gate voltage V_G during the period t3–t4 in Fig. 1b. V_G is determined by the quiescent operating point of the cascade amplifier comprised of M_1, M_2, and M_3. When the BCT circuit closes, the equivalent resistance of M_1 will change according to the fluctuations in the input CM charge; this leads to a variation in V_G and generates charge transfer error. When the newly added NMOS M_{1FF} is introduced, V_G is determined by the quiescent operating points of M_{1FF}, M_1, M_2, and M_3. Assuming that an input CM charge error introduced in the BCT causes a reduction in the equivalent resistance of M_1 and V_{FF} controls increase the equivalent resistance of M_{1FF} accordingly, the parallel equivalent resistance of M_1 and M_{1FF} can still be constant. V_G remains constant because M_1 and M_{1FF} are constant. In this way, the CM charge error caused by the variation in input CM voltage can be compensated in real time.

Two vital parts must be accurately handled in the feed-forward CM charge control circuit, as illustrated in Fig. 2b. First, the input CM charge error should be precisely measured. Second, the CM error should be precisely compensated to keep the parallel equivalent resistances of M_1 and M_{1FF} constant. A CM voltage

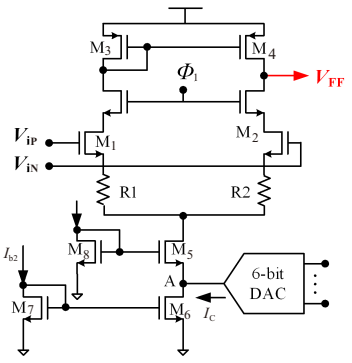
insensitive differential detect and amplify circuit is used to measure the input CM charge error in this design. In addition, the CM adjust circuit is implemented in a programmable form to achieve precise compensation; the CM adjust circuit can adjust the coefficient of feed-forward compensation in the application environment.

3.2 Circuit implementation

If a traditional voltage sampling switch is used and no isolation is introduced to sample the charge signal, the input charge signals $Q_{\text{outN,P}}$ and $Q_{\text{outN,N}}$ are coupled to C_1 and C_2, respectively; these charge signals introduce a charge detection error. To avoid this, charge sensors are used to isolate the charge package signal from the input sampling capacitors C_1 and C_2. Figure 3a shows the error detection and amplification circuit; the circuit comprised four charge sensors, a CM voltage insensitive high-speed SC differential voltage sampling network, and a fully differential amplifier with the gain of A_d. The charge sensor is shown in the dashed box. It is a clock-controlled source follower. M_3 can be implemented using a low-V_{th} transistor to reduce the voltage drop of the source follower. A fully differential amplifier can be realized by traditional differential amplifier that has been used.



(a) Error detect and amplify circuit



(b) Programmable CM adjust circuit

Fig. 3 Circuit implementation of the feed-forward circuit.

Figure 3b shows the circuit structure of the programmable CM adjust circuit; the circuit comprised a PMOS current mirror, differential input pair, bias circuit, and 6-bit programmable DAC. The transconductance of the CM adjust circuit is controlled by the current relation between I_c, I_{b1}, and I_{b2}, where I_c is controlled by the 6-bit current DAC. The MOSFET, M_1 and M_2, used in the differential input pair is biased and worked in the linear region. Assuming R1=R2=Rs, we can get the transconductance of the CM adjust circuit as

$$G_m = \frac{G_{m2}}{1 + G_{m2} \cdot \text{Rs}} = \frac{1}{\frac{1}{G_{m2}} + \text{Rs}} = \frac{1}{\frac{2 \cdot u_n \cdot C_{ox} \cdot (W/L)}{I_{b1} + I_c} + \text{Rs}} \quad (4)$$

where G_{m2} is the transconductance of the CM adjust circuit without R1 and R2. It can be seen from Eq. (4) that the transconductance of the CM adjust circuit can be precisely adjusted by R1, R2, and I_c. In practical application, the 6-bit current DAC that controls I_c is adjusted by the SPI port when the ADC is in test mode, so that compensation for the input CM charge error can be optimized.

4 12-bit 250 MS/s CD Pipelined ADC

A block diagram of the 12-bit CD pipelined ADC based on the proposed feed-forward CM charge control circuit is shown in Fig. 4. The 12-bit CD pipelined ADC comprised a high-speed low-distortion SH circuit, two 2.5-bit CD sub-stages, five consecutive 1.5-bit CD sub-stages, and a final 3-bit flash. The input differential analog voltage signals, V_{iN} and V_{iP}, are first sampled and converted into charge package signals, Q_{iN} and Q_{iP}, by sample and hold (S&H), respectively. Q_{iN} and Q_{iP} are then processed stage by stage via eight CD sub-stages and the final flash ADC. Finally, digital correction logic obtains the 19-bit quantization output from all the sub-stages and generates the final 12-bit output code. Two feed-forward CM charge control

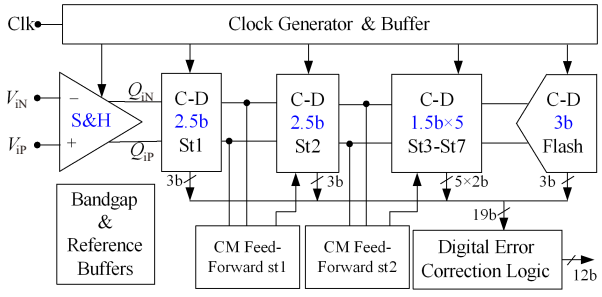


Fig. 4 Block diagram of the 12-bit CD ADC.

circuits, which are controlled by non-overlapping two clock phases, are used in the 12-bit CD pipelined ADC. The first stage feed-forward CM charge control circuit (st1) is used between the first and second CD pipelined sub-stages, and the second (st2) is used between the second and third CD pipelined sub-stages. As the influence of the input error to the pipelined stage is relaxed stage by stage, the fourth pipelined stage does not require the feed-forward CM charge control circuit.

5 Experimental Results

The prototype 12-bit CD pipelined ADC based on the proposed feed-forward CM charge control circuit was fabricated using a 1.8-V IP6M 180-nm CMOS process. The die photograph is shown in Fig. 5. The central part comprises the SH circuit and the tapered CD pipeline sub-stages, the clock buffer and digital error correction logic block are at the bottom, the replica-controlled circuit is at the top, and the bandgap reference voltage generator and reference buffer op-amps are shown on the right. The total active area, excluding the PAD and ESD cells, is approximately 1.4 mm × 1.6 mm, whereas the active area of the SH circuit and CD pipeline sub-stages is approximately 0.8 mm × 1.6 mm.

The measured Fast Fourier Fransform (FFT) spectra with input frequencies of 20.1 MHz and 239.9 MHz at 250 MS/s are shown in Fig. 6a. The measured Signal-to- Noise Ratio (SNR) is 65.3 dB, the Spurious Free Dynamic Range (SFDR) is 78.1 dB, and the Signal-to-Noise-and-Distortion Ratio (SNDR) is 64.6 dB for an input frequency of 20.1 MHz. The measured SNR is 62.8 dB, the SFDR is 74.9 dB, and the SNDR is 62.0 dB for an input frequency of 239.9 MHz. The measured nonlinearity of the ADC is shown in Fig. 6b. The maximum Integral NonLinearity (INL) is +1.6/–1.75 LSB, and the maximum Differential NonLinearity (DNL) is +0.45/–0.4 LSB. The INL graph shows large transitions in code at the six thresholds of the 2.5-bit first stage of the pipelined ADC.

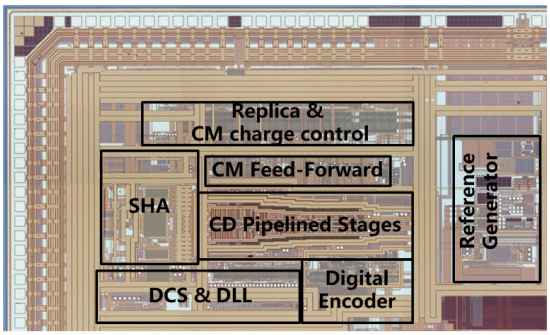


Fig. 5 Die photograph of the 12-bit ADC.

The measured dynamic performance versus input CM voltage level and the amplitude of the 20.1-MHz input at 250 MS/s are shown in Figs. 6c and 6d, respectively. The central input CM voltage of the prototype 12-bit ADC is 0.6 V; it can be seen from Fig. 6c that the variation in SNR for the ADC is less than 3 dB for an input CM level over the 0–1.2 V range. In addition, it can be seen from Fig. 6d that the SNR of the ADC increases linearly with the input amplitude from –63 to –3 dB, which shows very good linearity.

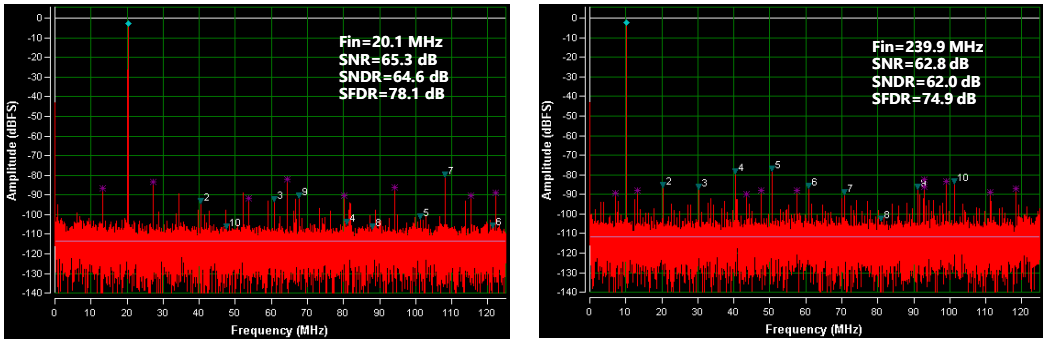
The measured performances of the prototype ADC are compared with those of the recently reported 12-bit ADCs[15−18], as summarized in Table 1. The 12-bit, 250-MS/s CD pipelined ADC based on the proposed feed-forward CM charge control circuit exhibits a power efficiency of 237 fJ/step, which is very good when compared with the recently reported 130-nm, 12-bit ADCs.

6 Conclusion

A feed-forward CM charge control circuit for a high-speed CD pipelined ADC is presented in the paper. It solves the problem whereby the precision of CD pipelined ADCs is restricted by the variation in input

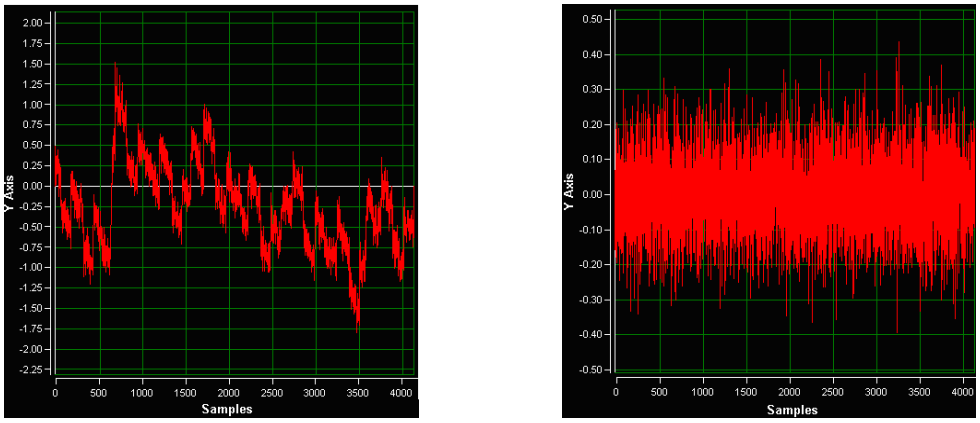
Table 1 Performance summary.

	Year	Sampling rate (MS/s)	Technology (nm)	DNL/INL (LSB)	SNR/SFDR (dB)	Power (mW)	FOM (fJ/step)	Active area (mm^2)
This work	2016	250	180	0.45/1.7	65.3/78.1 (Fin = 20.1 MHz)	85	237	2.24
Ref. [9]	2015	250	65	0.7/1.1	67/84 (Fin = 12.1 MHz)	50	107	2.40
Ref. [15]	2011	150	65	0.5/0.7	67/81 (Fin = 3.79 MHz)	48	194	0.78
Ref. [16]	2012	270	130	0.5/0.8	63.7/76.1 (Fin = 10.1 MHz)	250	1532	1.70
Ref. [17]	2014	200	55	0.6/1.0	64.9/82.9 (Fin = 1 MHz)	30.7	111	0.28
Ref. [18]	2016	650	130	0.4/0.6	65/– (simulation) (Fin = 61 MHz)	502	1045	–



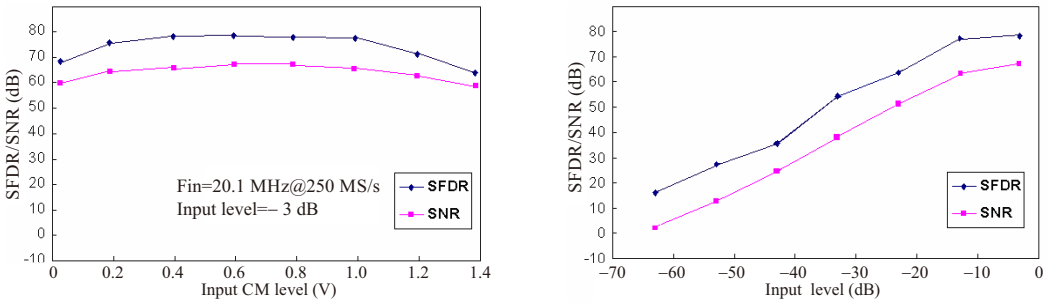
Fin=20.1 MHz @250 MS/s Fin=239.9 MHz @250 MS/s

(a) 32-K FFT spectrum



INL DNL

(b) INL/DNL



(c) SFDR/SNR vs input CM level (d) SFDR/SNR vs input amplitude

Fig. 6 Measured results from the prototype ADC.

CM charge and compensation for the CM charge errors caused by the variation in input CM charge in real time. A 12-bit, 250-MS/s CD pipelined ADC was designed and realized based on the feed-forward CM charge control circuit. The ADC achieved an SFDR of 78.1 dB and SNDR of 64.6 dB for a 20.1-MHz input at full sampling rate. The variation in SNR was less than 3 dB for a CM input voltage over the range 0–1.2 V. The power consumption of the prototype ADC is only 85 mW and the prototype occupies an active die area of 2.24 mm^2. The test results show that the proposed feed-forward CM charge control circuit accurately rejects the variations in input CM charge.

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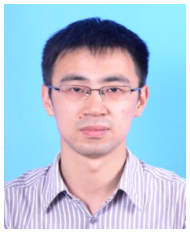

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