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# Carbon Nanotube Transistor with Short-Term Memory

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**Abstract:** Short-Term Memory (STM) is a primary capability of the human brain. Humans use STM to remember a small amount of information, like someone's phone number, for a short period of time. Usually the duration of STM is less than 1 minute. Synapses, the connections between neurons, are of vital importance to memory in biological brains. For mimicking the memory function of synapses, Carbon Nanotube (CNT) networks based thin-film transistors with Electric Double Layers (EDL) at the dielectric/channel interface were researched in this work. A response characteristic of pre-synaptic potential pulses on the gate electrode of this CNT synaptic transistor was shown remarkably similar to Excitatory Post-Synaptic Current (EPSC) of biological synapses. Also a multi-level modulatable STM of CNT synaptic transistors was investigated. Post-synaptic current was shown with tunable peak values, on-off ratio, and relaxation time.

**Key words:** carbon nanotube; thin-film transistor; synapse; excitatory postsynaptic current; short-term memory

## 1 Introduction

The memory and computation of biological brains rely on two basic elements: neurons and synapses. Neuron cells are the basic unit of a brain. Synapses are the fundamental structure for transferring electrical and chemical signals between neuron cells. There are approximately 100 billion neurons and $10^{15}$ synapses in the human brain[1]. Synapses connect neurons by releasing neurotransmitters and firing Excitatory Post-Synaptic Currents (EPSC) as a result of pre-synaptic potential spikes[2]. The connecting strength of synapse, synaptic weight, determines how much triggering spikes contribute to output. Synaptic weight modification is known as synaptic plasticity and is considered a basic mechanism of human memory and learning[3]. Induced by weak and short pre-synapse excitation, EPSC are triggered post-synaptically and hold for a short period of time, and represent Short-Term Memory (STM)[4]. Generally, the duration of STM is less than 1 minute.

Synapses connect neurons, and play a significant role in realizing the memory function in biological brains. Similarly, as the basic unit of brain-like computation, synaptic transistors are the base of brain-like computers. Researchers have been trying to mimic the behavior of synapses by using memristors[5, 6], RRAM[7, 8], and transistors[9–11]. And Carbon Nanotubes (CNT) have also been used in place of silicon[12, 13] to fabricate synaptic transistors[14–16]. Agnus et al.[14] developed an optically gated carbon nanotube transistor that can be controlled by light and potential pulses. Kim et al.[15] reported on a CNT synapse with memory, dynamic logic, and learning functionality. Chen et al.[16] demonstrated a spiking neuron circuit based on a CNT synaptic transistor.

In this paper, CNT-network-based thin-film transistors gated by $SiO_2$ with electric double layers are demonstrated with a large hysteresis window, a high on-off ratio, and low noise. For mimicking the behavior of synapses, EPSC on a transistor channel are triggered

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by a potential spike on the pre-synaptic gate electrode. The STM of this CNT synaptic transistor is realized and investigated by modifying the amplitude of the pre-synaptic potential spike. The response characteristic shows high similarity to biological synapses in terms of tunable peak value, on-off ratio, and relaxation time of post-synaptic current.

## 2 Experimental Detail

Figure 1 illustrates the fabrication procedure of a CNT network synaptic transistor. A 500 nm layer of aluminum, working as the back gate, is deposited on silicon substrate by sputtering. Then a layer of p-doped nanogranular silicon oxide film is deposited as the insulator layer by a Plasma-Enhanced Chemical Vapor Deposition (PECVD) system, using $SiH_4$ and $O_2$ as the reactive gasses, a technique introduced by Zhu et al.[17] Drain (D) and source (S) electrode patterns are defined by lithography. The chip is placed into an oxygen plasma environment for 5 minutes to remove the remaining polymer on the exposed $SiO_2$ surface. Then bilayer Pt/Ti (50 nm/10 nm) is evaporated, followed by a lift-off process. Platinum is chosen for ohmic contact between the CNT network and the electrodes[18, 19]. Titanium, underneath platinum, functions as an adhesion layer.

The CNT network film, functioning as a channel, is transferred onto the substrate by a solution method. The powder of semiconductor-enriched (99.99% content) Single-Walled CNT (SWCNT) is first dispersed into a solvent. N-methyl pyrrolidone (NMP) is used as the solvent because of its high stability and repeatability. Then 1 mg CNT is dispersed into 10 mL NMP using an ultrasonic machine. After that, the solution is diluted to 0.01 mg/mL and homogenized again in an ultrasonic environment. The chip is then immersed into the 0.01 mg/mL CNT dispersion solution for one hour for transfer of the CNT network. Finally, the channels are patterned by lithography and a Reactive Ion Etching (RIE) process by using oxygen as the reactive gas and photo-resist as the mask. The length and width of the channel between the drain and source electrodes are 16 μm and 200 μm, respectively.

## 3 Results and Discussion

### 3.1 Electrical performance of CNT synaptic transistor

The electrical performance of the CNT synaptic transistor was tested by using *Keithely 4200*. The transfer curves on linear and semilog coordinates are shown in Figs. 2a and 2b, respectively, at $V_{sd} = 0.1$ V. The voltage applied on the back gate electrode sweeps

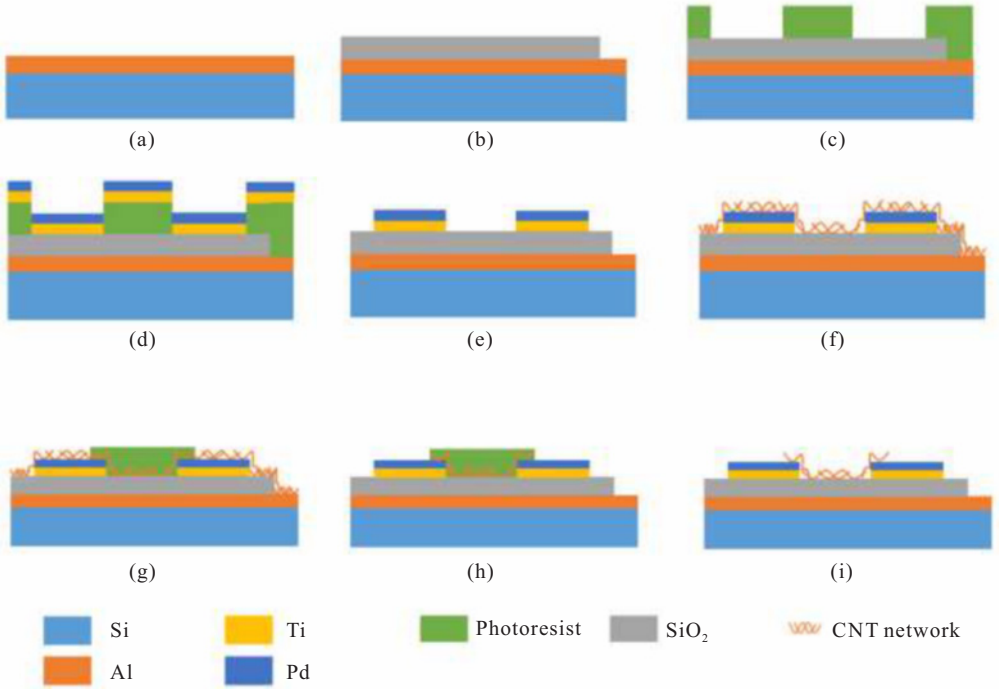


**Fig. 1 Processing steps: (a) Sputter Al on silicon substrate; (b) PECVD nanogranular silicon oxide; (c) Lithography for defining electrodes, then oxygen plasma to clean the surface; (d) Evaporate Ti/Pd; (e) Lift-off; (f) Transfer CNT networks; (g) Lithography to define CNT network channel patterns; (h) Etch CNT network with oxygen plasma; (i) Remove photoresist.**

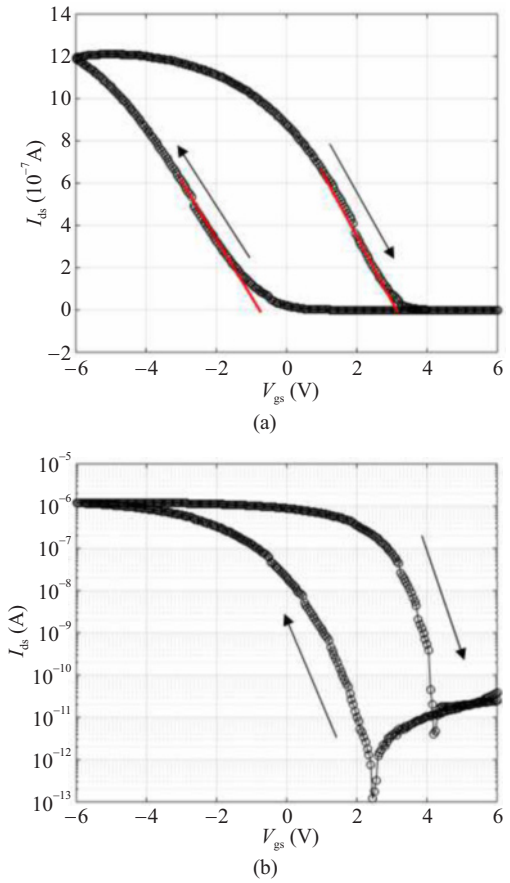


**Fig. 2 (a) Transfer curve of CNT synaptic transistor; (b) Semilog plot of the transfer curve.**

forward and backward from 6 V to −6 V with a step of 50 mV. The on-off ratio is $\sim 10^5$, with 1.2 μA as the "on" current. A large hysteresis window can be observed. The threshold voltage of the CNT synaptic transistor in the forward and backward sweeps of $V_{gs}$ is estimated to be −0.77 V and 3.12 V, respectively, by using extrapolation in the linear region method[20], as shown in Fig. 2a with red lines. It is mainly due to electric-double-layer effect and slow speed of the protons in the $SiO_2$ film[21]. The Subthreshold Slope (SS) of the CNT synaptic transistor is calculated by using the standard formula[22] $SS = d|V_{gs}|/d(\log|I_{ds}|)$ with a result of 925.5 mV per decade. The capacity of the $SiO_2$ film ($C_{ox}$) is around 0.02 μF/cm$^2$ measured by using *Agilent 4284A*. The mobility of the CNT network channel is $\mu_{eff} = 11.0\,cm^2 \cdot V^{-1} \cdot s^{-1}$ estimated by $\mu_{eff} = (dI_{ds}/dV_{gs})/(C_{ox}V_{ds}W/L)$[23].

Figure 3 shows the output characteristic of the CNT synaptic transistor. The $I_{ds} - V_{ds}$ dependences when $V_{gs}$ sweeps from 0 V to −5 V with a step of −1 V show that the CNT synaptic transistor is P-type. Also, the

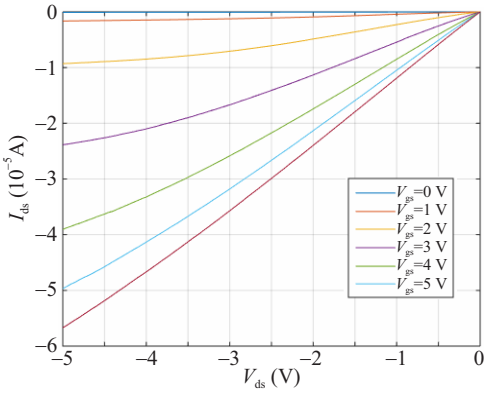


**Fig. 3 Output characteristic of the CNT synaptic transistor.**

transistor is closed with 0 V gate voltage, and open with gate voltage greater than −1 V. This is in accordance with the result that $V_{th} = -0.77$ V. The leakage current on the gate electrode was also detected during the test, as shown in Fig. 4. While the gate voltage varies between −6 V and 6 V, the current that leaks from the gate electrode is less than 300 pA, which is relatively low and negligible. The low leakage ensures the normal function and low noise of the CNT synaptic transistor.

### 3.2 EPSC of the CNT synaptic transistor

A pre-synaptic potential spike is applied to the back gate of the CNT synaptic transistor, as shown in Fig. 5. The amplitude of the spike on the gate electrode is −6 V for opening the P-type CNT network channel. The voltage between the source and drain electrodes $V_{sd}$ is 0.1 V for detecting the transient changing of the CNT network channel. The spike leads to an abrupt current increase on the CNT network channel. This phenomenon is similar to the EPSC of a biological synapse.

Figure 6a shows a schematic image of a biological synapse. Figure 6b shows the structure of a CNT synaptic transistor gated by nanogranular $SiO_2$ with

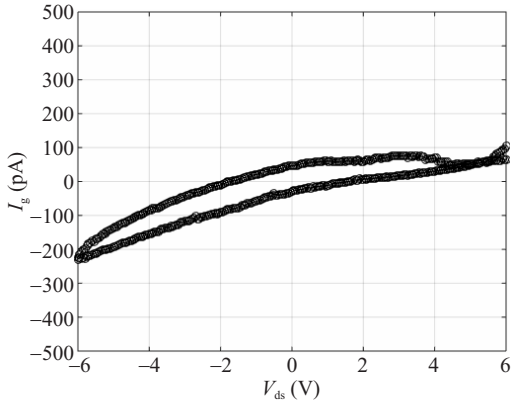


**Fig. 4 Leakage current of the CNT synaptic transistor.**

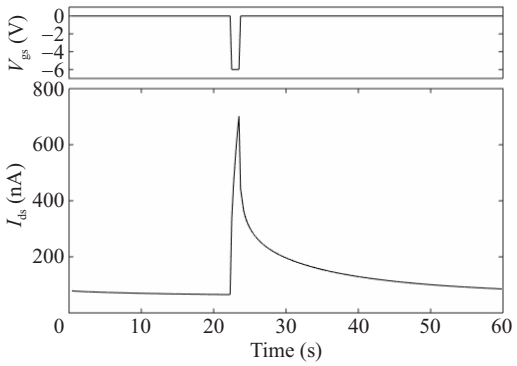


**Fig. 5 EPSC of CNT synaptic transistor.**

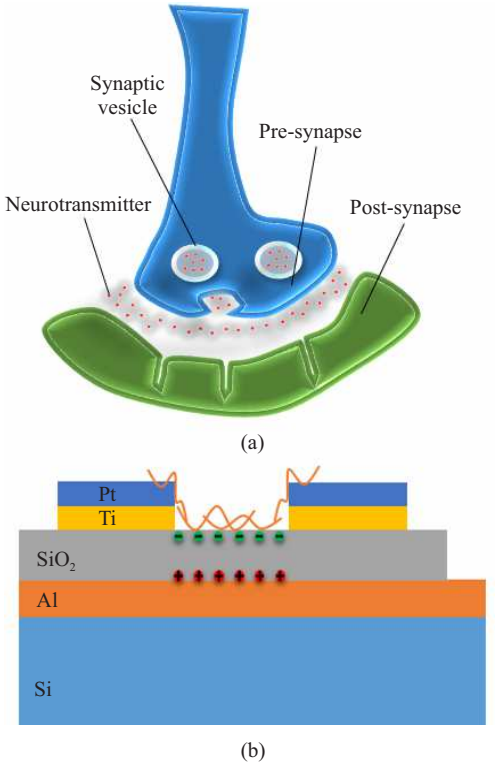


**Fig. 6 (a) Schematic of biological synapse; (b) Structure of CNT synaptic transistor.**

EDL at the dielectric/channel interface layer. In a biological synapse, an impulse at a pre-synapse membrane induces the release of neurotransmitters from synaptic vesicles, which will result in a transient postsynaptic membrane depolarization and increasing of synaptic weight[24]. Here, for the CNT synaptic transistor, the back gate, CNT network channel, and mobile proton in the EDL layer can be regarded as pre-synapse, post-synapse, and neurotransmitters, respectively. So the CNT transistor can be regarded as an artificial synapse with the current or conductance of CNT network channel taken as synaptic weight.

The response characteristic feature shown in Fig. 5 conforms perfectly to the EPSC of a biological synapse. Before the pre-synaptic potential spike, the current on the CNT network channel is around 65 nA. Then the pre-synaptic potential spike is initiated, and lasts for 1 s. Protons leave the interface between the CNT network channel and the $SiO_2$, but negative charges remain there and induce electric-double-layer effect, as shown in Fig. 6b. With pre-synapse excitation, the CNT network channel, which can be regarded as post-synapse, is stimulated, and the current dramatically rises to 700 nA. After the spike, the current does not fall immediately but holds for a short time. In this example, it takes the current 26.8 s to gradually decrease to 100 nA.

### 3.3 STM behavior of CNT synaptic transistor

For the purpose of investigating the STM behavior of the CNT synaptic transistor, distinguishable pre-synaptic potential spikes are used to initiate the EPSC phenomenon, as shown in Fig. 7a. All of the durations of the pre-synaptic potential spikes are 0.8 s. However, the pulse amplitudes of the pre-synaptic potential spike vary from −1 V to −6 V with a step of −1 V. The curves show that the stronger the pre-synaptic spike is, the higher the post-synaptic current abruptly rises. Meanwhile, the current decreases gradually instead of shutting down immediately after the pre-synaptic potential spike. And the stronger the pre-synaptic spike is, the longer the post-synaptic current holds after the spike. This phenomenon is similar to human STM and shows modulatable strength as the pulse amplitude sweeps.

As shown in Figs. 7b–7d, the STM characteristic of the CNT synaptic transistor is adjustable to multiple levels by controlling $V_{\text{pulse}}$. The peak of the post-synaptic current and on-off ratio of the CNT network channel vary from 140 nA to 700 nA and 1.8 to 10.8, respectively, as the pulse amplitude rises from 1 V to 6 V. The relaxation time of the post-synaptic current follows a similar trend, increasing from 0.8 s to 26.8 s as amplitude rises, which is defined as starting from the end of pre-synaptic spike and ending when the drain current decreases below 100 nA.

## 4 Conclusion

In summary, a CNT-network-based thin-film transistor gated by $SiO_2$ with EDL at the dielectric/channel interface was demonstrated as a CNT synaptic transistor that can mimic the EPSC and STM features of biological synapses. The elementary features of the

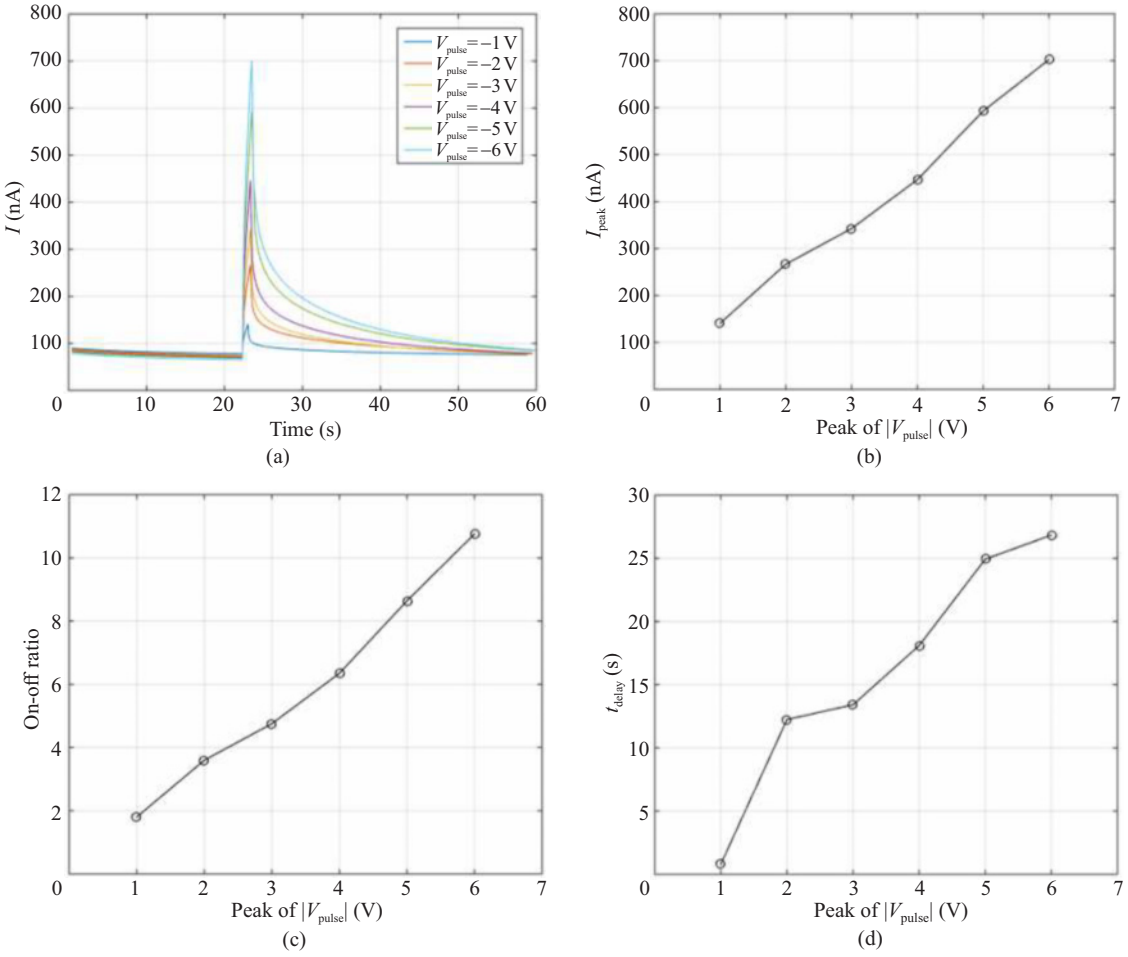


**Fig. 7 (a) EPSC induced by pre-synaptic potential spike with amplitude sweeping from –1 V to –6 V; (b) Dependence of peak of post-synaptic current on $V_g$; (c) Dependence of on-off ratio current of CNT network channel on $V_g$; (d) Dependence of relaxation time of post-synaptic current on $V_g$.**

CNT synaptic transistor were shown with a large hysteresis window that the threshold voltage can be from −0.77 V to 3.12 V, a high on-off ratio of $\sim 10^5$, and a negligible leakage current less than 300 pA. To mimic the behavior of synapses, EPSC on the channel of the CNT synaptic transistor were triggered by a potential spike on the pre-synaptic (gate) electrode. With the excitation of the pre-synapse gate, the current of the CNT network channel, which can be regarded as a post-synaptic gate, dramatically rose. After the spike, the current held for a short time and gradually decreased. The multi-level STM of CNT synaptic transistor was realized and investigated by modifying the amplitude of the pre-synaptic potential spike from −1 V to −6 V. The response characteristic shows great similarity to biological synapses in terms of tunable peak value, on-off ratio, and relaxation time of post-synaptic current; these ranged from 140 nA to 700 nA, 1.8 to 10.8, and 0.8 s to 26.8 s, respectively. This multi-level modulatable STM CNT synaptic transistor has potential for use as an artificial synapse in neural networks.

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## References


[1] D. A. Drachman, Do we have brain to spare? *Neurology,* vol. 64, no. 12, pp. 2004–2005, 2005.

[2] G. Q. Bi and M. M. Poo, Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type, *The Journal of Neuroscience*, vol. 18, no. 24, pp. 10464–10472, 1998.

[3] D. L. Schacter and A. D. Wagner, Learning and memory, in *Principles of Neural Science*, E. R. Kandel, J. H. Schwartz and T. M. Jessell, eds. New York, NY, USA: McGraw-Hill, 2000, pp. 1227–1246.

[4] R. M. Chapman, J. W. McCrary, and J. A. Chapman, Short-term memory: The "storage" component of human brain responses predicts recall, *Science,* vol. 202, no. 4373, pp. 1211–1214, 1978.

[5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, The missing memristor found, *Nature,* vol. 453, no. 7191, pp. 80–83, 2008.

[6] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nanoscale memristor device as synapse in neuromorphic systems, *Nano Letters,* vol. 10, no. 4, pp. 1297–1301, 2010.

[7] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, et al., RRAM-based synapse for neuromorphic system with pattern recognition function, presented at Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2012.

[8] S. Yu, H. Y. Chen, B. Gao, J. Kang, and H.-S. P. Wong, HfO$x$-based vertical resistive switching random access memory suitable for bit-cost-effective three-dimensional cross-point architecture, *ACS Nano,* vol. 7, no. 3, pp. 2320–2325, 2013.

[9] J. Shi, S. D. Ha, Y. Zhou, F. Schoofs, and S. Ramanathan, A correlated nickelate synaptic transistor, *Nature Communications*, vol. 4, no. 2676, pp. 1–9, 2013.

[10] L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, and Q. Wan, Artificial synapse network on inorganic proton conductor for neuromorphic systems, *Nature Communications*, vol. 5, no. 3158, pp. 1–7, 2014.

[11] H. Tian, W. Mi, X. F. Wang, H. Zhao, Q. Y. Xie, C. Li, Y. X. Li, Y. Yang, and T. L. Ren, Graphene dynamic synapse with modulatable plasticity, *Nano Letters,* vol. 15, no. 12, pp. 8013–8019, 2015.

[12] R. H. Baughman, A. A Zakhidov, and W. A. de Heer, Carbon nanotubes—The route toward applications, *Science,* vol. 297, no. 5582, pp. 787–792, 2002.

[13] M. M. Shulaker, G. Hills, N. Patil, H. Wei, H. Y. Chen, H.-S. P. Wong, and S. Mitra, Carbon nanotube computer, *Nature,* vol. 501, no. 7468, pp. 526–530, 2013.

[14] G. Agnus, W. Zhao, V. Derycke, A. Filoramo, Y. Lhuillier, S. Lenfant, D. Vuillaume, C. Gamrat, and J. P. Bourgoin, Two-terminal carbon nanotube programmable devices for adaptive architectures, *Advanced Materials,* vol. 22, no. 6, pp. 702–706, 2010.

[15] K. Kim, C. L. Chen, Q. Truong, A. M. Shen, and Y. Chen, A carbon nanotube synapse with dynamic logic and learning, *Advanced Materials,* vol. 25, no. 12, pp. 1693–1698, 2013.

[16] C. L. Chen, K. Kim, Q. Truong, A. Shen, Z. Li, and Y. Chen, A spiking neuron circuit based on a carbon nanotube transistor, *Nanotechnology,* vol. 23, no. 27, p. 275202, 2012.

[17] L. Q. Zhu, J. Sun, G. D. Wu, H. L. Zhang, and Q. Wan, Self-assembled dual in-plane gate thin-film transistors gated by nanogranular $SiO_2$ proton conductors for logic applications, *Nanoscale*, vol. 5, no.5, pp. 1980–1985, 2013.

[18] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Ballistic carbon nanotube field-effect transistors, *Nature*, vol. 424, no. 6949, pp. 654–657, 2003.

[19] S. Wang, Q. Zeng, L. Yang, Z. Zhang, Z. Wang, T. Pei, L. Ding, X. Liang, M. Gao, Y. Li, et al., High-performance carbon nanotube light-emitting diodes with asymmetric contacts, *Nano Letters*, vol. 11, no. 1, pp. 23–29, 2010.

[20] A. Ortiz-Conde, F. J. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, A review of recent MOSFET threshold voltage extraction methods, *Microelectronics Reliability*, vol. 42, no. 4, pp. 583–596, 2002.

[21] J. Zhou, C. Wan, L. Zhu, Y. Shi, and Q. Wan, Synaptic behaviors mimicked in flexible oxide-based transistors on plastic substrates, *Electron Device Letters, IEEE*, vol. 34, no. 11, pp. 1433–1435, 2013.

[22] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, Field-modulated carrier transport in carbon nanotube transistors, *Physical Review Letters*, vol. 89, no. 12, p. 126801, 2002.

[23] U. J. Kim, E. H. Lee, J. M. Kim, Y. S. Min, E. Kim, and W. Park, Thin film transistors using preferentially grown semiconducting single-walled carbon nanotube networks by water-assisted plasma-enhanced chemical vapor deposition, *Nanotechnology*, vol. 20, no. 29, p. 295201, 2009.

[24] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nanoscale memristor device as synapse in neuromorphic systems, *Nano Letters*, vol. 10, no. 4, pp. 1297–1301, 2010.


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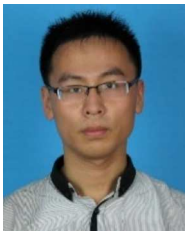

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