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Data Fusion with Genetic Algorithm Based Lifetime Prediction for Dependable Multi-Processor System-on-Chips

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Abstract: With the prevalence of big-data technology, intricate, nanoscale Multi-Processor System-on-Chips (MP-SoCs) have been used in various safety-critical applications. However, with no extra countermeasures taken, this widespread use of MP-SoCs can lead to an undesirable decrease in their dependability. This study presents a promising approach using a group of Embedded Instruments (EIs) inside a processor core for health monitoring. Multiple health monitoring datasets obtained from the employed EIs are sampled and collated via the implemented experiment and thereafter used for conducting its remaining useful lifetime prognostics. This enables MP-SoCs to undertake preventive self-repair, thus realizing a zero mean downtime system and ensuring improved dependability. In addition, a principal component analysis based algorithm is designed for realizing the EI data fusion. Subsequently, a genetic algorithm based degradation optimization is employed to create a lifetime prediction model with respect to the processor.

Key words: data fusion; genetic algorithm; lifetime prediction; health monitor; multi-core System-on-Chips (SoCs); embedded instruments

1 Introduction

Currently, Multi-Processor Systems-on-Chips (MP-SoCs) in the low nanometer range (10–28 nm) are increasingly used owing to their excellent multitasking and parallel computing capabilities. MP-SoCs are used in safety-critical applications in space and aviation[1], military systems[2], and automotives[3]. Stress conditions, such as vibration, radiation, and temperature, in safety-critical applications are extremely severe. For instance, inside a car, wheel sensors and controllers must withstand the operating ambient temperature of around 200 ℃[3]. Furthermore, the control electronics in aircraft must operate well in a temperature range of −55 ℃ to 200 ℃. These systems require high dependability with typically a close to zero mean downtime because even a brief loss of processor control might has disastrous effects[4]. Furthermore, the dependability of these intricate MP-SoCs tends to decrease automatically due to different aging processes under harsh conditions, such as negative-bias temperature instability, electromigration (namely EM), and Hot Carrier Injection (HCI)[5]. Therefore, to ensure high dependability and zero downtime throughout the operational lifespan, online health monitoring for target SoCs is a must, especially in safety-critical applications operating under extreme environmental circumstances. The use of Embedded Instruments (EIs)[6] has been implemented for several years. For instance, Ring Oscillators (ROs) are often used as a process evaluation module embedded in different design corners to guarantee error-free processing. Further, a

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temperature sensor functionally serves as an EI to track the temperature of the different corners of a chip during the lifetime of an SoC. Meanwhile, to lower the cost of SoC testing, EIs and Internal Joint Test Action Group (IJTAG) communication networks[7] were introduced, eventually becoming an industry standard. Reusing these test resources to achieve a reliable-system design has been inspired by this. A substantial number of EIs will be included in MP-SoCs in the near future and also in IJTAG-based design networks for control and observation. Machine learning and random coefficient regression techniques are two of the most popular data-driven techniques used for prognostic purposes. The first technique typically utilizes observable data and statistical methods, such as least squares[8]. The second technique uses health monitoring data to create a deterioration path, from which the Remaining Lifetime Prognostics (RLP) distribution is determined[9]. A previous study investigated how to justify an ideal critical level and a way to determine monitoring intervals[10], while other studies optimized remaining lifetime distribution for a single functioning device using sensor-based health-monitored data[11, 12]. Within a Bayesian framework, this model can continually update the parameters of the random coefficient model. In this study, based on the measured historical data from our designed variant EIs, a Principal Component Analysis (PCA) algorithm[13] is used for the required fusion of the multidimensional dataset. Subsequently, a Genetic Algorithm (GA) for degradation optimizatio[14] for the RLP of an MP-SoC is presented. The remainder of the article is organized in the following manner. In Section 2, the dependability of MP-SoCs and implemented EIs are introduced. Section 3 discusses the generated health monitoring database, which is used as the input for the RLP of a processor core. In Section 4, the implemented data-fusion PCA algorithm for our EIs is proposed. Furthermore, various EIs and the fused dataset are used as different inputs of our proposed GA optimization based RLP. The study's conclusions and future work prospects are presented in Section 5.

2 EIs Based on MP-SoC Architecture

A homogeneous MP-SoC consisting of nine processing cores from Xentium® has been constructed within our BASTION project[14]. Its photomicrograph is depicted in Fig. 1 (upper left inset). This is the so-called Reconfigurable Fabric Device (RFD) that can be utilized to command and monitor the Xentium processing core

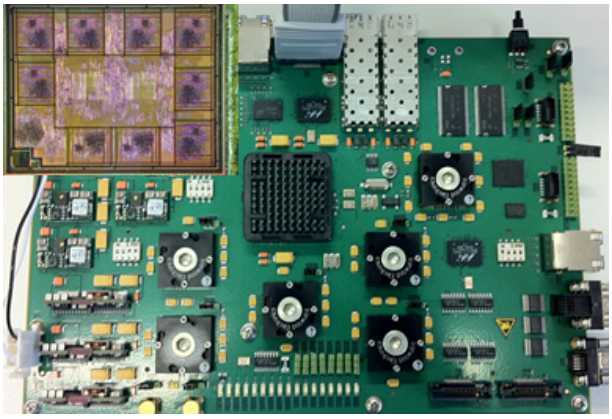

Fig. 1 Board-level configuration of MP-SoCs, with five RFD cores connected on the bottom. The above inset shows the nine Xentium processors inside the RFD[4]. The ARM-based general-purpose processor is shown on the top right.

when connected to an ARM926-based general-purpose device (top right). A packet switched Network-on-Chip (NoC) with routers and network interfaces (NI) was used for the whole system communication. For high performance computing while communicating within certain applications used in space, automotive, and military (e.g., a global navigation satellite system with a beam former) fields, this MP-SoC (i.e., RFD) is applied as an ultra-low-power digital signal processing device[4]. The key component of this strategy for ensuring dependability is the electronic quarantine of a Xentium core that is discovered to be defective by an on-chip controlling dependability manager in the RFD, after which a spare (or underutilized) processor replaces the defective processor through run-time mapping[15]. The Xentium is a very large instruction word processor that uses the UMC 90 nm CMOS technology. It operates at a clock frequency of 200 MHz and has a silicon area of 1.2 mm^2. This processor core was first created as a component of the RFD shown in Fig. 1. The NoC links the Xentiums together, and each individual Xentium may link through the NIs to the neighboring routers of NoC, which can also be coupled to more traditional bus designs (like Amba) to connect to other necessary peripherals. The Xentium is required not to be used when running life-critical Apps, e.g., the STARS project's use case of UAV communication for this Moon IC[16]. Therefore, in the proposed MP-SoC, potential Xentium core failure must be anticipated in time, and maintenance must be carried out before a failure occurs. For the aforementioned reasons, the EIs shown in Fig. 2 are employed and can be used to guarantee 100% availability in the target applications.

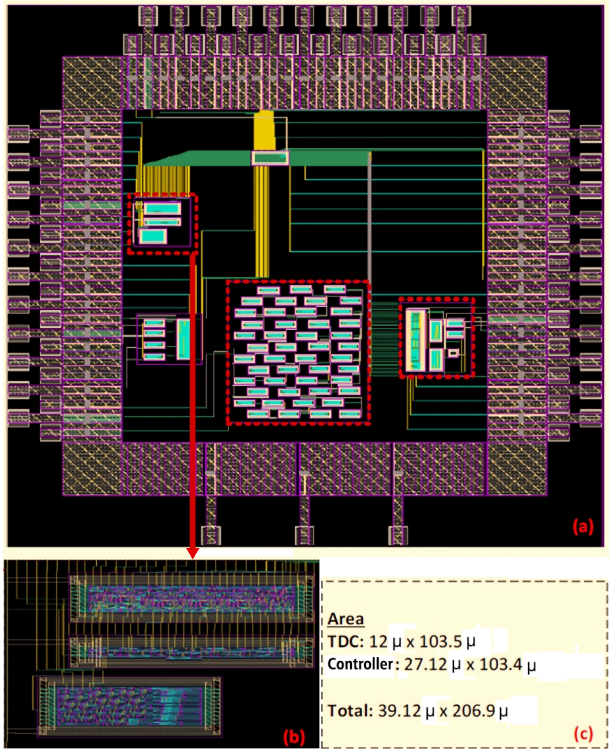

Fig. 2 (a) Three different types of EIs inside a single Xentium core; (b) zoomed-in image of the timing EI layout; and (c) EI area calculation.

Meanwhile, Fig. 2a shows the layout of one timing EI for Critical Path Delay (CPD) monitoring (left), one voltage EI (right) for the quiescent drain-drain current (namely IDDQ), and one EI for temperature monitoring (middle). The Taiwan Semiconductor Manufacturing Company (TSMC) standard cell library containing inverters with minimum propagation delay are then used to implement the TDC. The silicon areas of the TDC module (middle), critical path (bottom), and controller (top) are depicted in Figs. 2b and 2c. The TDC block, which may be inserted into the Xentium core, has a 12 µm×103.5 µm surface area. The planned timing EI has a total size of 39.12 µm×206.9 µm (or 0.008 mm^2). Different types of critical paths are implemented on the chip to properly define the EI.

3 Health Monitoring Data Generated by EIs

For collecting data for the health monitoring database, 46 Xentium processors are monitored under the stress operation condition of the high-temperature operation life approach. This is done to evaluate the dependability of the proposed MP-SoC in conjunction with the designed EIs.

The stress condition is set in accordance with the standard JEDEC operation (JESD22-A108)[17]. A stress supply of 1.2 V for the core power supply (typical value: 1 V) is employed. Meanwhile, the Xentium processor is stressed with ultra-speed frequency at 240 MHz (typical value = 200 MHz). This stress condition for the Xentium processor is applied for 1000 h or 6 weeks. The stress temperature is set to 125 °C. Power supply based IDDQ and transient drain-drain current (namely IDDT), or collectively refferred to as IDDx, are measured. A variety of CPD monitors are included in the expected aged critical paths of the processor. Measurements are also taken for the so-called process-related EIs, such as the frequency of ROs. Based on our developed EIs, CPD and IDDx during the Xentium normal run are carried out after each stress week. Figure 3a depicts the CPD for 46 processors fresh (nonaged) and 6 distinct aging conditions, while Figs. 3b and 3c present the IDDQ and IDOT values for all processors, respectively, including the initial fresh-state value at time zero. IDDQ and IDDT measurements are comparable in terms of the degradation trend. Figure 3d shows that the RO frequency changes for three different aging conditions. All test results demonstrate degrading behavior. Furthermore, in terms of aging time, the CPD rises while the IDDx decreases.

4 Data Fusion Using GA Optimization Based Lifetime Prediction

Based on the multidimensional health monitoring dataset measured using our developed EIs, we propose data fusion for the initial process. Furthermore, a PCA-based algorithm is employed in this study.

4.1 PCA and EI data fusion

The PCA algorithm has proven to be an effective approach to reducing the dimensions of a multidata set[14]. This can be fulfilled by mapping the used dataset onto eigendirections corresponding to the greatest eigenvalues of the sampled covariance matrix. The primary goal of the PCA algorithm is to generate one reduced multidimension dataset as a replacement. A considerable portion of the variance of the original data from various EIs may be recovered using the largest eigenvalues, sometimes referred to as the Principal Components (PCs). Three PCs exist in our study: CPD, RO, and IDDx, which are not exclusive representations of an EI. Considering the fresh condition and aging period, Fig. 4a illustrates the co-relationship of eigenvalue between the first and second PC. This

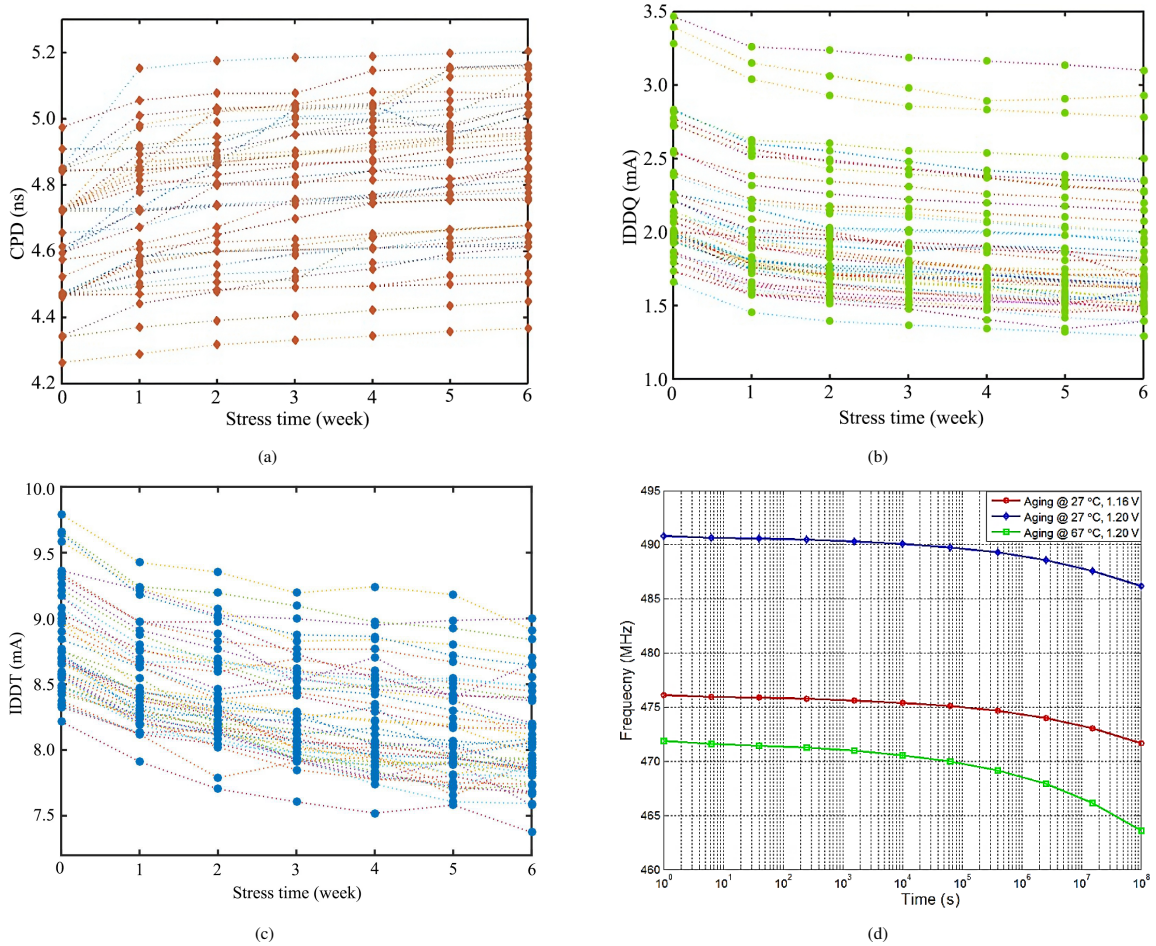

Fig. 3 Measurement results of (a) CPD, (b) IDDQ, and (c) IDDT monitor in 46 Xentium processors colored differently, and (d) RO frequency monitor with 3 aging condictions.

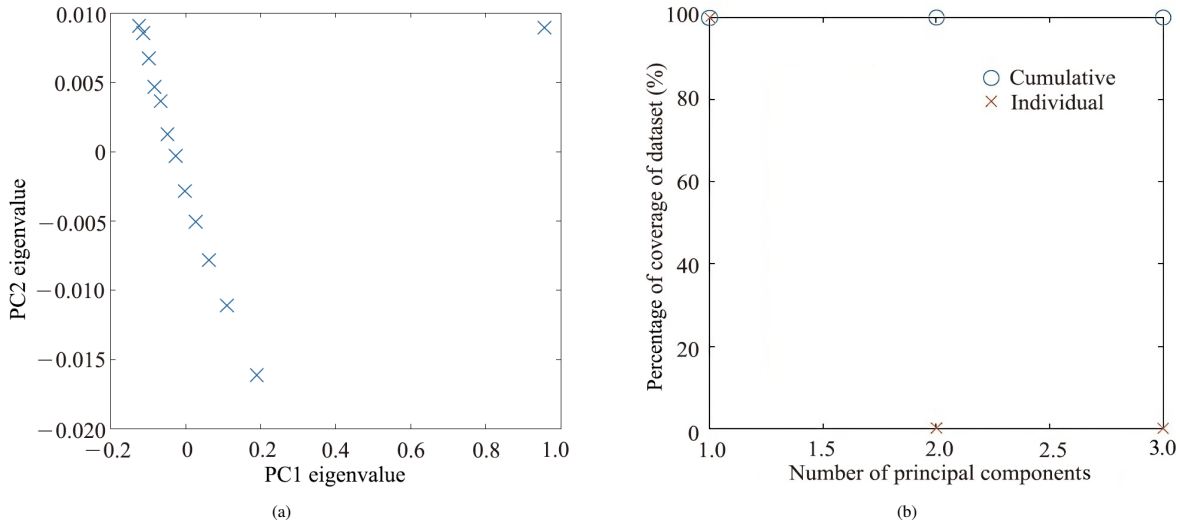

Fig. 4 (a) Graph illustration of co-relationship of eigenvalues between two PCs and (b) coverage contribution of PCs for the whole dataset.

diagram demonstrates the existence of two separate groups. One group can be found on the right side of the diagram, representing the fresh dataset of the proposed MP-SoC, while the other one can be found on the left side, depicting the monitored aging results. The notable difference between the two groups suggests that the processor undergoes considerable degradation once the aging process begins. The contribution of PCs in

covering the entire dataset is shown in Fig. 4b, in which each PC is considered both separately and cumulatively. PC1 fulfills a 100% coverage function, whereas PC2 and PC3 have no contributions to the mapping of data representation. As a result, in the part that follows, the RLP computation is performed using PC1.

The multiple data attributes must first be normalized to create a unitless data collection with the same scale before using the data-fusion algorithm. The term "feature scaling" refers to data scalability, which can range between a minimum and a maximum value. The final RLP comes after completing the data-fusion cycle, which includes the aforementioned data preparation and subsequent PCA.

4.2 GA procedure for optimizing CPD degradation

Based on reliable natural selection processes, GA[18] has shown its capacity to handle optimization issues that cannot be easily addressed using traditional methods. Because discontinuous and nonlinear objective functions can be handled, and many local optima in the dataset can be identified in GA, GA does not need an initial estimate of the solution[19]. GA can also work on a collection of candidate solutions as opposed to other optimizers with just one candidate solution. The coefficient sets of the proposed degradation model have been optimized in this study using GA to account for the CPD. In the GA technique, the best solution to the optimization problem is often obtained from a population of potential solutions (referred to as "individuals"). Each individual has distinct chromosomes that are utilized in crossover and mutation processes to develop them. To do this, the chromosomes are converted into binary bits (strings of 0s and 1s) that are then modified during the GA method[20]. Meanwhile, "generation" is the term used to describe the population in each iteration of the evolution method, which begins with a population of randomly created individuals. Every individual in the population is tested for fitness in each generation. The fittest ones are chosen from the present population, and their chromosomes are tweaked (recombined or randomly altered) to create a new generation. The following iteration uses a fresh generation of potential solutions. GAs often end after a specific number of generations[20].

Figure 5 depicts the flowchart of the proposed GA throughout the CPD optimization process. The core functions of GA are outlined as follows:

Step 1: Initialization. Our goal is to optimize the degradation path for CPD using previously available data. The participants in the GA optimization are referred to as "candidate solutions". These participants consist of measured data that form the CPD degradation path. In our previous work, CPD in the Xentium is shown to have a power law degradation trend. $delay\,(t)$ represents power law with respect to aging time[16], as shown below:

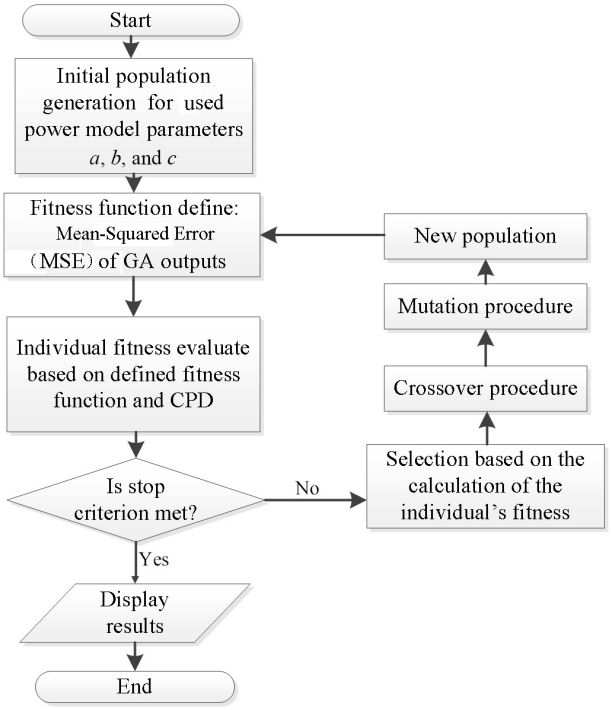

Fig. 5 Diagram of the GA procedure used for the CPD degradation trend optimization.

$$delay(t) = a + bt^c \tag{1}$$

where a, b, and c are the parameters to be solved based on measured CPD data.

The population of one GA generation, which in this example comprises 100 randomly produced individuals, contains the fittest individuals. In the solution of parameters a, b, and c, a population of 100 is chosen because if the initial population is too small, the algorithm may not find the best solution, and if it is too large, the method may incur excessive processing costs[20].

Step 2: Fitness function and fitness evaluation. The MSE of the GA output and the measured CPD value determine the fitness function $f(GA)$, which is represented by the following definition:

$$f(GA) = \frac{\sum N(CPD_{\mathrm{GA}} - CPD_{\mathrm{measured}})^2}{N} \tag{2}$$

where N is the number of our potential solutions, CPD_{GA} is the list of candidates selected by the GA, and CPD_{measured} is the list of outcomes of the measured CPD. Following the creation of the new population,

the fitness function is used to assess each individual's adaptability. The principle is that the lower the individual's fitness value, the further the individual's ranking moves up.

Step 3: Selection. Roulette-wheel selection[21] is employed for this approach. Hence, the likelihood that an individual would be chosen for inclusion in the population of the following generation would be inversely correlated with their fitness, as determined in Step 2.

Step 4: Crossover. The individuals from the second generation are now created together with the mutation process in the next stage. During the crossover process, a pair of "parent" solutions is chosen to construct a "child" solution, thereby creating a new population that generally shares as many traits as its "parents". New children are created when the parents cross over. Figure 6 demonstrates how the crossover is carried out using the dispersed crossover approach[21]. The parent individuals are matched off at random. Then, the chromosomal bits (0 and 1 in Fig. 6) are randomly selected using a binary vector that is also generated at random. The equivalent chromosome bits of Child 1 come from Parent 1 if the vector bit is 1 and from Parent 2 if the bit is 0. The parts are finally joined to create two offspring (Child 1 and Child 2). Therefore, two "children" with combined traits from both parents are created. When the crossover probability is 1, it means that every chromosome chosen is used for reproduction. However, empirical studies[20, 21] demonstrated that the desired outcomes are obtained by a crossover probability between 0.65 and 0.95, suggesting that the likelihood that a chosen chromosome remains unchanged to the next generation (aside from any changes brought on by mutation) with range from 0.35 to 0.05. A probability of 0.90 is applied in our study.

Step 5: Mutation. The mutation choices describe how the GA modifies individuals randomly and subtly to produce mutated offspring. Herein, the mutation operation is used to ensure genetic variation and to allow the GA to seek a large space. The goal of mutation is to cause a random change in the chromosomes, such as when 0 turns into 1 (Fig. 6) or vice versa. This is because the mutation rate is in the order of one out of every thousand, or 0.1% of the parent's chromosome bits.

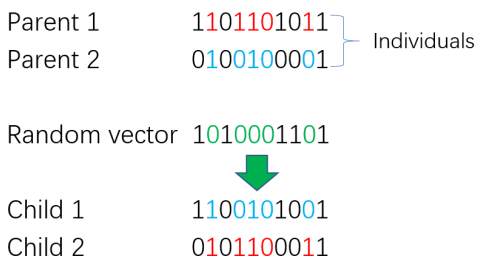

Fig. 6 Crossover process between two (dispersed) individuals, Parents 1 and 2. Based on the bit-value of the random vector, colors depict how the chromosomes operate.

4.3 Remaining lifetime calculation based on the GA-optimized delay trend

The GA cycle is completed after mutation. The GA in this instance is programmed to operate for a maximum of 100 generations. Simultaneously, the CPD findings from our 30 Xentium processors are utilized for training the delay-degradation trend model. For the purpose of validation, the CPD results from the remaining 18 processors are employed herein; this is also known as the holdout approach[22], used to ensure the accurate assessment of the projected model. Figure 7 displays the optimization result with data and illustrates the general RLP for all data (48 Xentium processors). The RLP of each Xentium is computed according to the GA learning trend based on the CPD measurement result from the EI and on the CPD threshold point of 8.5 ns, which is established using the static-timing analysis study for the Xentium processor[16]. The red line in Fig. 7 depicts the general learned deterioration trend of 30 devices from the

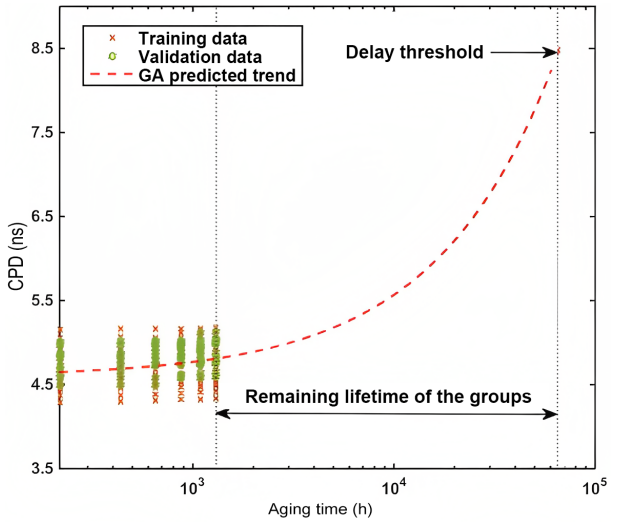

Fig. 7 Degradation path of the CPD prediction, in which the training data (for 30 Xentiums) are in red, while the validation data for 18 Xentiums are in green. Static-timing analysis of the netlist following synthesis yields a delay threshold of 8.5 ns. The *x*-axis uses the log scale.

training set. Meanwhile, the computed RLP for various combinations of fused EI datasets for both Xentium1 and Xentium2 processors are shown in Fig. 8. Using the measurement of the EI for the CPD monitoring, the RLP after 6 weeks of stress run for Xentium1 is calculated to be another 2.7 years, while for the EIs measured using IDDx and RO, the values are 5.3 years and 3.2 years, respectively. The RLP for Xentium1 is 3.5 years according to our employed PCA based fusion algorithm (i.e., fusion of CPD, RO, and IDDx values). The RLP values vary depending on the EI dataset combination: 3.7 years, 2.9 years, 4.0 years, and 3.5 years for CPD+IDDx, CPD+RO, RO+IDDx, and CPD+RO+IDDx, respectively. Meanwhile, for the RLP of the Xentium2 processor, single EI for IDDx, RO, PC1, and CPD yields RLP values of 4.3 years, 10.1 years, 5.7 years, and 4.9 years, respectively. Combined with fused EI, i.e., CPD+IDDx, CPD+RO, RO+IDDx, and CPD+RO+IDDx yield RLP values of 6.3 years, 4.6 years, 6.8 years, and 5.8 years, respectively. The minimal value of RLP must be taken for Xentium 1 and Xentium 2 to implement suitable countermeasures based on the findings of the various EIs that are employed. The computed RMSE values of the stated RLP for EIs are also shown in Fig. 8. The findings demonstrate that relatively lower RMSE values for all cases are suitable for a safety-critical application. For instance, when compared with the calculated RLP based on CPD (2.8 years and 3.7 years for Xentium 1 and Xentium 2, respectively), the corresponding RMSE values are calculated as 35.0 hours and 150.8 hours for Xentium 1 and Xentium 2, respectively. This indicates that RLP with fused data can reach good accuracy.

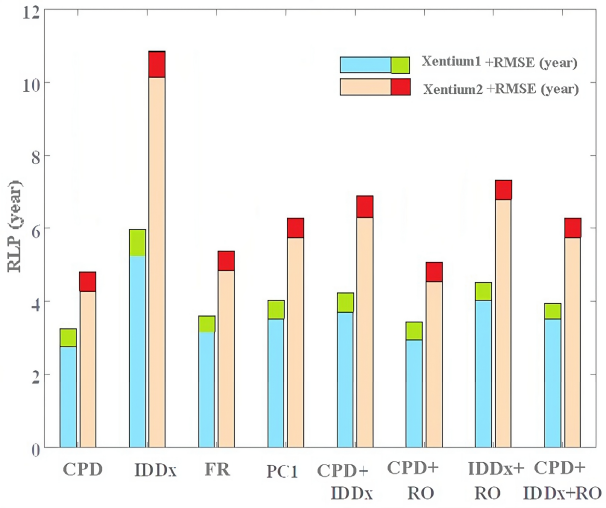

Fig. 8 RLP values for various single, fused, and combined EIs are calculated, which are calculated for various combinations with RMSE.

5 Conclusion

The development of a dependable MP-SoC under (severe) aging circumstances in a particular safety-critical application is described in this study. The target of this study realizes an MP-SoC with zero downtime. The proposed method integrates a variety of EIs for the health monitoring of each processor core, thus generating a PCA-based data-fusion algorithm and GA-based lifetime prediction algorithm. The health monitoring data based on our EIs (i.e., IDDx, CPD, and RO) are created and subsequently fused using a PCA-based algorithm. Then, the RLP is optimized using a GA flow-based algorithm.

According to the RLP results, the designed EI for CPD measurement has the minimum RLP value for two Xentium processors, while IDDx has the maximum value. In accordance with the predicted minimum RLT from different PCA data-fusion results, the dependability of the proposed MP-SoC can be increased using appropriate countermeasures, such as a run-time task/core remapping before failure occurs.

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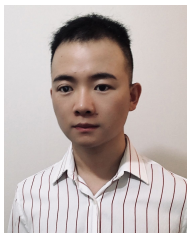

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