Signal Integrity and Power Integrity

En-Xiao Liu, Guest Editor

Welcome to the Signal Integrity and Power Integrity Column!

With great pleasure, I introduce to you a contribution by Biyao Zhao and co-authors about a systematic approach for Power Integrity (PI) analysis of power distribution networks (PDNs) in multi-layered printed circuit boards (PCBs). Power Integrity is an essential consideration for high-speed designs. Noise in PDNs due to poor designs may lead to malfunction or failure of high-speed circuit systems. One main objective of the PDN design is to achieve target impedance. For this purpose, various methodologies have been proposed in the literature to address the PI modeling and analysis of PDNs, many of which are already in commercial use.

In this paper, what makes the authors' work different is that their approach is devised to link the PI results with the geometrical features of the PDN, which can guide the designers for a PCB PDN design. It is realized though decomposition of inductance of two critical current paths: one is the mid-frequency PCB equivalent inductance L_{PCB_EQ} and the other is the high-frequency IC interconnect inductance L_{PCB_IC}. Some of its underlying techniques include circuit reduction and cavity model. With some workarounds, the proposed approach will be able to handle more general cases, such as PDNs with multiple stack-ups and of irregular shapes.

I hope that you will find this practical paper useful and illuminating. Have a pleasant reading!

Systematic Power Integrity Analysis Based on Inductance Decomposition in a Multi-Layered PCB PDN

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Abstract—An approach is presented for power integrity analysis on multi-layer printed circuit boards in this paper. Two critical current paths are analyzed. Inductance decomposition is applied to identify the critical parameters that can influence the PDN input impedance. Two types of stack-ups are used to perform sensitivity analysis to illustrate the effectiveness of PDN design guidelines. Based on the analysis of the inductance contribution from different blocks in the PCB PDN, a systematic approach to obtain a complete understanding of PDN behavior is proposed. The approach can be used to provide design guidance in PDN design practice.

Keywords— Power distribution network, PDN impedance, current path.

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I. Introduction

The switching current of integrated circuits (ICs) from power to power return causes voltage ripple on the power rails [1]-[4]. The voltage ripple can propagate through the power distribution network (PDN) and be coupled to other power nets, signal nets or IOs, resulting in signal integrity problems, radiation issues, and an increase in power consumption [5]-[7]. Designing a good PDN for high-speed digital systems to limit the voltage ripple within specifications is crucial for high-speed digital system design.

Commercial post-layout simulation tools and numerical electromagnetic tools for PDN impedance analysis are mature and powerful, and are used often to analyze PDN designs. The PDN input impedance can be extracted accurately to check the impact of potential design solutions. However, the results are not readily related to the geometry details of the PDN design [7]. In most PI design scenarios, the designers often need to run many simulations or perform measurements to identify the limiting factor of a design. Each design is adjusted incrementally, often in a trial-and-error fashion until it meets a target impedance specification. The process can be time-consuming due to the complexity of the

geometry. A systematic method of power integrity analysis to guide the PCB PDN design remains to be developed.

There are design best practices from experience, or design guidelines to follow in PCB PDN design to lower the PDN input impedance [8]-[11]. Many of the guidelines or analyses are from case-by-case summaries. The effectiveness of the same approach in different PDN designs may vary. Adding decoupling capacitors (referred to as 'decaps' for brevity) is a common way to reduce the PDN input impedance. In some cases, increasing the number of decaps can dramatically reduce the PDN input impedance. While in other cases, adding decaps is not as effective, and the input impedance looking into the PDN from the IC decreases only slowly. In addition, it is known that adding the decap vias in alternating directions between nearby power and ground via pairs can reduce the number of decaps needed by taking advantage of mutual inductance [12]. In other designs, the same approach of placing via pairs in alternating directions may introduce little difference. Similarly, other design tips can result in significant reduction in the PDN impedance in one case, while have little effects on the design. The impact of different design guidelines on the PDN input impedance needs to be quantified in a systematic way.

An analysis based on the current paths and the associated inductance is proposed to identify the critical geometry parameters that have a large impact on the PDN input impedance. The analysis methodology enables designers to have a detailed and complete understanding of a PDN design. The limiting factor of each design can then be readily identified. Based on this information, design rules and guidelines can be developed for similar designs. By analysing different scenarios, the effectiveness of the design tips can be quantified. Using this approach, the physical connection between the PDN input impedance and the geometry is illuminated.

The equivalent inductance from the IC to the decaps is decomposed into distinct pieces associated with the current path, which leads to the analysis method proposed herein. Based on the analysis, the degree to which a particular part of the geometry contributes to the PDN input impedance is quantified. A rigorous physics-based circuit model developed from the cavity model can associate an inductance with each current segment on a via and the power plane, which is used to extract the inductance contribution from different blocks of the geometry using circuit reduction. The physics-based circuit model is validated using different commercial products in [13], [14] and [15] with simulation and measurements.

The geometry, current path and inductance segmentation are detailed in Section II to lay the physics foundation of the approach. Two critical inductances are analysed in the paper. The IC interconnect inductance is analyzed in Section III. Formulations and design values for the IC interconnect inductance are presented herein for quick design estimations. The mutual inductances within the IC interconnect region are extracted to develop the guidelines on using the geometry characteristics to reduce the IC interconnect inductance faster. The equivalent inductance from IC to decaps is studied in Section IV. Sensitivity analysis and the variation of the equivalent inductance with geometry is presented. The percentage of different inductance components in the equivalent inductance is detailed to illustrate the effectiveness of design guidelines.

II. Geometry and Inductance Segmentation

A schematic drawing of a high-layer count PCB PDN geometry is shown in Fig. 1(a) with decaps placed on the top layer, on the bottom layer away from the IC, and on the bottom layer under the IC. The stack-up shown in Fig. 1(a) is a representative figure to show one type of a high-layer count PCB with a single power layer. It can have many ground planes between GND3 and GND1, and GND4 and GND6. Signal layers are not shown. Here, h_2 is set to be a large value to represent the contribution of all layers between the power cavity and decaps on the outer layer of the PCB.

Two common current paths in the PDN geometry are observed based on the sensitivity analysis shown in [16], which lead to the generic PCB PDN input impedance shown in Fig. 1(b). There are two important inductances in the PDN impedance. The impedance in the middle-frequency range of approximately a megahertz to tens of megahertz is dominated by the equivalent inductance of the current path from the IC to decaps through the power net

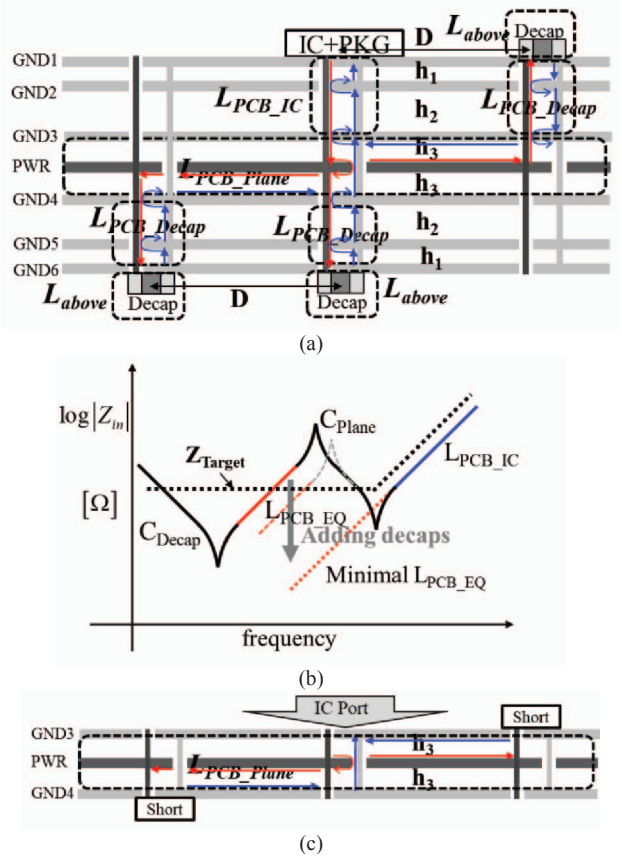


Fig. 1. (a). A stack-up of a high-layer count PCB PDN geometry, and the definitions of the inductances associated with the PCB PDN geometry. Decap to IC distance is D. (b). Generic PCB PDN input impedance. (c) L_{PCB_Plane} extraction settings.

area fill (the power plane is referred to as power net area fill since it can be irregular shape with many voids and plane is more of solid shape) and back to the IC through vias and ground planes as seen in Fig. 1(a). The inductance associated with this current path is denoted herein as the PCB equivalent inductance L_{PCB_EQ}. The PCB PDN impedance in the high-frequency range above approximately tens of megahertz to the hundreds of megahertz is dominated by the current path from the IC to the power plane and back to the IC through displacement current in the inter-plane capacitance of the power and ground planes, without passing through the decaps. The inductance associated with this current path is denoted as the IC interconnect inductance L_{PCB_IC}.

The L_{PCB_EQ} current path can be divided into four parts, the IC interconnect inductance L_{PCB_IC}, the decap interconnect inductance L_{PCB_Decap}, the plane inductance L_{PCB_Plane} (the port and short settings are shown in Fig 1(c) to extract L_{PCB_Plane} based on the cavity model), and the inductance above the topmost or bottommost ground plane L_{above}, as shown in Fig. 1(a). The current density between the vias with different distance provides physics support to the segmentation [17]. The current path in the L_{PCB_Decap} region is from the power cavity to the decaps and back to the ground layers through the decap ground vias. The current path in the L_{PCB_Plane} is from the IC to the decaps across the power net area fill with the return path from the decaps to the IC through the ground planes in the power cavities. L_{above} includes the inductance from the decap body, traces, vias, pads and the coupling between decaps to the nearest ground plane. L_{above} is treated as a short and not analyzed in this paper since it was detailed in [18]. The assumption of the segmentation is that there is little or no coupling between the blocks. The mutual inductance between the current segments in the IC and decap regions between GND1 to GND3, and GND4 to GND6 in Fig. 1(a) is neglected, as decaps are not typically placed very close to the IC due to routing constraints, and current concentrates in each region since there are ground vias nearby. The mutual inductance between IC and decap regions in the power cavity (between GND3-PWR- GND4) is taken into account and considered as a part of L_{PCB_Plane}. Then, the L_{PCB_EQ} can be expressed as the summation of the four parts, as,

$$L_{PCB\_EQ} = L_{PCB\_Decap} + L_{PCB\_IC} + L_{PCB\_Plane} + L_{above} \quad (1)$$

III. L_{PCB_IC} Modeling, Formulation, and Analysis

L_{PCB_IC} depends on the stack-up, IC pin map pattern, and number of IC pins. Several IC pin map patterns are studied in this section to analyze the L_{PCB_IC}. An analytical formulation is proposed to calculate L_{PCB_IC} and a unit cell approach is presented for fast L_{PCB_IC} approximation.

Several IC pin patterns are used herein to represent common IC pin maps. The IC pin map patterns are defined as row, alternating, grid and hexagonal according to the relative locations of the power and ground vias, as shown in Fig. 2. The power and ground vias are placed in rows in the row pattern, and are placed in an alternating direction in the alternating pattern to take advantage of the mutual inductance between the power and ground vias. In the grid pattern, there are four ground vias around every power via, as shown in the cross shape in red. There are extra vias (circled in blue) added around the alternating pattern. For hexagonal patterns, the relative locations of power and power-return vias are different with two or three power vias in a line, as shown using the blue arrow in Fig. 2 (d) and Fig. 2 (e). The placement patterns of row, alternating, and hexagonal has the ratio of power to ground vias as 1:1. The pitch size for the IC pins considered here is 1 mm.

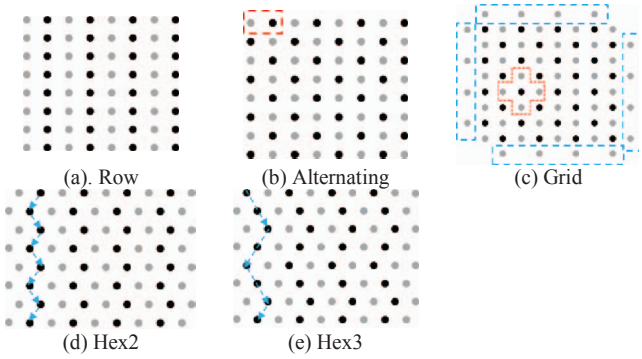


Fig. 2. IC pin patterns, (a) Row pattern, (b) Alternating pattern, (c) Grid pattern, (d) Hex2 pattern with 2 power vias in a line, and, (e) Hex3 pattern with 3 power vias in a line.

A. Circuit reduction and rigorous L_{PCB_IC} formulation

L_{PCB_IC} is extracted from the cavity model [19]-[23] based on the circuit reduction shown in Fig. 3. The port is set to be on the top layer in the IC region. The short is set on GND3 where the vias in the IC region reaches the power cavity. The settings maintains the current path in the L_{PCB_IC} region. The physics-based circuit model with a one-to-one correspondence to the geometry in Fig. 3 (a) is shown in Fig. 3 (b). Series reduction is performed on the inductors connected in series from Fig. 3 (b) to Fig. 3 (c). Since the inductance is proportional to the cavity thickness, L_{PCB_IC} can be scaled to total thickness of different cavities. Then, all power vias can be merged into a single power via, and all ground vias can be merged into a single ground via with parallel reduction, as shown from Fig. 3 (c) to Fig. 3 (d). The effective inductance after parallel reduction can be represented mathematically as

$$L_{Group} = \left(\sum_{columns} \sum_{rows} \left[\mathbf{L}_{Group} \right]^{-1} \right)^{-1}. \quad (2)$$

Here, L_{Group} is the L_{ij} matrix of the inductors connected in parallel and is calculated using cavity model. After reducing all power vias to be one power inductor and all ground vias to be one ground inductor, the L_{ij} matrix after reduction for the circuit shown in Fig. 3 (d) can be written as

$$\mathbf{L}_{PCB\_IC} = \begin{bmatrix} L_{PWR} & L_{PWR\_GND} \\ L_{GND\_PWR} & L_{GND} \end{bmatrix} \quad (3)$$

Here, L_{PWR} is the self-inductance of the single power via merged from all power vias in series and in parallel, L_{GND} is the self-induc-

tance of the single ground via merged from all ground vias. L_{PWR_GND} is the mutual inductance between the ground via and the power via. Then L_{PCB_IC} can be calculated as

$$L_{PCB\_IC} = L_{PWR} + L_{GND} - 2L_{PWR\_GND} \quad (4)$$

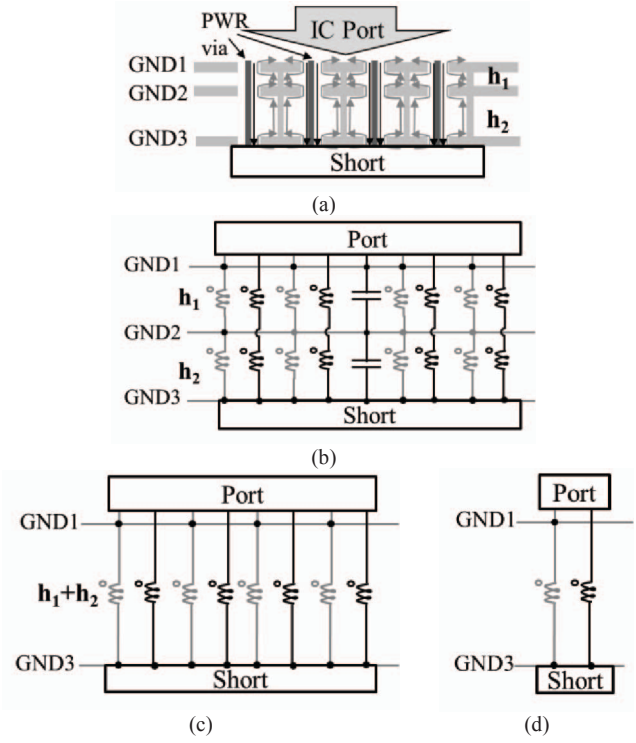


Fig. 3. (a). Geometry for L_{PCB_IC}. (b). The physics-based circuit model for L_{PCB_IC}. (c). The circuit after series reduction. (d). The circuit after parallel reduction.

The L_{PCB_IC} modeling results with a total cavity thickness of 49 mils are shown in Fig. 4. Here, since there can be many ground planes between GND1 and GND3 in a high-layer count PCB PDN stack-up, the total thickness can be large. The thickness of 49 mils is used to represent such a scenario. The 1/n curve is calculated as the L_{PCB_IC} from a pair of power and ground vias (circled in red in Fig. 2 (b)) divided by the number of IC pins to represent the change of L_{PCB_IC} by adding the IC pins in parallel without considering the mutual inductances between the vias. The 1/nCell curve is calculated by the L_{PCB_IC} of a cell with one power surrounded by four ground vias (circled in red in Fig. 2 (c)), divided by the number of IC pins. The two curves form the upper and lower bound to the rigorously calculated curves. The mutual inductance between pairs/cells is not included in the upper and lower bound curves. When the number of IC pins is small, the grid pattern is close to the 1/nCell curve and the other cases are close to the 1/n curve. With an increasing number of IC pins, the L_{PCB_IC} of all patterns becomes closer. The row placement pattern is used to validate the L_{PCB_IC} extraction. The L_{PCB_IC} of the row placement from rigorous calculation matches well with that from the CST simulation, as shown in TABLE I. The IC pin number is set to be large so that L_{PCB_IC} is small in the validation to demonstrate the accuracy of first-principles cavity-model formulation.

TABLE I
L_{PCB_IC} [pH] FOR THE ROW PATTERN, WHEN THE DRILL DIAMETER IS 8 MILS, ANTI-PAD DIAMETER IS 16 MILS, PITCH IS 1MM, AND THE THICKNESS FROM THE IC TO THE POWER CAVITY IS 40 MILS

IC power pin #	Rigorous Calculation	CST
72 (6 rows by 12 cols)	12.3	12.5
200 (10 rows by 20 cols)	4.2	4.1

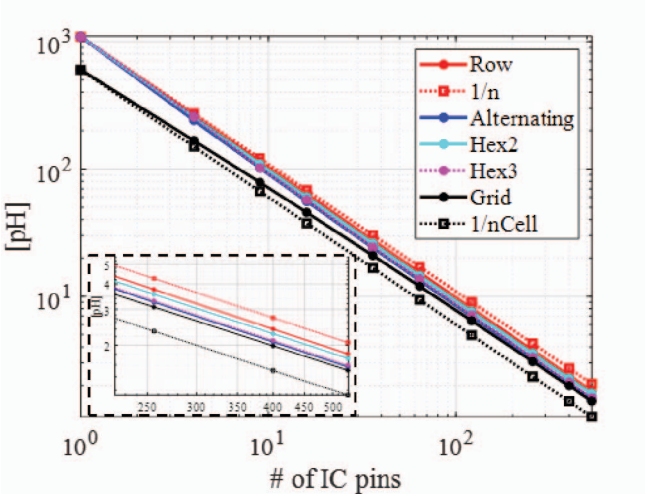


Fig. 4. L_{PCB_IC} comparison for the IC pin patterns shown in Fig. 2.

B. Quick estimation of L_{PCB_IC}

The unit-cell approach can be used to analyze the inductance contribution in L_{PCB_IC}. The unit cell for the grid pattern is one power via surrounded by four ground vias, as shown in Fig. 5. The return current for the power via mostly concentrates on the nearby ground vias. A similar approach can be extended to other IC pin patterns. Thus, L_{PCB_IC} can be calculated as

$$L_{PCB\_IC} = h\left(\frac{L_{unitcell\_PUL}}{n_{ICpin}} + M_{unitcell\_PUL}\right). \quad (5)$$

Here, since the inductance from the cavity model is proportional to the thickness, a per unit length (PUL) can be extracted to generalize the formulation. The first term in (5) represents the 1/nCell or 1/n calculation. The second term $M_{unitcell\_PUL}$ represents the mutual inductance between pairs/cells.

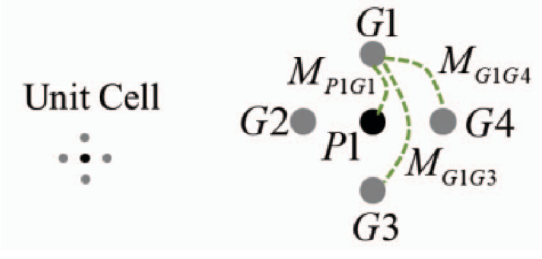


Fig. 5. Unit cell definition in the grid IC pin placement pattern and the via names.

By applying KCL and KVL, the unit cell L_{PCB_IC} is calculated from

$$j\omega\begin{bmatrix} L_{P1} & M_{P1G1} & M_{P1G2} & M_{P1G3} & M_{P1G4} \\ M_{P1G1} & L_{G1} & M_{G1G2} & M_{G1G3} & M_{G1G4} \\ M_{P1G2} & M_{G1G2} & L_{G2} & M_{G2G3} & M_{G2G4} \\ M_{P1G3} & M_{G1G3} & M_{G2G3} & L_{G3} & M_{G3G4} \\ M_{P1G4} & M_{G1G4} & M_{G2G4} & M_{G3G4} & L_{G4} \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix}. \quad (6)$$

Assuming that $I_{G1}=I_{G2}=I_{G3}=I_{G4}=-I_{P1}/4$, and $V_{IC}=V_1-V_2$, $V_2=V_3=V_4=V_5$, the PUL unit cell L_{PCB_IC} can be calculated as

$$L_{unitcell\_PUL,Gird} = L_{P1} + \frac{L_{self,GND}}{4} - 2M_{PG} + \frac{M_{GG1}}{2} + \frac{M_{GG2}}{4}, \quad (7)$$

Here, I_{IC} is the current going in to the port. L_{P1} is the self-inductance of the power via. L_{Gi} is the self-inductance of the i^{th} ground via, i=1,2,3,4. M_{PiGj} is the mutual inductance of the i^{th} power via and j^{th} ground via. M_{GiGj} is the mutual inductance of the i^{th} ground via and j^{th} ground via. V_i, I_i are the voltage and current for the i^{th} via. V_{IC} is the voltage across the unit cell. By solving the matrix, the L_{PCB_IC} of the unit cell is calculated with the assumption $M_{GG1}=M_{G1G4}=M_{G1G2}=M_{G2G3}=M_{G3G4}$, and $M_{GG2}=M_{G1G3}=M_{G2G4}$, $L_{self,GND}=L_{G1}=L_{G2}=L_{G3}=L_{G4}$, $M_{PG}=M_{P1G1}=M_{P1G2}=M_{P1G3}=M_{P2G4}$. The mutual inductance impact is clear in this formulation. The inductance $L_{P1}+L_{self,GND}/4$ is the self-inductance of the unit cell, and the term $(-2M_{PG}+M_{GG1}/2+M_{GG2}/4)$ gives the mutual inductance contribution for L_{PCB_IC} within the unit cell. Similarly, the L_{PCB_IC} of the unit cell for the other cases of IC pin patterns with one pair of power and ground vias is calculated as

$$L_{unitcell\_PUL,PG} = L_{self,PWR} + L_{self,GND} - 2M_{PG}. \quad (8)$$

The mutual inductance between the pairs/cells for different IC pin patterns is shown in Fig. 6. For the grid pattern, the power via is surrounded by ground vias and the current carried by the neighbouring ground vias is along the same direction, which leads to the positive mutual inductance between cells. But for row, alternating and hexagonal patterns, there are vias carrying currents in opposite directions between power and ground vias among neighbouring pairs, which leads to the negative mutual inductance between the pairs. As the number of IC pins increases, the mutual inductance decreases, since more parallel paths are added. In addition, since the first term in (5) decreases faster than the second term, the percentage of the mutual inductance between cells/pairs in L_{PCB_IC} increases with the increase of IC pins. When the number of IC pins increases from 9 to 529, the percentage of mutual inductance between the cells/pairs in L_{PCB_IC} increases from 6% to 13.9% for the row pattern, and from 18.7% to 31.8% for the alternating pattern.

L_{PCB_IC} is bounded by the 1/n and 1/nCell curves from Fig. 4. When the IC pin number is over 100, L_{PCB_IC} is below 10 pH with h_1+h_2=49 mils for all the IC pin patterns. Thus, it is usually very small for a PDN design using a large number of IC vias for power. The 1/n and 1/nCell curves can be used directly to approximate L_{PCB_IC} with the relative error around 2.9% ~ 32%. The larger error happens when the number of IC pins is large and L_{PCB_IC} is small. To improve accuracy and retain a fast calculation, another approximation can be used with a combination of 1/n and 1/nCell curves, as shown in TABLE II. The maximum relative error can be reduced to less than 20%. The benefit of using an approximation is to avoid complex formulas using cavity model, and enable simple estimation of L_{PCB_IC} using a simple formula with design tables during the PDN design stage, with acceptable accuracy.

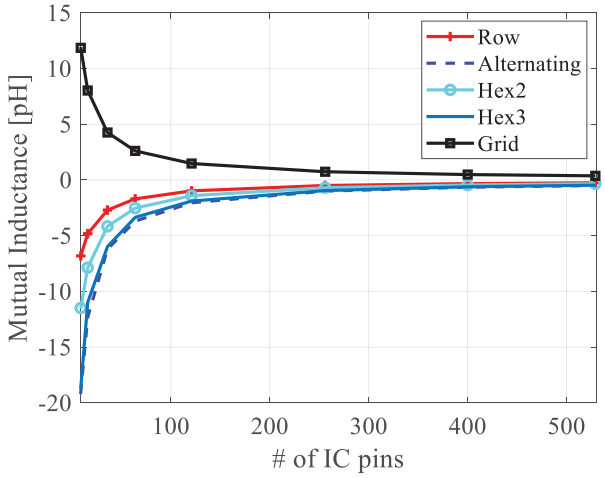


Fig. 6. Mutual inductance contribution between the cells or pairs.

TABLE II
FAST APPROXIMATION OF L_{PCB_IC} FOR THE RESULTS IN FIG. 4

IC pin pattern	# of IC pin <16	# of IC pin >=16	Relative Error
Row	$h\frac{L_{unitcell\_PUL,PG}}{n_{ICpin}}$		2.9% ~ 13.8%
Alternating, Hex3	$h\frac{L_{unitcell\_PUL,PG}}{n_{ICpin}}$	$h\frac{\left(L_{unitcell\_PUL,PG}+L_{unitcell\_PUL}\right)}{n_{ICpin}}$	0.3%~ 18.7%
Hex2	$h\frac{L_{unitcell\_PUL,PG}}{n_{ICpin}}$	$h\frac{\left(L_{unitcell\_PUL,PG}+L_{unitcell\_PUL}\right)}{n_{ICpin}}$	8.1%~ 12.3%
Grid	$h\frac{L_{unitcell\_PUL}}{n_{ICpin}}$	$h\frac{\left(L_{unitcell\_PUL,PG}+L_{unitcell\_PUL}\right)}{n_{ICpin}}$	3.1% ~16%

The per-unit-length L_{PCB_IC} for the unit pair/cell depends on the pitch size and drill size. Some commonly used pitch sizes, drill sizes and anti-pad sizes are listed in TABLE III. The L_{PCB_IC} for 1 mil thickness with the unit power-ground (PG) pair/cell is listed in TABLE IV. The two tables can be used with TABLE II for quick L_{PCB_IC} estimation in different PDN geometries.

TABLE III
IC PIN VIA DESIGN WITH DIFFERENT PITCH SIZES AND VIA-PADSTACK SIZES

Pitch Size	Drill (Diameters)	Anti-pad (Diameters)
1 mm	8 mils	20 mils
	10 mils	30 mils
	12 mils	32 mils
0.8 mm	8 mils	20 mils
	12 mils	20 mils
0.5mm	8mils	20mils

TABLE IV
L_{PCB_IC} [PH/MIL] FOR THE PG PAIR AND UNIT CELL

Pitch [mm]	Drill [mils]	PG pair, formula (8)	CST	Grid unit cell formula (7)	CST
1	8	24.5	24.0	13.5	12.9
	10	22.2	21.8	12.1	11.5
	12	20.4	20.0	11.0	10.2
0.8	8	22.0	21.8	12.0	11.3
	12	17.9	17.3	9.5	8.6
0.5	8	17.4	16.6	9.1	8.3

IV. L_{PCB_EQ} Modelling Results and Analysis

L_{PCB_EQ} is influenced by the stack-up, IC pin pattern, IC pin number, number of decaps, decap location, decap layout, decap package size and decap to IC distance. Sensitivity analysis and the variation of L_{PCB_EQ} with geometry details are studied to illustrate the impact of the number of decaps, the distance from the decap to the IC, and the thickness from the decaps to the power cavity on L_{PCB_EQ} in this section. The connection between the geometry and the inductance is illuminated as well. The limiting factors of the decap effectiveness in different design scenarios are identified. With such information, a systematic approach to analyze and improve the PDN design is proposed. Fundamental reasoning behind design guidelines and the effectiveness of each guideline can be explained.

The PCB stack-up shown in Fig. 1(a) is used to investigate different PCB designs in this section. The values for h_1, h_2 and h_3 used are 9mils, 40mils (since many ground planes can be added between GND1 and GND3, GND4 and GND6) and 9mils, respectively. The IC pin map used in this section is the grid pattern with 36 power pins. Decaps are placed using a doublet layout, as shown in Fig. 7 (a). In the doublet layout, two decaps are placed in pairs with power and ground vias placed as close as possible in alternating directions. The decaps are added in pairs as a line around the IC on the top layer, as shown in Fig. 7 (b). For other common decap placements, the analysis can follow the same approach shown here, since the current paths in PCB PDN are generic.

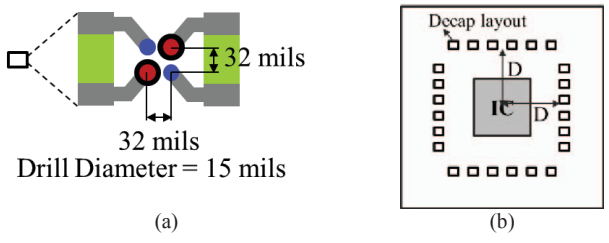


Fig. 7. (a) Doublet layout for decap placement. (b) Adding decaps around the IC with center-to-center distance D with each square representing the doublet layout in (a).

The L_{PCB_EQ} change with the number of decap pairs is shown in Fig. 8. Here, there is not enough room to add 32 pairs of decaps when D=500 mils. The L_{PCB_EQ}, and, in particular the L_{PCB_plane} component increases with an increase of the distance between the decaps and the IC, since a larger D increases the length of the current path from the IC to the decaps. The L_{PCB_EQ} reduction rate decreases with an increase in the number of decaps. When the number of decaps is small, here from one pair to four pairs, the reduction rate by adding decaps is rapid. Adding decaps is very effective in this region. In addition, the L_{PCB_EQ} reduction rate is much faster when the thickness from the decap to the power cavity is large (h_1+h_2=49mils), which means adding decaps to reduce the PDN impedance is effective when the power cavity is buried deep in the stack-up because L_{PCB_Decap} is dominant. When the number of decaps is large, here from eight pairs to 16 pairs or 32 pairs, the reduction in L_{PCB_EQ} is small. Adding decaps is not as effective in reducing the PDN impedance in this region, because L_{PCB_Decap} becomes smaller relative to L_{PCB_plane}+ L_{PCB_IC}.

The effectiveness of adding decaps is related to the dominant inductance component in L_{PCB_EQ} [24]. When h_1+h_2 is large and the number of decaps is small, the dominant component in L_{PCB_EQ} is L_{PCB_Decap}. The rapid reduction of L_{PCB_Decap} by adding more decaps leads to the fast reduction in L_{PCB_EQ}. With more decaps added, L_{PCB_Decap} continues to decrease until the dominant component in L_{PCB_EQ} changes to L_{PCB_Plane}. The L_{PCB_EQ} reduction rate then slows down. When h_1+h_2 is small, the dominant component is L_{PCB_plane}, and the L_{PCB_EQ} reduction rate is slower by adding decaps, as shown in Fig. 8. In both scenarios when L_{PCB_plane} is or becomes the dominant inductance component in L_{PCB_EQ}, adding decaps is not as effective in reducing the PDN impedance as the scenario when L_{PCB_Decap} is dominant. To summarize, adding decaps is more effective in decreasing the PDN impedance when L_{PCB_Decap} is the dominant component. The details of the inductance decomposition are discussed further in Section A below.

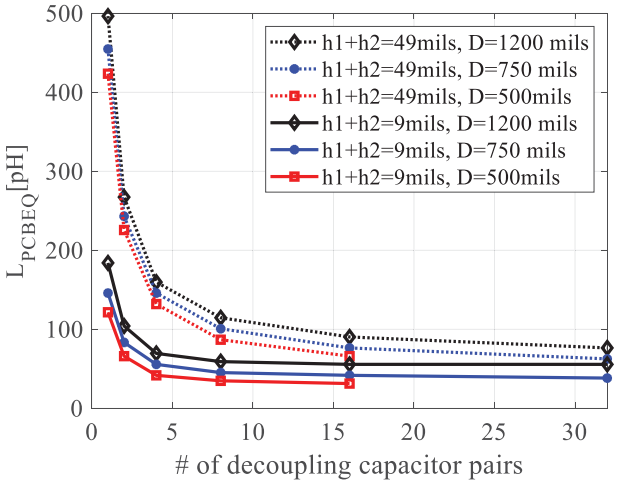


Fig. 8. L_{PCB_EQ} change with the number of decap pairs, distance (D) between the decap and the IC, and different thickness (h_1+h_2) from the decap to the power net area fill. Decaps are placed on the top layer.

Analysis of the inductance components is performed to illustrate the change in L_{PCB_EQ} with a design change, and illuminate how each design guidelines works in different design scenarios. The variation of L_{PCB_EQ} with geometry details is also performed to understand the relationship of L_{PCB_EQ} with the number of decaps, the thickness from the decaps to the power cavity, and the distance between the decaps and the IC. In this section, a special case with decaps placed under the IC is also analyzed.

A. L_{PCB_EQ} analysis

Inductance decomposition is performed in this section to identify the limiting factors for PDN designs. The L_{PCB_Decap} and L_{PCB_plane} percentage in L_{PCB_EQ} related to the number of decaps, the distance between the IC and decaps, and the thickness from the decaps to the power cavity, is shown in Fig. 9. Here decaps are

treated as a short and Labove is not included. The L_{PCB_IC} percentage range in L_{PCB_EQ} is 3% -19% depending on the number of decaps added. The L_{PCB_Decap} percentage decreases as the number of decaps increases because of the increasing decap parallel paths, and the L_{PCB_plane} percentage increases with an increasing number of decaps. The rate of reduction of the L_{PCB_Decap} percentage by adding decaps is faster than the rate of increase of the L_{PCB_plane} percentage, which indicates L_{PCB_Decap} is more sensitive to the increase in the number of decaps here. When h_1+h_2=49 mils for the case when power layers are buried deep in the board, and the number of decaps is small (1-8 pairs), L_{PCB_Decap} is a large fraction of L_{PCB_EQ}, and has a dominant impact on the PDN impedance. With a larger number of decaps, the percentage of L_{PCB_Decap} decreases and L_{PCB_plane} becomes the dominant portion in L_{PCB_EQ} after eight pairs of decaps are added. When h_1+h_2=9mils, the power layers are close to the IC. Then, L_{PCB_plane} is the dominant component in L_{PCB_EQ} and dominates the PDN impedance, and adding decaps only contributes incrementally in reducing the PDN impedance, at which point further decaps are relatively ineffective.

The effectiveness of best practice design guidelines is directly related to the percentage of L_{PCB_Decap} and L_{PCB_plane} in L_{PCB_EQ} and the impact on the PDN impedance. The number of decaps, the thickness from the decap to the power cavity, the via locations in the decap footprint impacts L_{PCB_Decap}, and the distance from the IC to the decaps impacts L_{PCB_plane}, all contributing to L_{PCB_EQ}, and the resulting PDN input impedance. Together, it leads to a changing effectiveness of design guidelines in PDN design practice. One design guideline can be effective in a certain design, and be less effective in another. Eventually it depends on which inductance component is dominant in L_{PCB_EQ}, and if the design guideline contributes to reducing the dominant inductance component. An analysis of the L_{PCB_Decap} and L_{PCB_plane} percentage in L_{PCB_EQ} illuminates the design guidelines impacts on the PDN impedance.

The limiting factor of the decap effectiveness can be identified through the inductance components in L_{PCB_EQ}. When the thickness from the decaps to the power cavity is large, the limiting factor is the decap interconnect inductance L_{PCB_Decap}, which is up to 70% of L_{PCB_EQ} when there are many decaps (and parallel paths) as seen in Fig. 9. Adding decaps can reduce the equivalent inductance and PDN impedance rapidly. When the number of decaps added becomes sufficient such that the limiting factor changes to L_{PCB_plane}, the effectiveness of adding more decaps is reduced, which is seen in Fig. 8. To further reduce L_{PCB_EQ}, design approaches to reduce L_{PCB_plane} must be used, such as placing the decaps closer to the IC, or reducing the thickness of the power cavity, depending on design and manufacturing flexibility. When the total layer thickness h_1+h_2 from the decaps to the power cavity is small, the limiting factor of the decap effectiveness is L_{PCB_plane}. Adding decaps is less effective, as shown in Fig. 8. Moving the decaps closer to the IC or reducing the thickness of the power cavity to reduce L_{PCB_plane} is more effective in reducing L_{PCB_EQ}.

The limiting inductance portion is identified by breaking down L_{PCB_EQ} to the inductance pieces along the current path. Whether a particular design adjustment can effectively reduce the PDN impedance for a given design can be easily quantified and simulated based on the inductance change for every block. Engineers can quickly make design decisions such as when adding more decaps is more effective, or when moving the power layer toward the IC is more effective. In addition, with the ability to extract each inductance component using the cavity model, or other fast approximations, the improvement for any design change can be predicted with fast and accurate calculations to provide design feedback. The result is a systematic PDN analysis approach to guide the PDN design and shorten the design cycle.

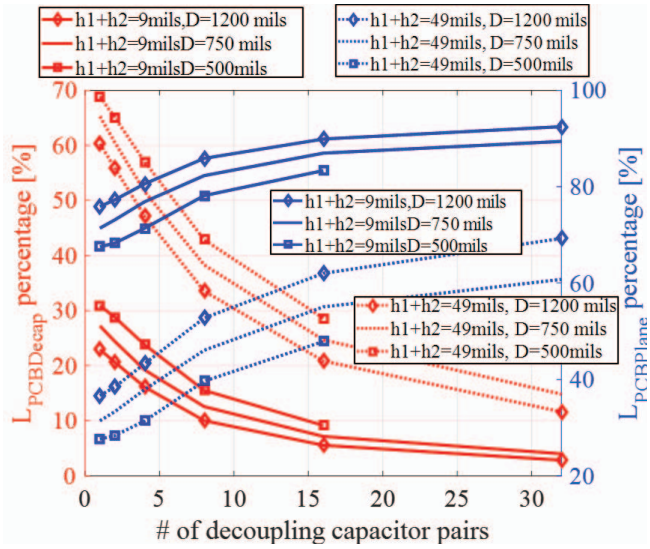


Fig. 9. L_{PCB_Decap} and L_{PCB_Plane} percentage in L_{PCB_EQ} with the number of decaps, the decap to power cavity thicknesses h_1+h_2, and, the distance D between decaps and IC. Decaps are placed on the top layer.

B. L_{PCB_EQ} variation with geometry

The L_{PCB_EQ} variation with the thickness from the decaps to the power cavity (h_1+h_2) is shown in Fig. 10. The distance between the decaps and the IC is 1200 mils. Decaps are added in a line on the four sides symmetrically around the IC incrementally. When there are only a few decaps, increasing the thickness h_1+h_2 results in a rapid increase in L_{PCB_EQ}, since L_{PCB_Decap} increases proportionally with the thickness and L_{PCB_plane} remains the same, since h_3 and D are unchanged. The slope for L_{PCB_EQ} when the number of decap pairs is four is larger than that when the decap pairs is 64. Using inductance decomposition, when the number of decap pairs is small, such as four decap pairs, the L_{PCB_Decap} percentage changes from 16% to 47.4% when h_1+h_2 changes from 9 mils to 49 mils. The same percentage changes from 1.6% to 6.5% when there are 64 decap pairs. From this analysis, the PDN design with the power layer buried deep in the stack-up is more sensitive to the number of decaps used in the design, and adding more decaps can reduce the PDN impedance.

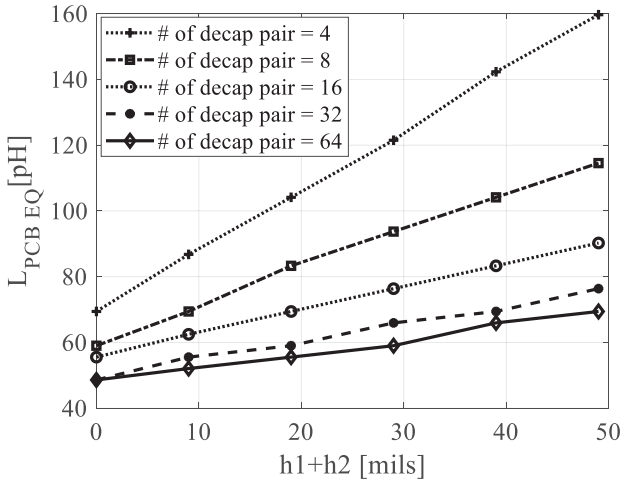


Fig. 10. L_{PCB_EQ} change with the thickness from the decaps to the power cavity. Decaps are placed on the top layer of the PCB.

The percentage increase of L_{PCB_EQ} with D for different thickness h_1+h_2 with different number of decaps added is shown in Fig. 11. The percentage increase is defined as the increase in L_{PCB_EQ} when D is larger than 500 mils normalized to the L_{PCB_EQ} when D is 500 mils, as

$$\underset{\text{percentage}}{L_{PCB\_EQ}\ \text{increase}} = \frac{\left(L_{PCB\_EQ}(D>500mils) - L_{PCB\_EQ}(D=500mils)\right)}{L_{PCB\_EQ}(D=500mils)}. \quad (9)$$

The L_{PCB_EQ} increase with D is related to the L_{PCB_Plane} percentage in L_{PCB_EQ}. The larger the portion L_{PCB_Plane} takes in L_{PCB_EQ}, the more sensitive L_{PCB_EQ} will be to the increase of D, such as the scenarios when h_1+h_2 is small or the number of decaps is large. The number of decaps, and the thickness from the decaps to the power cavity changes L_{PCB_Decap}, which impacts L_{PCB_EQ} to change the L_{PCB_Plane} percentage. The power cavity thickness, the distance between the decaps and IC, the decap layout and number, the IC pin pattern and the number IC power pins influences L_{PCB_Plane} directly. When only D increases and the other parameters remain fixed, increasing D increases L_{PCB_Plane}, and L_{PCB_EQ} becomes more sensitive to the increase of D. From Fig. 11, when the number of decaps is small, e.g., one or two pairs of decaps; the increasing percentage with the increase of D is small. When there are more decaps, e.g., eight or 16 pairs, the increasing percentage with the increase of D is large. The reason is that L_{PCB_Plane} percentage becomes larger by adding more decaps as the result of the fast decrease of L_{PCB_Decap}, as shown in Fig. 8 and Fig. 9. Also, when the thickness from the decaps to the power cavity is small (h_1+h_2=0), the percentage increase is much larger than that when the thickness is large (h_1+h_2=49 mils). The reason is that the L_{PCB_Decap} is proportional to the thickness h_1+h_2. Increasing the thickness from the decaps to the power cavity increases L_{PCB_Decap}, and decreases the percentage of L_{PCB_Plane}. Here, there is a jump of L_{PCB_EQ} increase percentage when the decap pairs changes from four pairs to eight pairs for h_1+h_2=49 mils. It reflects the dominant inductance component switch from L_{PCB_Decap} to L_{PCB_Plane} by adding decaps. In summary, L_{PCB_EQ} is more sensitive to the increase of D when L_{PCB_Plane} is a larger portion of L_{PCB_EQ}.

A straightforward design improvement to lower the PDN impedance can be guided by minimizing the dominant inductance component in L_{PCB_EQ}. When L_{PCB_Decap} is the dominant component, changing the layer of the power net area fill to be closer to the outer layer on which the decaps are located, or adding more decaps, are effective in lowering the PDN impedance. While moving decaps closer to the IC is not as effective in this case, since this impacts only L_{PCB_Plane}. Specifically, when the power layer is closer to the top layer in the stackup, decaps should be added to the top layer. Otherwise decaps should be added to the bottom layer when the power layer is closer to the bottom layer. When the power layer is in the middle, decaps can be added either on the top layer or the bottom layer. When a large thickness from the decap to the power cavity is unavoidable in the design, adding enough decaps is more critical to lower L_{PCB_Decap} and maintain a low L_{PCB_EQ} value. More decaps are needed to compensate for the inductance increase due to the thickness h_1+h_2. A special design scenario is when L_{PCB_Decap} is the dominant component, the distance from the decaps to the IC does not have much impact on L_{PCB_EQ}, which means decaps can be placed anywhere to increase the routing flexibility. When L_{PCB_Plane} is the dominant component, the effectiveness of adding decaps is reduced. To minimize L_{PCB_Plane}, moving the decaps closer to the IC or using a thin layer thickness for the power cavity are better and more effective solutions. To summarize, the change of the effectiveness of design guidelines can be determined through the analysis of dominant component in L_{PCB_EQ}. To reduce the PDN input impedance, the guidelines that can reduce the dominant inductance component should be implemented in the design.

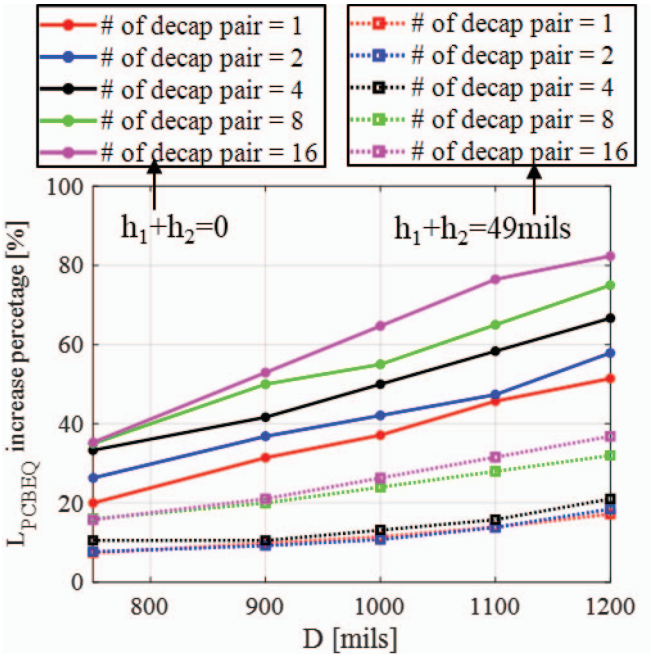


Fig. 11. L_{PCB_EQ} percentage increase (normalized to the L_{PCB_EQ} when D=500mils) with the distance from the decaps to the IC. Decaps are placed on the top layer.

C. Decaps under the IC

A special case is adding decaps under the IC. The current does not need to cross the power net area fill horizontally. The current comes directly from the IC power pins to power net area fill, and is redistributed to go to the power vias that are connected to the decaps, reaches the decaps through the vias, and comes back using the nearby ground vias and planes. Depending on the number of decaps added, not all the IC vias are used as decap interconnect vias. Adding more decaps adds more parallel current paths in the decap interconnect region, and reduces L_{PCB_Decap}. The L_{PCB_IC} and L_{PCB_decap} percentage in L_{PCB_EQ} with different number of decaps under the IC is shown in Fig. 12. Here, the number of IC power pins is 400. When there are few decaps, L_{PCB_EQ} is large and is dominated by L_{PCB_Decap}, since there are few parallel current paths in the L_{PCB_Decap} region. When more decaps are added, L_{PCB_Decap} is reduced, which leads to the increase percentage of L_{PCB_IC} in L_{PCB_EQ}. When decaps are added to all the power pins in the IC region, the total number of vias used are the same as that in the IC interconnect region. L_{PCB_Decap} calculation becomes the same as L_{PCB_IC} calculation. Then, L_{PCB_IC} estimation method can be used to estimate L_{PCB_EQ}. The limit of adding decaps under the IC can be estimated using formulas and design tables provided in Section III. In Fig. 12, the L_{PCB_Plane} percentage is not plotted. When decaps are added for all IC pins, L_{PCB_Decap} and L_{PCB_IC} is over 85% of L_{PCB_EQ} with the other 15% from the current redistribution through the power cavity. Consequently, the PDN design in this scenario is limited by the IC pin map and the thickness of the board. In most designs, since adding decaps under the IC does not require additional vias or space, which would compromise signal routing channels, it is the first choice of decap locations.

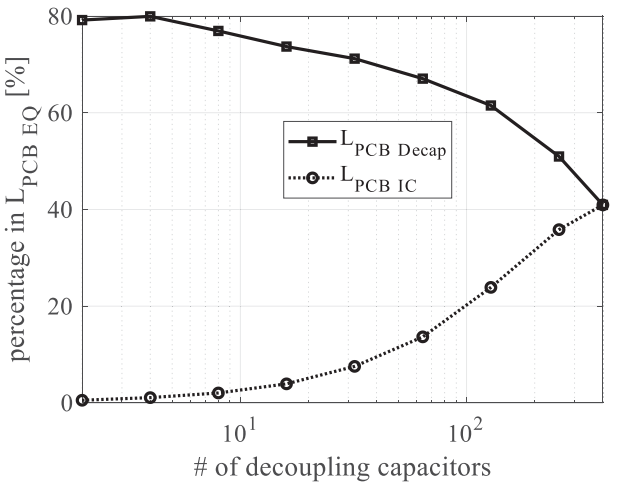


Fig. 12. L_{PCB_IC} and L_{PCB_Decap} percentage with the number of decaps when the decaps are placed on the bottom layer under the IC with h_1+h_2=49mils.

V. Conclusion

Current and inductance in PCB power delivery networks is analyzed to understand the impact on the PDN input impedance. A systematic approach using inductance decomposition is proposed herein to obtain a complete understanding of the PDN layout geometry impacts on PDN impedance. Design scenarios are discussed. Two critical components in the PDN impedance are studied according to the two current paths. The inductance from the IC to the power-net area fill, denoted L_{PCB_IC}, is quantified using the formulas from the cavity model, and quick estimation for L_{PCB_IC} of common IC power pin pattern layouts are presented. The mid-frequency range to a few tens of megahertz for PCB PDN behaviour is also presented herein. The L_{PCB_Decap} and L_{PCB_Plane} percentage in L_{PCB_EQ} is analyzed to understand the effectiveness of best practice design guidelines. The geometry impacts on the L_{PCB_EQ} are illustrated and the limiting factors for decap effectiveness are identified. With a complete understanding of PDN behaviour, design insight and guidelines can be developed. The proposed method can be extended to complex systems.

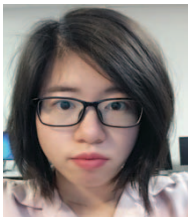
The current paths in PCB PDN provides the insights to guide the PCB PDN designs. Depending on different designs with different stack-ups and the number of power planes, the current paths can be different. For stack-ups with multiple power layers, a similar analysis can be performed using the approach proposed here. The only difference would be that the interactions between different current paths and components need be treated carefully using the same current tracking method and inductance decomposition [13], [17]. In addition, the formulations included here are based on the cavity model. If the power shape is not well defined with lots of voids, and the current path from the IC to the decaps is largely impacted by the power shape, which can increase L_{PCB_Plane}, other modeling methods or simulations can be used to extract L_{PCB_Plane} [13]. For the stagged via, the horizontal connections in the "dog-bone" geometry is not included in the inductance extraction [25]. Full-wave simulations can be used to substitute the inductance components extraction with the port settings included in the paper to increase accuracy. The analysis and design of PDN can still follow the proposed method.

References

1. I. Novak, "Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination," IEEE Transactions on Advanced Packaging vol. 22, pp. 274-283, Aug. 1999.
2. W. D. Becker, J. Eckhardt, R. W. Frech, G. A. Katopis, E. Klink, Michael F. McAllister, T. G. McNamara, P. Muench, S. R. Richter, and H. Smith, "Modeling, simulation, and measurement of mid-frequency simultaneous switching noise in computer systems," in IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 21, pp. 157-163, May 1998.
3. A. Waizman and C. Chung, "Resonant free power network design using extended adaptive voltage positioning (EAVP) methodology," in IEEE Transactions on Advanced Packaging, vol. 24, no. 3, pp. 236-244, Aug 2001.
4. R. Senthinathan, and J. L. Prince. Simultaneous switching noise of CMOS devices and systems. Springer Science & Business Media, 2013.
5. B. Garben, M. F. McAllister, W. D. Becker, and R. Frech, "Mid-frequency delta-I noise analysis of complex computer system boards with multiprocessor modules and verification by measurements," IEEE Trans. Adv. Packag., vol. 24, pp. 294–303, Aug. 2001.
6. W. D. Becker, H. Harrer, A. Huber, W. L. Brodsky, R. Krabbenhoft, M. A. Cracraft, D. Kaller, G. Edlund, and T. Strauch, "Electronic Packaging of the IBM

z13 processor drawer," IBM J. Res. & Deve., vol 59, no.4/5, pp. 740-741. Aug. 2015.
7. K. Jaemin, W. Lee, Y. Shim, J. Shim, K. Kim, J. So Pak, and J. Kim, "Chip-Package hierarchical power distribution network modeling and analysis based on a segmentation method," in IEEE Transactions on Advanced Packaging, vol. 33, no. 3, pp. 647-659, Aug. 2010.
8. L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," IEEE Transactions on Advanced Packaging, , vol. 22, pp. 284-291, 1999.
9. J. Kim, S. Wu, H. Wang, Y. Takita, H. Takeuchi, K. Araki, F. Gang, and F. Jun, "Improved target impedance and IC transient current measurement for power distribution network design," 2010 IEEE International Symposium on Electromagnetic Compatibility (EMC), Fort Lauderdale, FL, USA, 25-30 July 2010, pp. 445-450.
10. M. Swaminathan, and E. Engin. Power integrity modeling and design for semiconductors and systems. Pearson Education, 2007.
11. L. D. Smith, and E. Bogatin. Principles of Power Integrity for PDN Design--Simplified: Robust and Cost Effective Design for High Speed Digital Products. Prentice Hall, 2017.
12. K. Shringarpure, Pan, S., Kim, J., Achkir, B., Archambeault, B., Fan, J., Drewniak, J., " Innovative PDN design guidelines for practical high layer-count PCBs," DesignCon2013, Santa Clara, CA, USA, pp. 1290-1314.
13. B. Zhao, S. Bai, S. Connor, W. D. Becker, M. Cocchini, J. Cho, A. Ruehli, B. Archambeault, J. Drewniak, "Physics-Based Circuit Modeling Methodology for System Power Integrity Analysis and Design", IEEE Transactions on Electromagnetic Compatibility, Early Access, July, 2019.
14. K. Shringarpure, S. Pan, J. Kim, J. Fan, B. Achkir, B. Archambeault, and J. L. Drewniak. "Formulation and network model reduction for analysis of the power distribution network in a production-level multilayered printed circuit board." IEEE Transactions on Electromagnetic Compatibility 58, no. 3, pp 849-858, Jun. 2016.
15. X. Fang, S. Bai, S. Liang, B. Zhao, "A Two-Port Measurement With Mechanically Robust Handhold Probes for Ultra Low PDN Impedance", 2019 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), New Orleans, LA, USA, July 22-26, 2019.
16. K. Shringarpure, B. Zhao, L. Wei, B. Archambeault, A. Ruehli, M. Cracraft, M. Cocchini, E. Wheeler, J. Fan, J. Drewniak., "On finding the optimal number of decoupling capacitors by minimizing the equivalent inductance of the pcb pdn," In 2014 IEEE International Symposium on Electromagnetic Compatibility (EMC), Raleigh, NC, USA, 4-8 Aug. 2014, pp. 218-223.
17. B. Zhao, S. Bai, C. Huang, J. Fan, A. Ruehli, J. Drewniak, H. Ye, E. Li, B. Achkir, B. Archambeault, S. Connor, M. Cracraft, M. Cocchini, "Surface current distribution for PCB PDNGeometry." In Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Seoul, South Korea , 14-16 Dec. 2015, pp. 113-116.
18. S. Yang, Y. S. Cao, H. Ma, J. Cho, A. E. Ruehli, J. L. Drewniak, and E. Li. "PCB PDN prelayout library for top-layer inductance and the equivalent model for decoupling capacitors." IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 6, pp.1898-1906, Dec. 2018.
19. B. Zhao, S. Bai, S. Connor, M. Cecchini, D. Becker, M. Cracraft, A. Ruehli, B. Archambeault, and J. Drewniak. "System Level Power Integrity Analysis with Physics-Based Modeling Methodology." In 2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI), Long Beach, CA, USA, July 30 – Aug 3, 2018, pp. 379-384.
20. T. Okoshi, Planar Circuits for Microwaves and Lightwaves: Springer-Verlag 1984.
21. Y. T. Lo, W. Solomon, and W. F. Richards, "Theory and experiment on microstrip antennas," IEEE Trans. Antenna Propag., vol. AP-7, no. 2, pp. 137–145, Mar. 1979.
22. R. Sorrentino, "Planar circuits, waveguide models and segmentation method," IEEE Trans. Microw. Theory Tech., vol. MTT-33, no. 10, pp. 1057–1066, Oct. 1985.
23. G. T. Lei, R. W. Techentin, and B. K. Gilbert, "High-frequency characterization of power/ground-plane structures," IEEE Trans. Microw. Theory Tech., vol. 47, no. 5, pp. 562–569, May 1999.
24. Y. Fan, B. Zhao, S. Liang, S. Connor, M. Cocchini, B. Achkir, S. Scearce, J. Drewniak, "Equivalent Inductance Analysis and Quantification for PCB PDN Design", 2019 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), New Orleans, LA, USA, July 22-26, 2019.
25. J. Cho, S. Bai, B. Zhao, A, Ruehli, J. Drewniak, M. Cocchini, S. Connor, M. A. Cracraft, and D. Becker. "Modeling and analysis of package PDN for computing system based on cavity model." In 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Washington, DC, USA, Aug. 7-11,2017, pp. 213-218.

Biographies



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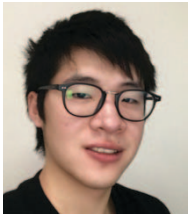

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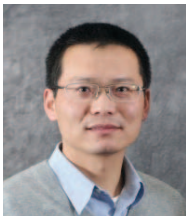

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