Investigating Substrate Loss in MEMS Acoustic Resonators and On-Chip Inductors

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***Abstract*— This work studies the influence of substrate loss on the performance of acoustic resonators and on-chip inductors and investigates the effective substrate resistivity of seven commonly used substrates in silicon-based devices. The substrates include X-cut lithium niobate ($LiNbO_3$) film with two different thicknesses (400 nm and 1.6 μm) on high-resistivity Si (HR-Si) and amorphous Si wafers, SiO_2 film with two different thicknesses on HR-Si, and bare HR-Si. The effective resistivities of these substrates are extracted using coplanar waveguides (CPWs) over a frequency range from 1 to 40 GHz. Using the effective resistivity approach, the efficiency of two substrate loss reduction techniques—Si wafer removal and amorphous Si—in reducing substrate loss is quantified. Comparison of the extracted substrate resistivities of the suspended and un-suspended dielectric-on-Si structures and comparison of $LiNbO_3$ on HR-Si and amorphous Si are carried out. Substrate loss reduction techniques are more advantageous for a thinner dielectric film and at a lower frequency range due to the higher filling factor of the electric field in the Si wafer. Finally, by comparison of the effective substrate resistivity of SiO_2 film on an HR-Si with bare HR-Si, thick plasma-enhanced chemical vapor deposition (PECVD) SiO_2 film is found to be a good insulation layer to reduce substrate loss.**

***Index Terms*— Coplanar waveguide, effective resistivity, lithium niobate, microelectromechanical systems (MEMSs), millimeter-wave devices.**

I. Introduction

With the expansion of 5G communication, the lower radio spectrum becomes increasingly crowded for various usage scenarios. For this reason, applications need to scale to the 5G high band, where more bandwidth is available. However, the high-band counterparts have degraded performance due to increased loss at high frequency. Degraded performance of an RF front-end filter, an indispensable component in telecommunication, results in higher passband insertion loss and deteriorated frequency selectivity. By understanding the loss mechanism, one could improve the device performance and thus enhance front-end capabilities.

For 5G handheld applications, miniaturization of front-end components is essential. More than 100 filters are arrayed in a phone to support an increasing number of functions [1]. Miniature filters at 5G high band are still under development to meet stringent sizes. Microelectromechanical system (MEMS) acoustic filters have shown strong potential due to their compact dimensions, pervasiveness at RF, and low manufacturing cost. Tremendous research efforts have been invested in frequency scaling of acoustic resonators for 5G applications in the past 20 years. Acoustic devices using surface acoustic wave (SAW) resonators and film bulk acoustic wave resonators (FBARs) are indispensable RF front-end components in 4G communication. It has been demonstrated that these acoustic devices could be scaled to 5G bands using various piezoelectric materials, including aluminum nitride (AlN), lithium tantalite ($LiTaO_3$), and lithium niobate ($LiNbO_3$) [2]–[9]. Frequency-scaling of SAW resonators requires a reduction in the lateral dimensions, which increases the metal loss in the electrodes and is limited by the resolution of the lithography process. Among the state-of-the-art SAW devices, 3.5 GHz is the highest operating frequency, which comes with the price of having an electrode periodicity of 550 nm [3], [4]. On the other hand, frequency-scaling of FBAR requires a reduction in piezoelectric film thickness, and excessive reduction leads to poor film quality. As a result, the resonant frequencies of state-of-the-art FBARs are limited to sub-6 GHz [6], [8], [9]. Besides SAW resonators and FBARs, MEMS resonators on $LiNbO_3$ thin film have been demonstrated with resonant frequencies over 10 GHz while maintaining high quality factor (Q) and compact footprint [10], [11]. An MEMS resonator with a 3-μm feature size using antisymmetric Lamb wave overmodes in a 400-nm-thick Z-cut $LiNbO_3$ thin film with the 13th-order overmode (A13) resonates at 55.7 GHz and has a mechanical Q of 340, which promises an excellent resonator platform to enable miniature filters [11].

One of the major challenges faced by MEMS acoustic filters is the narrow passband. The bandwidth of an acoustic filter is fundamentally determined by the electromechanical coupling k_t^2, whereas k_t^2 ($\sim 1/f^2$) is roughly proportional to one over frequency square in the overmode scaling process [10]. A previously demonstrated MEMS filter using the 3rd-order antisymmetric Lamb wave mode (A3) has a fraction

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bandwidth (FBW) of only 0.7% at 10.9 GHz [12]. To tackle this issue, hybrid acoustic filters with on-chip inductors have been proposed as a solution [13], [14]. Hybrid filters exploiting the 5th- and 7th-order antisymmetric modes on a 650-nm-thick Z-cut $LiNbO_3$ film and operating at 14.7 and 19 GHz have been demonstrated to boost the FBW by five times that of their acoustic-only counterparts [14]–[16].

Due to the low inductor quality factor at high frequencies, the previous demonstrations of hybrid filters suffer from high passband insertion loss. An inductor on suspended $LiNbO_3$ film with a peak Q of 35 at 7 GHz only has a Q of 8 at 19 GHz, which results in a passband insertion loss of 8 dB for the hybrid filter at 19 GHz [14]. As will be shown in detail in Section II of this article, substrate loss is the major contributor to the low inductor Q at high frequency, which increases fast with frequency. To maintain low loss when scaling RF front-ends to 5G high band, substrate loss has to be mitigated. Despite the importance of $LiNbO_3$ film for MEMS acoustic filters, its substrate loss has not been characterized yet.

The parasitic surface conduction (PSC) effect is known to occur in oxide-on-Si structures, which severely increases substrate loss [17]–[19]. Free carriers are attracted and accumulate at the interface between the oxide and Si because of the existence of fixed charges in the oxide layer [20], [21]. The effective resistivity of a fully processed high-resistivity silicon-on-insulator wafer has been shown to be an order of magnitude lower than the nominal value of an HR-Si [20]. The introduction of a trap-rich passivation layer at the interface has been proven to be an efficient method to eliminate the PSC effect, which effectively traps the free carries at the interface. The trap-rich techniques include ion implantation [22], [23], and deposition of an amorphous Si or polycrystalline silicon thin film on HR-Si [24].

As a result of high substrate loss at high frequency, acoustic resonators and on-chip inductors have low quality factors, which significantly deteriorate the filter performance and cause high passband insertion loss and narrow bandwidth. By understanding and characterizing the loss mechanism and contributors to the substrate loss intrinsic to the device structure, the filter performance could be improved. In this work, the substrate loss of three types of dielectric-on-Si structures with two different dielectric film thicknesses is experimentally quantified and compared with a bare HR-Si wafer. The dielectric-on-Si substrate involves $LiNbO_3$ film on HR-Si, $LiNbO_3$ film on amorphous Si, and SiO_2 film on HR-Si. In addition to studying the influence of dielectric film thickness on substrate loss, the efficiency of substrate loss reduction through the Si removal process is quantified. Finally, the relationship between on-chip inductor quality factor and substrate loss is experimentally studied.

II. Influence of Substrate Loss on Resonator and Inductor Quality Factors

A. MEMS Resonator Quality Factor

In the nonideal condition, substrate loss increases R_0 in the static branch in the modified Butterworth–van Dyke (MBVD) model of an acoustic resonator. The substrate loss in an MEMS resonator can be modeled by an equivalent series resistance (ESR) in the standard model of a capacitor [25]

$$R_0 = \text{ESR} \approx \frac{\tan\delta}{\omega C_0} = \frac{1}{\omega^2 C_0 \rho \epsilon} = \frac{1}{\omega^2 C_0 \epsilon_0 \rho_{\text{eff}} \psi} \tag{1}$$

$$\psi = \frac{1 + q\left(\epsilon_{r,\text{eff}} - 1\right)}{q} \tag{2}$$

where ϵ and ρ are the permittivity and the resistivity of the parallel plate equivalent of the interdigital electrode structure of an MEMS resonator, respectively; C_0 is the static capacitance of the resonator; ω is the angular frequency. For a nonuniform substrate, the inhomogeneous bottom substrate could be modeled as an equivalent effective homogeneous substrate with uniform resistivity ρ_{eff} and relative permittivity $\epsilon_{r,\text{eff}}$. q is the filling factor of the electric field in the effective substrate; ϵ_0 is the permittivity of vacuum. ψ is a factor determined by the substrate permittivity and device structure.

In Fig. 1(a), admittances of an acoustic resonator with a mechanical Q of 1000 on a substrate with different $\psi\rho_{\text{eff}}$s of 10^3 and 10^5 $\Omega\cdot$ cm are plotted. For an MEMS acoustic resonator with a high figure-of-merit, the series resonance of the resonator is determined mainly by the motional branch (consisting of R_m, L_m, and C_m in the MBVD model), which experiences minimal influence from substrate loss. The resonator's anti-resonance, on the other hand, is a parallel resonance that is controlled by both the motional branch and the static branch (consisting of R_0 and C_0 in the MBVD model), which is influenced by substrate loss. The 3-D surface plot and contour plot of the resonator's anti-resonance quality factor Q_{anti} are plotted against substrate $\psi\rho_{\text{eff}}$ and resonator mechanical quality factor Q_m in Fig. 1(b) and (c), respectively. Q_{anti} is defined as the ratio between the anti-resonant frequency and 3-dB bandwidth of the anti-resonance of the admittance response. At radio frequency, Q_m of a typical MEMS acoustic resonator is usually larger than 100; as seen from Fig. 1(b), the contribution from Q_m to Q_{anti} increases with an increasing $\psi\rho_{\text{eff}}$. In the contour plot, it is observed that when $\psi\rho_{\text{eff}}$ is smaller than 10^3 $\Omega\cdot$ cm, the resonator Q_{anti} is strongly influenced by substrate loss. With a substrate $\psi\rho_{\text{eff}}$ of 10^3 $\Omega\cdot$ cm, a resonator with Q_m of 100 and 1000 would only have a loaded Q_{anti} of 21.4 and 22.2, respectively.

B. On-Chip Inductor Quality Factor

The effective substrate resistivity not only affects the acoustic resonators' Q_{anti}s but also results in deteriorated on-chip inductor quality factors (Q_{tot}s) at high frequencies. The nonideal substrate isolation results in a leakage resistance in parallel with the parasitic capacitance C_p, which is transformed into a series equivalent parasitic resistance R_p in the circuit model of an inductor shown in the inset of Fig. 2(a). R_p equals the ESR in (1), with C_0 replaced by C_p. The inductive branch of the circuit model consists of an inductance L and a metal resistance (R_S). Under the condition that the inductor cross-sectional dimension is much larger than the skin depth, the metal resistance can be approximated by

$$R_s \approx \frac{l}{\sigma_{\text{metal}} C_{\text{cross}} \delta} \tag{3}$$

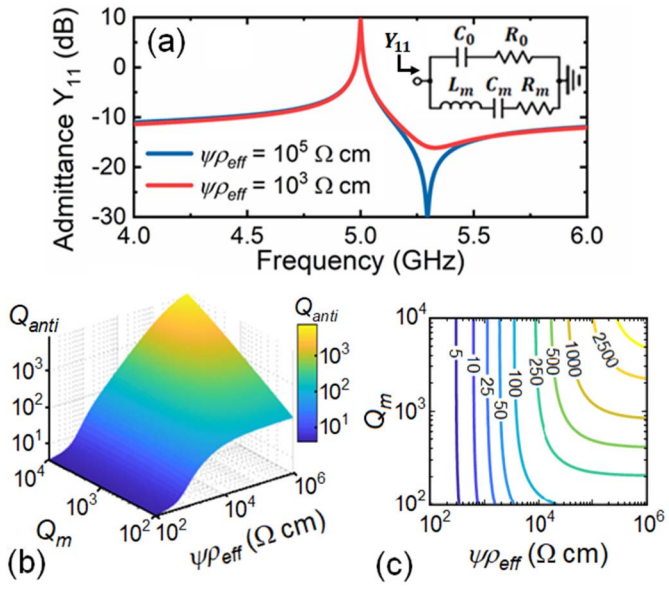


Fig. 1. (a) Admittance of the MBVD circuit model of an acoustic resonator (in the inset) with substrate $\psi\rho_{\text{eff}}$ of 10^3 and 10^5 Ω·cm. (b) Three-dimensional surface plot and (c) contour plot of the resonator quality factor at anti-resonance (Q_{anti}) with substrate $\psi\rho_{\text{eff}}$ varying from 10^2 to 10^6 Ω· cm and resonator mechanical Q (Q_m) varying from 10^2 to 10^4.

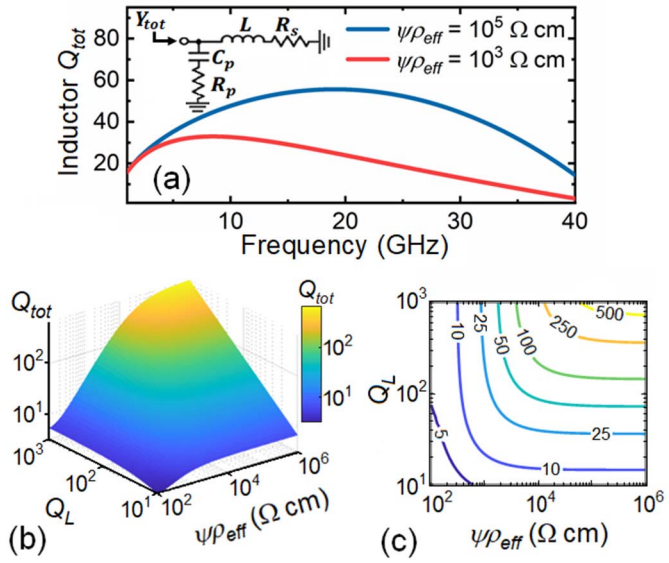


Fig. 2. (a) Inductor Q_{tot} of the equivalent circuit model of an inductor (in the inset) with substrate $\psi\rho_{\text{eff}}$ of 10^3 and 10^5 Ω· cm. (b) Three-dimensional surface plot and (c) contour plot of the inductor quality factor (Q_{tot}) at 24 GHz with substrate $\psi\rho_{\text{eff}}$ varying from 10^2 to 10^6 Ω·cm and quality factor of the inductive branch Q_L varying from 10 to 10^3.

where σ_{metal} is the metal conductance, δ is the skin depth, l is the wire length of the inductor, and C_{cross} is the circumference of the inductor cross section.

The quality factor of an on-chip inductor on a substrate with $\psi\rho_{\text{eff}}$s of 10^3 and 10^5 Ω· cm (with inductance $L = 0.54$ nH, parasitic capacitance $C_p = 25$ fF, and metal conductivity $\sigma_{\text{metal}} = 1.46 \times 10^7$ S/m) is plotted in Fig. 2(a). At low frequencies, substrate loss has little influence on inductor Q_{tot}, whereas the influence becomes substantial at frequencies beyond 5 GHz.

With Q_L defined as the quality factor of the inductive branch of the circuit model (consisting of L and R_s), the 3-D surface plot and contour plot of the inductor Q_{tot} at 24 GHz with varying Q_L and $\psi\rho_{\text{eff}}$ are shown in Fig. 2(b) and (c), respectively. With the inductor parameters listed in the previous paragraph, Q_L equals 78 at 24 GHz. As a result, Q_L varying from 10 to 1000 is selected. Both the plots indicate that in the diagonal direction, the two variables have a balanced contribution to Q_{tot}. Q_L is dominating when substrate $\psi\rho_{\text{eff}}$ is larger than 10^5 Ω· cm, whereas the substrate effect is dominating when $\psi\rho_{\text{eff}}$ is smaller than 10^3 Ω· cm and Q_L is greater than 100.

With Q_C being the quality factor of the capacitive branch (consisting of C_p and R_p) in the circuit model of an inductor, from circuit analysis, the total quality factor Q_{tot} is related to Q_C and Q_L by the following expressions:

$$Q_{\text{tot}} = (1-\chi)Q_L - \chi Q_C \tag{4}$$

$$\chi = \frac{R_s\left(1+Q_L^2\right)}{R_s\left(1+Q_L^2\right)+R_p\left(1+Q_C^2\right)} \approx \frac{1}{1+A\cdot\rho_{\text{eff}}\psi\cdot\omega^{-\frac{3}{2}}} \tag{5}$$

$$A = \frac{l\sqrt{\mu}}{C_{\text{cross}}\sqrt{2\sigma_{\text{metal}}}}\cdot\frac{\epsilon_0}{L^2C_p} \tag{6}$$

where μ is the permeability. The approximation in (5) is under the condition of both Q_L^2 and $Q_C^2 \gg 1$. Q_C, Q_L, χ, and Q_{tot} versus frequency are plotted in Fig. 3. As χ increases with frequency, the destructive contribution of the capacitive branch to Q_{tot} increases with frequency. At a frequency high enough such that $(A\rho_{\text{eff}}\psi)^{-1}\omega^{(3/2)} \gg 1$, $1-\chi$ decays at $\omega^{-(3/2)}$, whereas Q_L only increases at $\sqrt{\omega}$, and the constructive contribution of the inductive branch to Q_{tot} decreases with frequency. This agrees with Fig. 3(c) when the frequency is larger than 10 GHz.

III. Effective Substrate Loss Extraction

A. Effective Substrate Resistivity

The effective resistivity method was first introduced by Lederer and Raskin [20], which characterizes the substrate loss of planar structures using coplanar waveguides (CPWs). The substrate loss is isolated from the conductor loss, which collaboratively contributes to the total loss in a coplanar waveguide. The contribution of loss contributors could be identified with a breakdown understanding of the total loss. The substrate loss of SiO_2 film on Si has been examined in some previous works [20], [26], but the substrate loss of $LiNbO_3$ film on Si has not been characterized thus far. This work studies the substrate loss of X-cut $LiNbO_3$ film on Si wafers using CPW structures.

The cross-sectional views of the CPW structures to be investigated in this work are shown in Fig. 4. The test structure is a CPW on a dielectric-on-Si substrate [shown in Fig. 4(a)]. The inhomogeneous substrate consisting of a dielectric film and a Si wafer is modeled with a homogeneous effective substrate in the effective resistivity approach, as illustrated in Fig. 4(b). The substrate ρ_{eff} can be extracted from the lumped-element circuit equivalent of a CPW structure, and

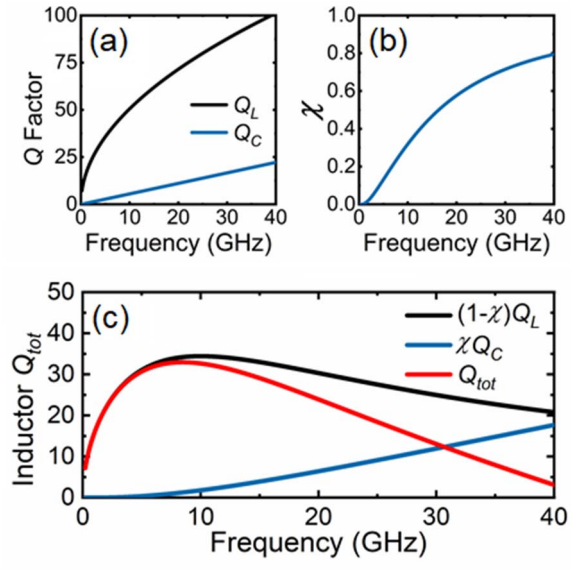


Fig. 3. (a) Quality factors of the inductive branch Q_L and capacitive branch Q_C of the equivalent circuit model of an inductor versus frequency. (b) χ factor versus frequency. (c) Total quality factor (Q_{tot}) of an inductor with weighted distribution from Q_L and Q_C with inductance $L = 0.54$ nH, parasitic capacitance $C_p = 25$ fF, metal conductivity $\sigma_{metal} = 1.46 \times 10^7$ S/m, and $\psi\rho_{eff} = 10^3$ Ω·cm.

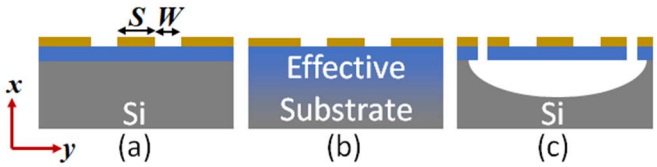


Fig. 4. Cross-sectional views of a coplanar waveguide on (a) dielectric film on Si (test structure), (b) effective homogeneous substrate, and (c) test structure after release (reference structure).

the expression is [20] and [27]

$$\rho_{\text{eff}} = q \cdot \frac{A}{d \cdot G_{\text{test}}} = q \cdot \frac{C_{\text{test}}}{\epsilon_0 \epsilon_{r,\text{test}}} \frac{1}{G_{\text{test}}} \tag{7}$$

$$q = q_1 + q_2 \tag{8}$$

where q, q_1, and q_2 are the filling factors of the electric field in the effective substrate, dielectric film, and Si wafer, respectively. C_{test} and G_{test} are the capacitance and conductance per unit length in the lumped-element equivalent circuit of the measured CPW test structure, respectively. A and d are the area and separation of a parallel plate equivalent to the CPW structure, respectively. $\epsilon_{r,\text{test}}$ is the relative permittivity of the test structure.

Electric field distribution in the inhomogeneous substrate is dependent on the physical dimension of the CPW: the width of the signal line (S) and the gap between the signal line and the ground plane (W), which, as a result, determines the filling factors of the electric field in the dielectric film (q_1) and Si wafer (q_2). The filling factors of the electric field could be theoretically modeled by the conformal mapping method [27], [28], and the dependence of q_1 on S and W is plotted in Fig. 5(a) and (b). The conformal mapping approach predicts an increase in S and W, as well as a decrease in dielectric

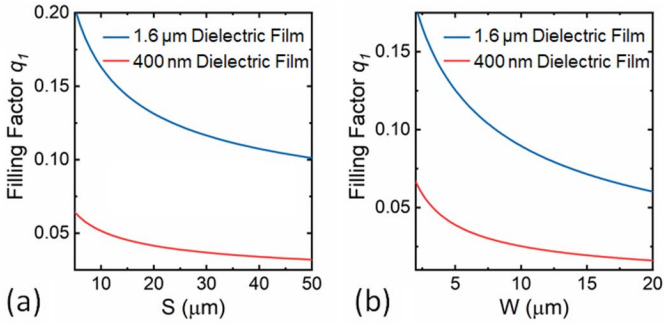


Fig. 5. Filling factor of electric field in the dielectric film (q_1) with (a) width of the signal line (S) of the CPW varying from 5 to 50 μm and (b) width of the gap between the signal line and ground plane (W) of the CPW varying from 2 to 20 μm.

TABLE I
DESIGN PARAMETERS OF THE VARIOUS CPWS

	Design I	Design II	Design III
Gap between signal and gnd (W)	4.5 μm	9 μm	15 μm
Width of signal line (S)	20 μm	40 μm	67 μm

film thickness. Both subsequently result in a lower q_1. As the physical dimension of the CPW influences the contribution from the two substrate materials to the total substrate loss of an inhomogeneous substrate, the effective resistivity is experimentally studied with three groups of CPW designs with different gap sizes while keeping the same S-to-W ratio. Detailed physical dimensions of the three designs are listed in Table I.

B. Si Wafer Resistivity

For the test structure shown in Fig. 4(a), the capacitance per unit length of the CPW (C_{test}) can be expressed by the permittivities and filling factors of the electric field in the two substrate materials

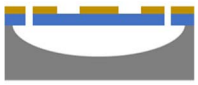
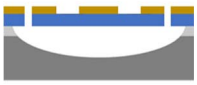
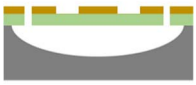
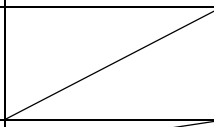
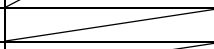
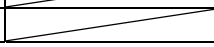
$$C_{\text{test}} = \epsilon_{r,\text{test}} C_{\text{air}} \tag{9}$$

$$\epsilon_{r,\text{test}} = 1 + q_1(\epsilon_{r,\text{diel}} - 1) + q_2(\epsilon_{r,\text{Si}} - 1) \tag{10}$$

where C_{air} is the capacitance per unit length of a CPW with the substrate in Fig. 4(b) replaced by air. $\epsilon_{r,\text{Si}}$ and $\epsilon_{r,\text{diel}}$ are the relative permittivity of Si wafer and dielectric film, respectively. Although $LiNbO_3$ is an anisotropic material, $\epsilon_{r,\text{LN}}$ for the samples with $LiNbO_3$ as the dielectric material in this work is approximated by 45. Because CPWs in this work are oriented along the z-axis of the X-cut $LiNbO_3$, the x- and y-components of $\epsilon_{r,\text{LN}}$ are both 45 in the cross section of CPW.

The reference structure is the test structure enabled by a release process to isotropically etch away Si. The central region of the CPW resides on a suspended dielectric film. According to a finite-element analysis performed on the reference structure using the high-frequency structure simulator (HFSS), when the release radius exceeds 100 μm, the contribution of the Si wafer after release to the effective relative

TABLE II
ILLUSTRATION OF THE STRUCTURES STUDIED AND THEIR SYMBOLS

		$LiNbO_3$ Film on Si	$LiNbO_3$ Film on α-Si	SiO_2 Film on Si	HR Si	HR Si (Type 2)
Unreleased	**Structure**					
	t_{diel} = 1.6 µm	LN1	LNα1	SO1	S1	S2
	t_{diel} = 400 nm	LN2	LNα2	SO2		
Released	**Structure**					
	t_{diel} = 1.6 µm	LN1R	LNα1R	SO1R		S2R
	t_{diel} = 400 nm	LN2R	LNα2R	SO2R		

permittivity of the reference structure ($\epsilon_{r,\text{ref}}$) is negligible. Consequently, the following formula describes the capacitance per unit length of the reference structure (C_{ref}):

$$C_{\text{ref}} = \epsilon_{r,\text{ref}} C_{\text{air}} \tag{11}$$

$$\epsilon_{r,\text{ref}} = 1 + q_1\left(\epsilon_{r,\text{diel}} - 1\right). \tag{12}$$

By subtracting the capacitance and conductance per unit length of the test structure from the reference structure, the resistivity of Si wafer (ρ_{Si}) is obtained

$$C_{\text{test}} - C_{\text{ref}} = q_2\left(\epsilon_{r,\text{Si}} - 1\right) C_{\text{air}} \tag{13}$$

$$\rho_{\text{Si}} = q_2 \cdot \frac{C_{\text{air}}}{\epsilon_0} \frac{1}{G_{\text{Si}}} = \frac{C_{\text{test}} - C_{\text{ref}}}{\epsilon_0\left(\epsilon_{r,\text{Si}} - 1\right)} \frac{1}{G_{\text{test}} - G_{\text{ref}}}. \tag{14}$$

This subtraction method avoids the inaccuracy caused by approximating q of the effective substrate by a constant in the traditional method. Furthermore, the test and reference structures in this study are identical CPW structures before and after Si wafer removal, which eliminates any inaccuracy caused by nonuniformity in the thicknesses of the dielectric film and electroplated Cu layer. This two-measurement method was previously used for extracting the dielectric constant and loss tangent of ferroelectric thin-film materials with high accuracy [29].

HFSS finite element analysis is used to validate the two substrate resistivity extraction methods. As illustrated in Fig. 6(a), a coplanar waveguide with 1-mm length is built on a substrate with a resistivity of 10 Ω· cm. Thru, Reflection, and Line standards for TRL calibration are also simulated in HFSS. After a TRL calibration, the simulated CPW performance is used to extract the substrate ρ_{eff} and plotted in Fig. 6(b). The subtraction method has much higher accuracy than the traditional method introduced in part A of this section due to the inaccuracy in assuming q by 0.5 in the conventional method. In addition, as TRL calibration is used, the extraction is accurate when the Line standard has an electrical length ranging from 20° to 160° [30]. As a result, a Line standard with a 1-mm length provides accurate results from

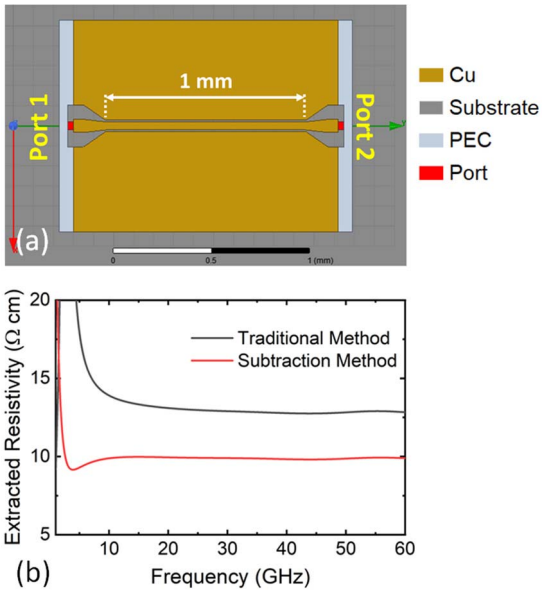


Fig. 6. (a) HFSS model of a coplanar waveguide of 1-mm length on a substrate with resistivity 10 Ω·cm. (b) Extracted substrate resistivity from HFSS simulation using the traditional and subtraction methods.

6.9 to 55 GHz. It agrees with the observation in Fig. 6(b) that the extracted ρ_{eff} by the substation method is accurate when frequency is higher than 6.9 GHz.

IV. MEASUREMENT RESULTS AND DISCUSSION

To examine the relationship between the substrate loss of dielectric-on-Si structures and dielectric film thicknesses, CPW designs are fabricated on $LiNbO_3$-on-Si and SiO_2-on-Si samples with different film thicknesses: 400 nm and 1.6 μm. The CPW designs are also fabricated on X-cut $LiNbO_3$ film on amorphous Si to quantify the substrate loss reduction from amorphous Si technology. The amorphous Si wafer used in this work consists of a 400-nm-thick amorphous Si deposited on a conventional high-resistivity Si wafer. Finally, the CPW

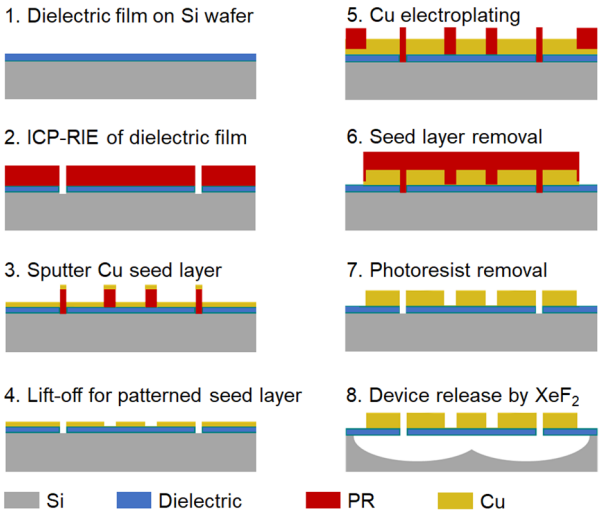


Fig. 7. Fabrication process of CPW on dielectric film on Si wafer.

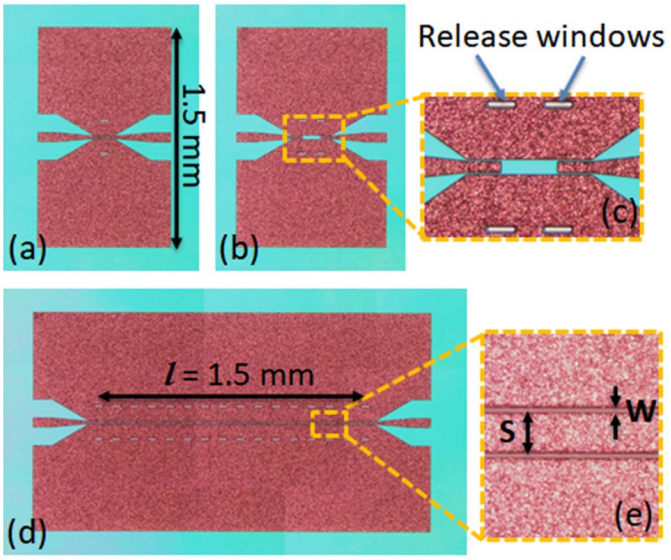


Fig. 8. Microscope image of the fabricated test structures with Design I: (a) Thru standard, (b) Reflection standard, (c) center region of the Reflection standard, (d) Line standard, and (e) center region of the Line standard.

designs are fabricated on bare HR-Si and SiO_2 on HR-Si to see which structure has less substrate loss at high frequency. Detailed illustrations of the substrate structures studied in this work and their symbols are listed in Table II, in which t_{diel} represents the thickness of the dielectric film.

A. Fabrication Process

The CPWs are fabricated with a four-mask process, which starts with a dielectric-on-Si wafer, as illustrated in Fig. 7. Inductively coupled plasma-reactive ion etching (ICP-RIE) is used to make release windows for the release process in the final step, and SPR220 photoresist (PR) is used as the mask. Due to the small feature size of CPW designs, the seed layer is patterned via a lift-off process. To reduce the conductor loss in CPW, the metal layer is thickened by Cu electroplating. The method of the patterned seed layer is important for Design I CPWs, as it avoids the narrow gap from merging during electroplating. After electroplating, in the seed layer removal step, the electroplated region is protected by a layer of PR and the sample is treated with Cu etchant. After PR removal using Aceton, the test structure is obtained and measured. The test structures are then etched by XeF_2 to produce the reference structures.

CPWs on the various substrates share the same fabrication process starting from step 3 in Fig. 7. The fabrication of X-cut $LiNbO_3$ samples starts from a transferred $LiNbO_3$ film on a Si wafer produced by NGK. Mixed ICP-RIE is used to etch $LiNbO_3$ for creating release windows. For SiO_2-film-on-Si samples, the first step is plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 film with a desired thickness (400 nm and 1.6 μm) on an HR-Si wafer, followed by Freon-based ICP-RIE of SiO_2 film with patterned SPR220 as a mask. Finally, for CPWs on a bare Si wafer, the fabrication process starts directly from step 3.

The microscopic images of the fabricated CPW structures before and after the release process are shown in Figs. 8 and 9. TRL calibration is applied to the measurement results of the CPW to remove any parasitic effect due to the probing pads,

TABLE III
FREQUENCY (GHz) WITH CPW LENGTHS CORRESPONDING TO QUARTER WAVELENGTH

	3 mm	2 mm	1.5 mm	1 mm	0.75 mm
400 nm $LiNbO_3$	10	15.3	22.6	30	40
1.6 µm $LiNbO_3$	9.2	13.8	20.7	27.6	36.8

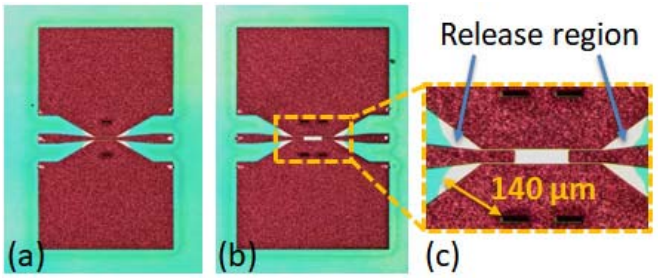


Fig. 9. Microscope images of the fabricated reference structures with Design I: (a) Thru and (b) Reflection standards, and (c) center region of the Reflection standard after the release process with a release radius of 140 μm.

which allows a high level of accuracy. As TRL calibration is the most accurate when the electrical length of the Line standard is close to 90°, CPWs with various lengths, ranging from 750 μm to 3 mm, are fabricated to extract ρ_{eff} over a frequency range from 1 to 40 GHz. The detailed lengths of the CPWs fabricated and the frequencies at which the CPW lengths correspond to a quarter wavelength are listed in Table III. The extracted resistivity is obtained by combining the extracted ρ_{eff} and ρ_{Si} in the selected frequency range of the CPW with various lengths.

From the measured *S*-parameters, the complex propagation constant and characteristic impedance of the transmission line could be derived, which is then converted into a

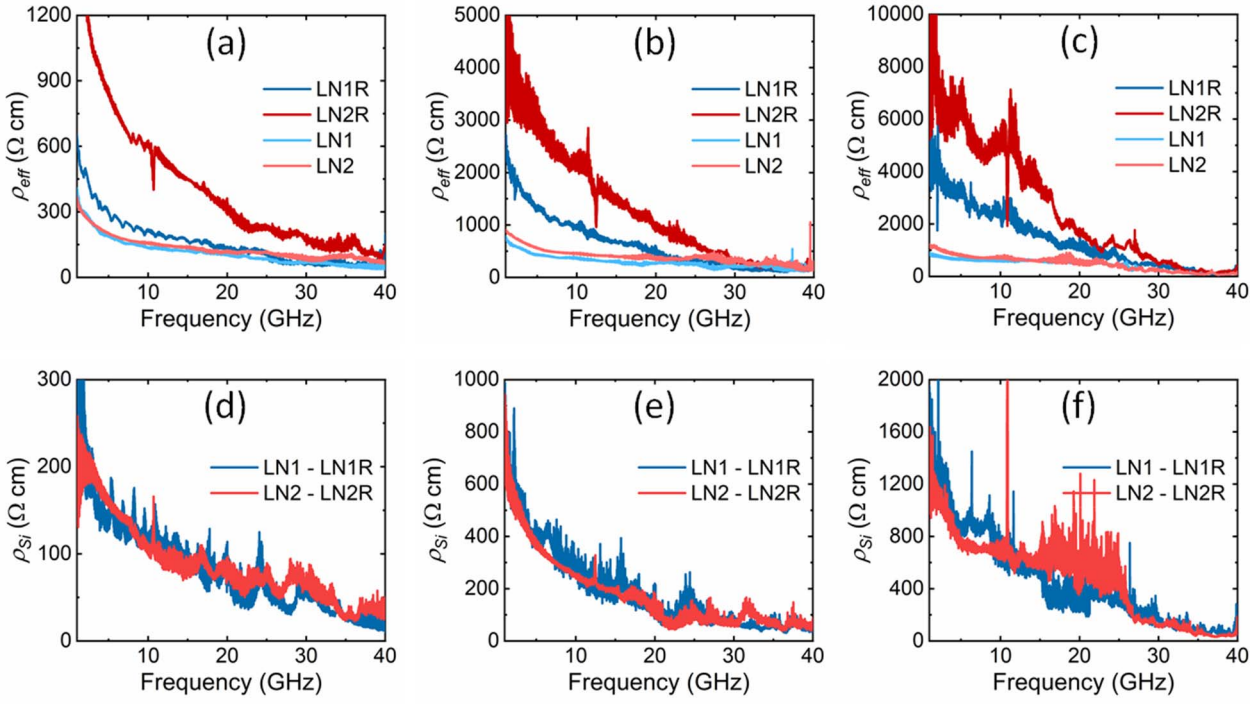


Fig. 10. Extracted (a)–(c) effective substrate resistivity (ρ_{eff}) of the released and unreleased structures and (d)–(f) Si wafer resistivity (ρ_{Si}) by the subtraction method from CPWs on X-cut $LiNbO_3$ film on high-resistivity Si with CPW Designs I, II, and III (physical dimensions listed in Table I), respectively.

TABLE IV
EXTRACTED EFFECTIVE SUBSTRATE RESISTIVITY (ρ_{EFF} IN Ω·cm) OF X-CUT $LiNbO_3$ ON Si BEFORE AND AFTER RELEASE AT 5 AND 24 GHz

	Frequency = 5 GHz			Frequency = 24 GHz		
	Design I	**Design II**	**Design III**	**Design I**	**Design II**	**Design III**
400 nm $LiNbO_3$ on Si (LN2)	200.6	569.2	859.5	112.1	361.4	414.4
400 nm $LiNbO_3$ (Released) (LN2R)	847.0	3263.1	6966.7	222.3	679.4	1297.9
1.6 µm $LiNbO_3$ on Si (LN1)	195.0	437.0	663.9	89.3	278.2	458.5
1.6 µm $LiNbO_3$ (Released) (LN1R)	298.9	1364.2	3295.4	116.3	314.1	783.2

lumped-element circuit equivalent [31]. After obtaining C_{test} and G_{test} of a test structure, as well as C_{ref} and G_{ref} of a reference structure from the lumped-element circuit equivalent, ρ_{eff} and ρ_{Si} are calculated using (7) and (14), respectively.

B. Comparison of Various Dielectric Thickness

The extracted ρ_{eff} of $LiNbO_3$ on Si structures from CPW Design I with two different $LiNbO_3$ thicknesses (400 nm and 1.6 μm) is plotted in Fig. 10(a). By comparing the extracted substrate ρ_{eff} before and after a release process, the effectiveness of substrate loss reduction from the Si wafer removal technique is quantified. This method has significant substrate loss reduction efficiency in the low-frequency range. As listed in Table IV, for the 400-nm $LiNbO_3$ sample, at 5 GHz, ρ_{eff} improves from 200.6 to 847 Ω· cm, by 4.2 times, whereas at 24 GHz ρ_{eff} only rises from 112.1 to 222.3 Ω· cm, by 1.98 times. In the lower frequency range, Si wafer has a high contribution to the unreleased structure substrate loss, but at higher frequencies, $LiNbO_3$ film is the major contributor.

Furthermore, for the thick-film structure, namely, 1.6-μm $LiNbO_3$, the reduction in substrate loss owing to Si removal is less substantial. At 5 GHz, ρ_{eff} for the 1.6-μm $LiNbO_3$ sample rises by just 1.5 times, from 195 to 298.9 Ω · cm, a substantially smaller improvement than the 4.2 times improvement for the 400-nm-thick $LiNbO_3$ sample. This is because the thicker $LiNbO_3$ film has a higher filling factor of the electric field, resulting in a greater contribution from $LiNbO_3$ film to substrate loss and consequently a lower contribution from Si wafer.

Using the subtraction method, the resistivities of Si wafer (ρ_{Si}s) in the two $LiNbO_3$ on Si samples are extracted from the measurement results and shown in Fig. 10(d). In the two samples with various $LiNbO_3$ film thicknesses, the contribution from Si wafer to substrate loss of the unreleased structure is comparable. $LiNbO_3$ film thickness does not influence the loss in Si wafer. The difference in ρ_{eff} between the two unreleased samples is mostly due to the difference in $LiNbO_3$ film thicknesses.

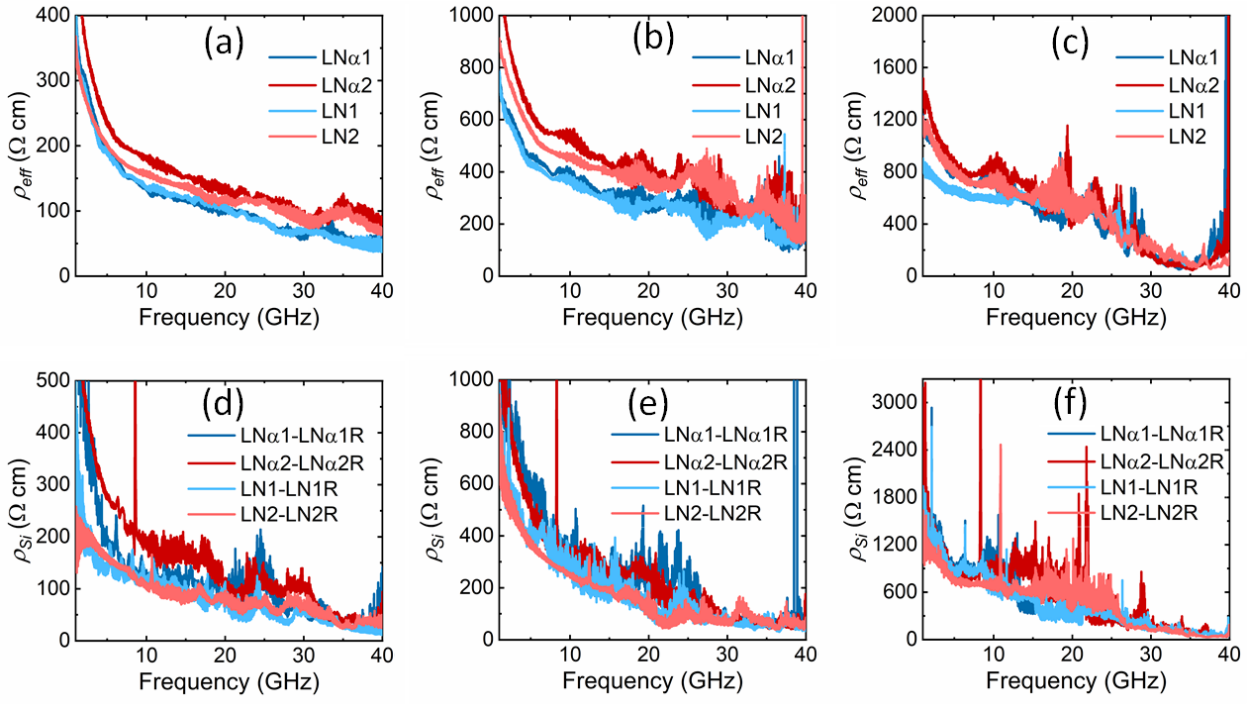


Fig. 11. Extracted (a)–(c) effective substrate resistivity (ρ_{eff}) of the unreleased structures and (d)–(f) Si wafer resistivity (ρ_{Si}) by the subtraction method from CPWs on X-cut $LiNbO_3$ film on high-resistivity Si and amorphous Si with CPW Designs I, II, and III, respectively.

The extracted ρ_{eff}s and ρ_{Si}s of the released and unreleased $LiNbO_3$ on Si structures from CPW Design II are plotted in Fig. 10(b) and (e), and from Design III are plotted in Fig. 10(c) and (f), respectively. The same conclusion can be drawn from these two designs: for unreleased $LiNbO_3$ on Si structures, $LiNbO_3$ film is the dominant contributor to the effective substrate loss at high frequencies, regardless of the depth of electric field distribution. According to the conformal mapping method, q_1 reduces as the feature size of CPW increases, which equals 0.041, 0.022, and 0.013 for Designs I, II, and III, respectively, with an $LiNbO_3$ film thickness of 400 nm. With higher CPW feature sizes (S and W) and lower film thickness, ρ_{eff} rises due to reduced electric field density distributed in the $LiNbO_3$ film.

C. Comparison of LN on HR-Si and Amorphous Si

The extracted $\rho_{eff}s$ of the unreleased $LiNbO_3$ on HR-Si and amorphous Si structures from CPW Design I with different $LiNbO_3$ thicknesses are plotted in Fig. 11(a). In comparison to Fig. 10(a), the substrate loss reduction by amorphous Si is less than that by Si wafer removal. The improvement due to amorphous Si is more significant at low frequency and insignificant at high frequency. As listed in Table V, for the samples with 400-nm $LiNbO_3$, ρ_{eff} at 5 GHz increases from 200.6 to 237.6 Ω· cm, and ρ_{eff} at 24 GHz rises from 112.1 to 128.0 Ω· cm. As shown in the previous section, the contribution of Si wafer to the overall substrate loss of the unreleased dielectric-on-Si structure is only substantial in the lower frequency range. As a result, the benefits of amorphous Si are more noticeable at low frequencies.

Similar to the observation from the Si removal technique, the substrate loss reduction by the amorphous Si technique is insignificant for thick-film structure. As listed in Table V, for the 1.6-μm $LiNbO_3$ sample, in comparison to regular HR-Si, ρ_{eff} increases from 195.0 to 199.9 Ω· cm at 5 GHz. $LiNbO_3$ film has a more significant contribution to the total substrate loss when the film is thicker. Moreover, amorphous Si is less efficient than the Si removal technique in reducing substrate loss.

The Si wafer resistivities (ρ_{Si}s) extracted from the measurement results of CPWs of Design I using the subtraction method are plotted in Fig. 11(d). At low frequency, the loss from a regular HR-Si wafer is more significant than an amorphous Si, but the advantage of an amorphous Si is not substantial at high frequency. A similar conclusion could be drawn from the extracted ρ_{eff}s and ρ_{Si}s with CPWs of Design II plotted in Fig. 11(b) and (e). However, as seen from the Design III results in Fig. 11(c) and (f), for a CPW structure with wider W, the electric field penetrates deeper into the substrate, and the field concentration at the dielectric/Si interface is much reduced. As a result, from Fig. 11(c), an amorphous Si brings more ρ_{eff} improvements to the thick-film structure and the influence of an amorphous Si layer to ρ_{Si}s in Fig. 11(f) is not visible.

D. Comparison of Various Substrates

In addition to $LiNbO_3$ on Si structures, CPWs are also fabricated on SiO_2 on HR-Si and bare HR-Si wafers to study the substrate loss in the commonly used substrates in Si-based devices. The extracted ρ_{eff}s of CPW Design II at 5 and 24 GHz are listed in Table VI.

TABLE V
EXTRACTED EFFECTIVE SUBSTRATE RESISTIVITY (ρ_{EFF} IN Ω·cm) OF X-CUT $LiNbO_3$ ON HR-Si AND AMORPHOUS Si AT 5 AND 24 GHz

	Frequency = 5 GHz			Frequency = 24 GHz		
	Design I	**Design II**	**Design III**	**Design I**	**Design II**	**Design III**
400 nm $LiNbO_3$ on Si (LN2)	200.6	569.2	859.5	112.1	361.4	414.4
400 nm $LiNbO_3$ on α-Si (LN2α)	237.6	641.3	890.2	128.0	446.9	552.0
1.6 µm $LiNbO_3$ on Si (LN1)	195.0	437.0	663.9	89.3	278.2	458.5
1.6 µm $LiNbO_3$ on α-Si (LN1α)	199.9	468.2	818.4	92.9	307.8	369.5

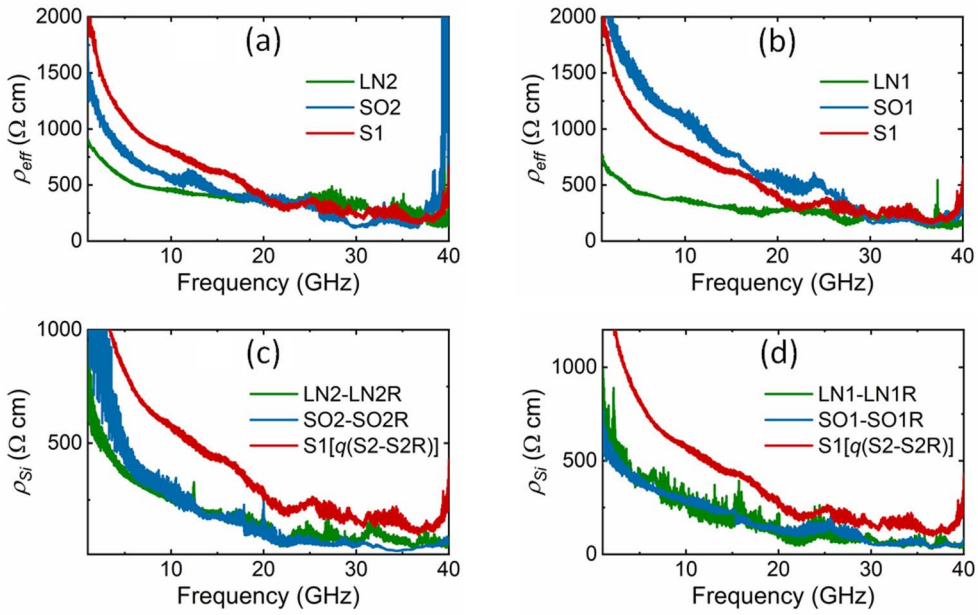


Fig. 12. (a) and (b) Extracted effective substrate resistivity (ρ_{eff}), and (c) and (d) extracted Si wafer resistivity (ρ_{Si}) of Design II CPWs on X-cut $LiNbO_3$ on an HR-Si, PECVD SiO_2 on an HR-Si, and a bare HR-Si, with a dielectric film thickness of 400 nm and 1.6 μm, respectively.

TABLE VI
EXTRACTED EFFECTIVE SUBSTRATE RESISTIVITY (ρ_{EFF} IN Ω·cm) OF VARIOUS SUBSTRATES WITH CPW DESIGN II AT 5 AND 24 GHz

	at 5 GHz	**at 24 GHz**
400 nm $LiNbO_3$ on Si (LN2)	569.2	361.4
400 nm SiO_2 on Si (SO2)	850.7	343.3
1.6 µm $LiNbO_3$ on Si (LN1)	437.0	278.2
1.6 µm SiO_2 on Si (SO1)	1442.0	490.8
High-Resistivity Si (S1)	1118.1	331.1

The extracted ρ_{eff}s of the unreleased $LiNbO_3$ and PECVD SiO_2 with 400-nm thickness on HR-Si and bare HR-Si wafers from CPWs with Design II are plotted in Fig. 12(a). The bare HR-Si wafer has the highest ρ_{eff} among the three substrates. In addition, from the extracted Si wafer resistivities (ρ_{Si}s) in these three structures plotted in Fig. 12(c), ρ_{Si}s of the two dielectric-on-HR-Si structures are smaller than a bare HR-Si wafer, indicating a PSC effect occurring in both $LiNbO_3$ and SiO_2 on HR-Si structures. ρ_{Si} of the S1 structure cannot be obtained by the subtraction method, as in the release process, the regions on the Si wafer not covered by CPWs will be isotopically etched away. To eliminate the inaccuracy in ρ_{eff} caused by approximating the filling factor of the electric field by 0.5, the filling factor q versus frequency is extracted using the S2 and S2R structures listed in Table II, which uses PECVD SiO_2 to cover the Si wafer except for the CPW regions. ρ_{Si} of the S1 structure plotted in Fig. 12(c) and (d) is obtained by replacing 0.5 in ρ_{eff} with the experimentally extracted q from the S2 and S2R structures.

Thick-film dielectric-on-HR-Si structures with a film thickness of 1.6 μm are also studied, and the extracted ρ_{eff}s of the unreleased structures from CPW Design II are plotted in Fig. 12(b). Similar to the thin-film structures, $LiNbO_3$ on an HR-Si structure has a smaller ρ_{eff} than bare HR-Si due to the large loss in $LiNbO_3$ thick film, whereas the thick SiO_2 film on an HR-Si structure has a higher ρ_{eff} than bare HR-Si. As can be observed from the extracted ρ_{Si}s in Fig. 12(d), the Si wafer is lossier in the 1.6-μm SiO_2 on Si structure than a bare Si. However, because a portion of the electric field is distributed in the low-loss SiO_2 thick film, the unreleased SiO_2 on Si structure has a larger ρ_{eff} than a bare HR-Si wafer.

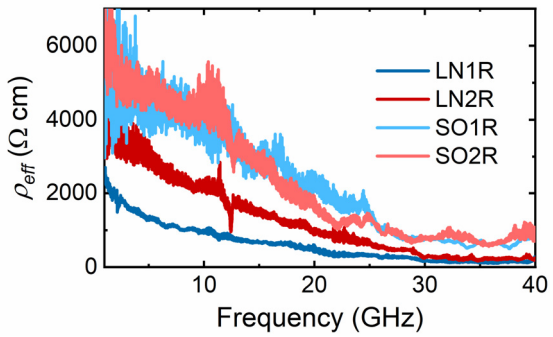


Fig. 13. Extracted effective substrate resistivity (ρ_{eff}) of released Design II CPWs on X-cut $LiNbO_3$ film and SiO_2 film on HR-Si wafer.

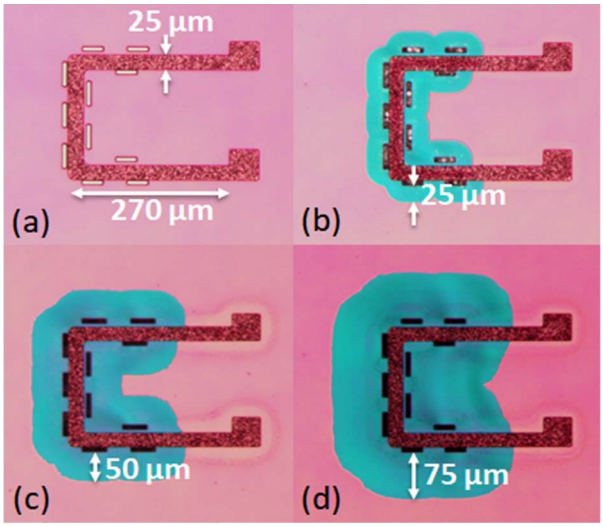


Fig. 14. Microscope images of the fabricated inductors on 400-nm-thick X-cut $LiNbO_3$ with (a) no release and release radius of (b) 25, (c) 50, and (d) 75 μm.

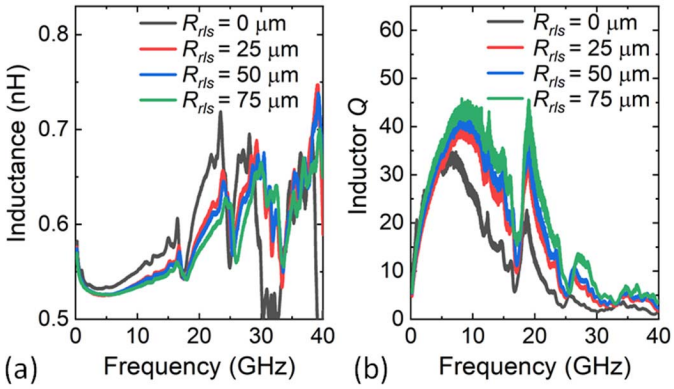


Fig. 15. Measured (a) inductance and (b) quality factor of a fabricated inductor on 400-nm-thick X-cut $LiNbO_3$ with release radius (R_{rls}) equal to 0, 25, 50, and 75 μm.

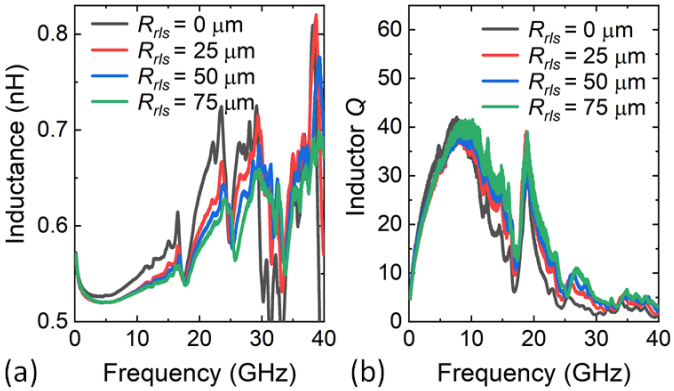


Fig. 16. Measured (a) inductance and (b) quality factor of a fabricated inductor on 1.6-μm-thick X-cut $LiNbO_3$ with release radius (R_{rls}) equal to 0, 25, 50, and 75 μm.

The difference in ρ_{eff}s of the unreleased structures is attributed to the different losses in the dielectric films, as ρ_{Si}s of the two dielectric-on-HR-Si structures are of comparable value. The extracted ρ_{eff}s of the released dielectric-on-HR-Si structures are shown in Fig. 13. The losses in $LiNbO_3$ films are larger than in SiO_2 films. The loss in a thick $LiNbO_3$ film is significantly larger than in a thin film, whereas in SiO_2 films, the dielectric loss is very small such that the film thickness does not bring much influence to the total substrate loss of the suspended structures. Due to the low loss in SiO_2 film, a thick SiO_2 film could serve as a great insulation layer.

E. On-Chip Inductor

On-chip inductors are also fabricated on the X-cut $LiNbO_3$ on Si wafers to study how to improve the inductor quality factor (Q). As seen from the analysis in the previous sections, the loss in the Si wafer increases fast with frequency. As a result, Si wafer removal could be a viable solution to improve inductor Q at high frequency.

An on-chip inductor with various release radii (R_{rls}) of 0, 25, 50, and 75 μm is studied, and the microscope images are shown in Fig. 14. The inductor shown in Fig. 14(a) is unreleased, and the white rectangles beside the inductor are release windows. In the release process, XeF_2 gas contacts and reacts with Si from the release windows. The inductor after a release process is shown in Fig. 14(b). The suspended $LiNbO_3$ film has a turquoise color under a microscope, and the release radius is 25 μm. More cycles of XeF_2-based dry etch are processed on the inductor to increase the release radius to 50 and 75 μm [as shown in Fig. 14(c) and (d)]. The measured inductance and Q of the on-chip inductor with various R_{rls} on X-cut $LiNbO_3$ on Si with $LiNbO_3$ thickness of 400 nm and 1.6 μm are plotted in Figs. 15 and 16, respectively.

At low frequency, the Si wafer removal does not show great benefit in on-chip inductor Q improvement. As listed in Table VII, at 5 GHz, the inductor Q on 400-nm $LiNbO_3$ increases slightly with an increasing release radius. However, the inductor Q on 1.6-μm $LiNbO_3$ at 5 GHz decreases to a growing release radius. As seen in Fig. 16(a), the inductance decreases with increasing release radius due to a reduced effective permittivity of the structure with Si removal. Moreover, for thick-film $LiNbO_3$ on Si structure, the main contributor to the substrate loss at high frequency is the $LiNbO_3$ film. Therefore, the inductor Q on thick $LiNbO_3$ film decreases with an increasing release radius at low frequencies.

TABLE VII
MEASURED QUALITY FACTOR OF A FABRICATED INDUCTOR WITH VARIOUS RELEASE RADII AT 5 GHz

	Release Radius (R_{rls})			
	0 μm	**25 μm**	**50 μm**	**75 μm**
400 nm $LiNbO_3$ on Si	30.5	32.1	33.7	35.5
1.6 μm $LiNbO_3$ on Si	34.7	31.2	32.0	32.1

TABLE VIII
MEASURED QUALITY FACTOR OF A FABRICATED INDUCTOR WITH VARIOUS RELEASE RADII AT 24 GHz

	Release Radius (R_{rls})			
	0 μm	**25 μm**	**50 μm**	**75 μm**
400 nm $LiNbO_3$ on Si	3.0	6.7	8.6	14.3
1.6 μm $LiNbO_3$ on Si	3.2	5.4	7.6	10.0

At high frequency, the inductor Q increases significantly with an increasing release radius. As listed in Table VIII, the inductor Q increases by 2.2 times on a 400-nm $LiNbO_3$ film and 1.7 times on a 1.6-μm $LiNbO_3$ film with a release radius of 25 μm. The inductor Q increases by 4.8 times on a 400-nm $LiNbO_3$ film and 3.1 times on a 1.6-μm $LiNbO_3$ film with a release radius of 75 μm. For high-frequency applications, the release radius of on-chip inductors should be as large as possible.

V. CONCLUSION

Over a frequency range of 1–40 GHz, the substrate loss of seven widely used substrates in silicon-based devices, including $LiNbO_3$-on-HR-Si, $LiNbO_3$-on-amorphous Si, SiO_2-on-HR-Si, and bare HR-Si substrates, is characterized using CPWs. Using two different dielectric film thicknesses of 400 nm and 1.6 μm, the relationship between substrate loss in dielectric-on-Si substrates and dielectric film thickness is investigated. To evaluate the contribution of the Si wafer to the overall loss of the inhomogeneous substrate, the dielectric-on-Si substrates before and after XeF_2 etching of the Si wafer are examined and compared. Si wafer has a higher contribution to the total substrate loss when the dielectric film is thinner and at a lower frequency. In comparing the extracted Si wafer resistivities of $LiNbO_3$ on HR-Si wafers with bare HR-Si wafers, a PSC effect is observed in $LiNbO_3$ on an HR-Si. Finally, judging from the comparison between the extracted substrate resistivity of SiO_2 on an HR-Si with a bare HR-Si, a thick PECVD SiO_2 film could be used as an insulation layer to improve effective substrate resistivity.

Based on the findings of this work, several recommendations could be made for improving the performance of MEMS devices. First, a thick layer of SiO_2 could be used as a sound insulation layer to reduce substrate loss. Second, in the case of MEMS acoustic devices using $LiNbO_3$ film, a thin film is preferred over a thick film from the effective resistivity perspective. Third, a dielectric material with high permittivity is preferred, as it increases the ψ factor defined in (2). Finally, to avoid the PSC effect, instead of a high-resistivity Si carrier wafer, piezoelectric film on an insulator carrier wafer should be used.

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