Low-Power MEMS-Based Pierce Oscillator Using a 61-MHz Capacitive-Gap Disk Resonator

Thura Lin Naing, *Member, IEEE*, Tristan O. Rocheleau, *Member, IEEE*, Elad Alon, *Fellow, IEEE*, and Clark T.-C. Nguyen, *Fellow, IEEE*

***Abstract*— A 61-MHz Pierce oscillator constructed in 0.35-μm CMOS technology and referenced to a polysilicon surface-micromachined capacitive-gap-transduced wine-glass disk resonator has achieved phase noise marks of −119 dBc/Hz at 1-kHz offset and −139 dBc/Hz at far-from-carrier offsets. When divided down to 13 MHz, this corresponds to −132 dBc/Hz at 1-kHz offset from the carrier and −152 dBc/Hz far-from-carrier, sufficient for mobile phone reference oscillator applications, using a single MEMS resonator, i.e., without the need to array multiple resonators. Key to achieving these marks is a Pierce-based circuit design that harnesses a MEMS-enabled input-to-output shunt capacitance more than 100× smaller than exhibited by macroscopic quartz crystals to enable enough negative resistance to instigate and sustain oscillation while consuming only 78 μW of power—a reduction of ∼4.5× over previous work. Increasing the bias voltage of the resonator by 1.25 V further reduces power consumption to 43 μW at the cost of only a few decibels in far-from-carrier phase noise. This oscillator achieves a 1-kHz-offset figure of merit (FOM) of −231 dB, which is now the best among published chip-scale oscillators to date. A complete linear circuit analysis quantifies the influence of resonator input-to-output shunt capacitance on power consumption and predicts further reductions in power consumption via reduction of electrode-to-resonator transducer gaps and bond pad sizes. The demonstrated phase noise and power consumption posted by this tiny MEMS-based oscillator are attractive as potential enablers for low-power "set-and-forget" autonomous sensor networks and embedded radios.**

***Index Terms*— Low power, MEMS, micromechanical, oscillator, phase noise, quality factor, resonator, RF MEMS.**

I. Introduction

In RECENT years, reference oscillators based on high-Q MEMS resonators have become viable alternatives to traditional quartz-based oscillators. Indeed, programmable oscillators using MEMS resonators are now available commercially [1], [2] with impressive specs for timing applications. The latest generation of MEMS-based TCXO products using single-crystal silicon structural material already post long-term stabilities better than ±100 ppb over the commercial temperature range [3]. MEMS-based oscillators also post good short-term stability, on the order of −140 dBc/Hz at 1-kHz offset from 10 MHz. However, their use of fractional-N synthesis to avoid the need for resonator frequency trimming induces fractional spurs [4] that necessitate suppression via defensive design if communication local oscillator applications are of interest. This raises both complexity and power consumption, where power draws in the range of 100 mW in steady state are common.

Recent demonstrations of wide voltage-controlled tunability—up to 46% over 2.3 V [5]—for high-frequency (HF) capacitive-gap transduced MEMS resonators now present an opportunity to reduce power by instead setting frequency via voltage control of the reference resonator itself. To avoid noise from dc-bias fluctuations [6], conceptual approaches to such a synthesizer so far feature multiple resonators at higher VHF to UHF frequencies, each with perhaps 300 ppm/V tuning, in a noncoherent arrangement that switches resonators serving prescribed ranges into a sustaining feedback loop as needed by the desired output [7], [8]. If done using UHF MEMS resonators that post Q's >40 000, such as the ring of [9], there is a potential for radar-like phase noise performance. While still very much a topic of research, the prospect of such a synthesizer drives efforts to reduce oscillator power consumption while maintaining low phase noise.

In past literature, when combined into mechanically coupled array composites, micromechanical resonators have already enabled oscillator marks that meet the −130 dBc/Hz at 1-kHz offset from 13-MHz Global System for Mobile Communications (GSM) reference oscillator spec while consuming only 350 μW of power [10]. While such devices offer compelling savings in power and space compared with quartz for mobile applications, further reductions in power are still desired for future autonomous wireless sensor networks [11], where nodes might be expected to operate for long periods while relying only on compact battery or scavenged power.

Pursuant to further reducing power and area consumption while retaining or exceeding the performance of previous such efforts [10], [12], this work introduces a Pierce-topology oscillator referenced to a single polysilicon wine-glass disk resonator (see Fig. 1). The Pierce topology [13] has long been a

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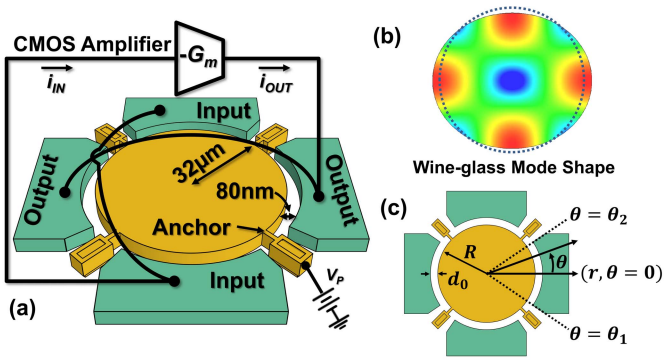

Fig. 1. (a) Perspective-view schematic of the capacitive-gap microchanical disk resonator combined with a sustaining transconductance amplifier to form the Pierce oscillator of this work. (b) Resonator mode shape. (c) Top-view schematic of the MEMS resonator.

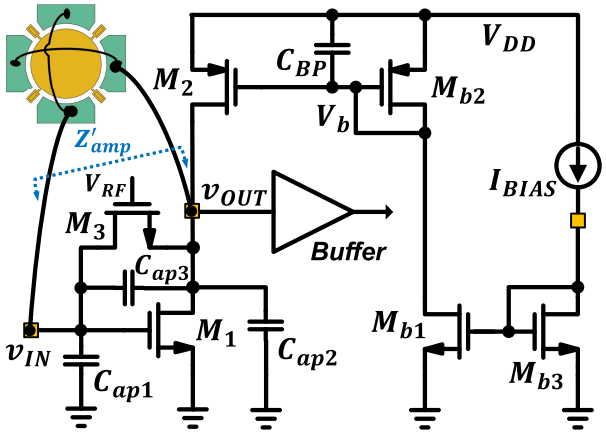

Fig. 2. Schematic of the CMOS amplifier used in the Pierce oscillator, including bias network and device/parasitic capacitance at input and output nodes. Here, C_{ap1}, C_{ap2}, and C_{ap3} are added or nondevice parasitic capacitors that will absorb into C_1, C_2, and C_3 during later analysis.

standard circuit for traditional crystal oscillators due to its low complexity and high performance. So not surprisingly, it has also found use in previous capacitive-gap transduced flexural-mode MEMS resonator oscillators [14], [15]. More recently, use of this topology in piezoelectric resonator oscillators has demonstrated an ability to achieve low-power operation in an on-chip MEMS system [16]–[18].

Until now, however, oscillators referenced to much higher Q capacitive-gap transduced wine-glass disk resonators have not used the Pierce topology, opting instead to employ balanced transresistance amplifier designs [12] more resistant to common-mode noise sources, e.g., from the power supply and its dependence on temperature and acceleration. With more transistors, however, this topology inevitably draws more power than a much simpler Pierce topology employing only one drive transistor. In addition, if the transresistance circuit ends up less balanced than intended, e.g., due to device mismatch, common-mode noise does not fully cancel, and the noise advantage diminishes.

Recognizing the potential advantages, this article presents a complete circuit analysis governing the Pierce oscillator designs suitable for use with capacitive-gap transduced resonators [19]. The design and theory in Sections II–IV offer insights for lower power operation and particularly identify the low input-to-output shunt capacitance of a MEMS resonator as instrumental to achieving low-power oscillation, despite its kiloohm-range motional impedance, which is much higher than the 10–100-Ω values of quartz crystals. Phase noise modeling in Section V then establishes a framework from which to predict performance while incorporating real-world nonlinear and cyclostationary noise effects. Section VI finally presents the measurements on several low-power oscillator designs using the above-mentioned theory with fabricated 61-MHz polysilicon MEMS wine-glass disk resonators that attain phase noise performance marks of −119 dBc/Hz at a 1-kHz offset and −139 dBc/Hz at far-from-carrier offsets, satisfying typical mobile phone specifications [12] while consuming only 78 μW. The power consumption shrinks to just 43 μW via bias adjustments that sacrifice just a few decibels of far-from-carrier phase noise.

II. Pierce Oscillator

The Pierce oscillator topology used here combines a two-port frequency-selective vibrating MEMS wine-glass disk resonator [20] wired in closed-loop positive feedback with a single transconducting gain device, as shown in Fig. 1. Fig. 2 shows the CMOS circuit, where MOS transistor M_1 acts as the gain element and M_2 serves as a load transistor, while MOS resistor M_3 (operated in the linear region to simulate a large resistor) provides dc feedback to set the bias voltage at the gate of M_1 to match that at its drain. Transistors M_b–M_{b3} generate the needed bias voltage V_b at the gate of M_2 to give it a drain current matching or some multiple of I_{BIAS}. Here, a simple current mirror topology suffices for present purposes since the high Q of the MEMS resonator effectively suppresses oscillation frequency deviations due to transistor circuit thermal drift so that resonator drift governs temperature dependence [21]. M_{b3} is also considerably smaller than M_2, which helps to reduce current consumption in the mirror network.

For oscillation to occur, two conditions must hold: 1) the total closed-loop phase shift must be zero and 2) the loop gain must be larger than unity. Focusing on the first condition, transistor M_1 ideally introduces 180° of phase shift between the input and output voltages. At resonance, the phase shift across the wine-glass mode disk resonator is ideally 0°, and therefore an additional 180° is needed to satisfy criterion 2. To supply this, the resonator must operate in the inductive region, i.e., with frequency slightly above that of the series resonance, and resonate with all capacitance in shunt with the gate of M_1, in shunt with the drain of M_1, and in parallel with the resonator. These capacitors include the C_{apn} values of Fig. 2, as well as all relevant resonator and transistor parasitic capacitors.

During oscillation startup, the oscillation amplitude is small—on the order of thermal noise excursions—and the circuit remains linear. In this state, the impedance (Z'_{amp})

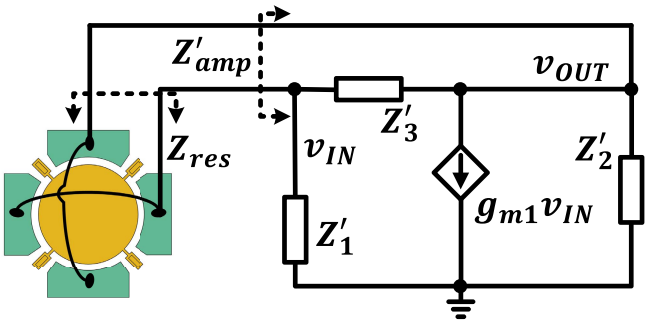

Fig. 3. Small-signal equivalent circuit of the complete oscillator using lumped impedances Z'_1, Z'_2, and Z'_3, which model all capacitance and resistance components of the transistors M_1 (except its transconduance g_{m1}), M_2, and M_3.

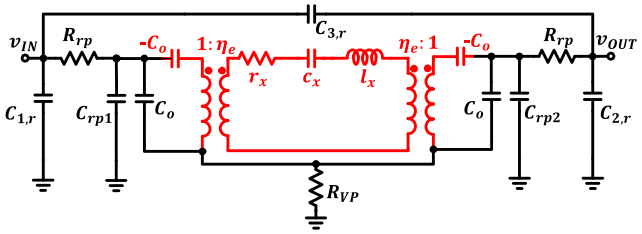

Fig. 4. Resonator small-signal equivalent circuit with the core tank circuit of the resonator shown in red. Here, R_{rp} and R_{VP} are parasitic resistors, mainly from interconnects, while the C_{rp} and C_r values are interconnect and bond pad capacitors, respectively. $C_{3,r}$ models feedthrough capacitance between the input and output nodes.

looking into the gate and drain of M_1 can be determined using the small-signal equivalent circuit of Fig. 3. Here, impedances Z'_1, Z'_2, and Z'_3 include the resistive and reactive components of devices M_1 (excluding its transconductance g_{m1}), M_2, and M_3, as well as nonresonator parasitic elements. Viewing this simplified circuit as a negative-resistance oscillator, the critical condition for oscillation occurs when [22]

$$Z_{\text{res}} + Z'_{\text{amp}} = 0 \tag{1}$$

where Z_{res} is the impedance looking into the resonator, as shown in Fig. 3. Further splitting (1) into real and imaginary components yields

$$-\text{Re}\{Z'_{\text{amp}}\} = \text{Re}\{Z_{\text{res}}\}; \quad -\text{Im}\{Z'_{\text{amp}}\} = \text{Im}\{Z_{\text{res}}\}. \tag{2}$$

Here, the real component requires that the effective resistance looking into the amplifier be negative (gain) to compensate the positive resistance (loss) of the resonator, while the imaginary component sets the phase shift at oscillation. This simple impedance-based approach provides a versatile framework in Section IV for the design and analysis of the present Pierce topology.

III. Resonator Operation and Modeling

The micromechanical disk resonator used as the frequency-selecting tank circuit in this work, shown in Fig. 1, comprises a 3-μm-thick, 32-μm-radius polysilicon disk supported at quasi-nodal points [12] by four beams and surrounded by electrodes spaced by 80-nm gaps from its edges. To excite the resonator into motion, a bias voltage V_P is applied to the disk and an ac drive voltage to the input electrode. These voltages combine to produce a force across the input electrode-to-resonator gap that, at resonance, can excite the compound (2, 1) mode shape, shown in Fig. 1(b), which comprises expansion and contraction of the disk along the orthogonal axes. The frequencies of the modes derive from the transcendental equations summarized in Table I, with resultant operating frequency for the (2, 1) mode used in the present work taking the form [20], [23]

$$f_{\text{nom}} = \frac{\omega_{\text{nom}}}{2\pi} = \frac{K}{R}\sqrt{\frac{E}{\rho(2+2\sigma)}} \tag{3}$$

where ω_{nom} is the angular resonance frequency and R, E, σ, and ρ are the disk radius, Young's modulus, Poisson ratio, and density, respectively, and K is a material-dependent parameter equal to 0.373 [20]. Equation (3) specifically gives the nominal frequency of the isolated disk, with no outside interactions, e.g., no applied voltages that can shift the frequency. Since the frequency of this resonator depends on lithographically defined lateral dimensions, multiple resonators with different operating frequencies are possible in a single process.

The model for this mechanical resonator takes the form of a lumped mechanical system comprising dynamic mass m_{mre}, stiffness k_{mre}, and damping c_{mre} terms [20], [24]. Fig. 4 shows the complete circuit model, including important parasitic elements. As these lumped elements attempt to model a distributed device, their values are location dependent. For a detailed derivation with use cases of the device model, we refer the reader to [20]. For the purposes of the present oscillator design, Table I summarizes the relevant resonator device model, focusing on the m_{mre}, k_{mre}, and c_{mre} values for an equivalent mass–spring system located at any one of the four maximum displacement points on the outer edge of the disk resonator.

Returning to device operation, an ac voltage at the mechanical resonance frequency with amplitude V_{in} applied to the input electrodes combines with the disk-to-electrode bias voltage V_{PCM} to induce resonant motion with radial amplitude, $\Re$, given by [20]

$$\Re = \frac{Q}{k_{\text{mre}}}\left(V_{\text{PCM}}\frac{\partial C_o}{\partial r}\right)V_{\text{in}} = \frac{Q}{k_{\text{mre}}}\eta_e V_{\text{in}} \tag{4}$$

where V_{PCM} ($= V_P - V_{CM}$) is the bias voltage applied across the resonator-to-electrode gap (defined in Table I), V_{CM} is the dc voltage at the gain and drain of M_1, $\partial C_o/\partial r$ is the change in gap capacitance with radial resonator displacement, k_{mre} and η_e (defined in Table I) are the lumped dynamic mechanical stiffness and electromechanical coupling factor, respectively, referenced to the maximum displacement locations in the disk mode shape [20], and Q is the mechanical quality factor.

The driven resonant motion, in turn, modulates the output electrode-to-resonator gap size and hence gap capacitance, which, with a constant electrode-to-resonator voltage,

TABLE I
RESONATOR DESIGN EQUATIONS

Parameter	Design Equations		Variable Definitions and Constants
Transcendental Frequency Equation [23]	$\left[\Psi_n\left(\frac{\zeta}{\xi}\right)-n-q\right].[\Psi_n(\zeta)-n-q]=(nq-n)^2$	(T1. 1)	$J_n(x)$ is the Bessel function of the first kind of order n. R is the disk radius. E, σ, and ρ are the Young's modulus, Poisson ratio, and density of the structural material, respectively. The compound mode shape in this paper corresponds to $(n,m)=(2,1)$, denoting the first ζ solution of (T1. 1) when $n=2$.
	$\Psi_n(x)=\frac{xJ_{n-1}(x)}{J_n(x)}$, $\zeta=2\pi f_{nom}R\sqrt{\frac{\rho(2+2\sigma)}{E}}$, $\xi=\sqrt{\frac{2}{1-\sigma}}$, $q=\frac{\zeta^2}{2n^2-2}$	(T1. 2)	
Mechanical Resonance Frequency	$f_{nom}=\frac{\omega_{nom}}{2\pi}=\frac{K}{R}\sqrt{\frac{E}{\rho(2+2\sigma)}}$	(T1. 3)	ω_{nom} is the radian frequency. $K=\zeta/2\pi$ follows from (T1. 2) and its value is 0.373 for polysilicon struture material and compound $(2,1)$ mode.
Mode Shape Equation [23]	$\Re(r,\theta)=\left[\frac{\partial}{\partial r}J_n\left(\frac{\zeta}{\xi R}r\right)+n\frac{B}{A}\frac{1}{r}J_n\left(\frac{\zeta}{R}r\right)\right]\cos(n\theta)$	(T1. 4)	$\Re(r,\theta)$ is the radial mode shape at the location (r,θ). B/A is the ratio of the coeffienets of rotation and areal dilation in displacments of the compound mode
	$\frac{B}{A}=\frac{2\Psi_n\left(\frac{\zeta}{\xi}\right)+\zeta^2-2n(n+1)}{2n[\Psi_n(\zeta)-(n+1)]}$	(T1. 5)	
Equivalent Dynamic Mass at Location (r,θ) [24]	$m_{mr}(r,\theta)=\frac{KE_{tot}}{0.5[v(r,\theta)]^2}=\frac{\rho h\int_0^{2\pi}\int_0^R r'[\Re(r',\theta')]^2dr'd\theta'}{[\Re(r,\theta)]^2}$	(T1. 6)	KE_{tot} is the total kinetic enery of the disk. $v(r,\theta)=\omega_{nom}\Re(r,\theta)$ is the resonance radial velocity. h is the thickness of the disk structure. The reference point location ($r=R$ and $\theta=0$ in Fig. 1(c)) has the maximum velocity.
Lumped Mechanical Elements	$m_{mre}=m_{mr}(R,0)$, $k_{mre}=\omega_{nom}^2 m_{mre}$, $c_{mre}=\frac{\omega_{nom}m_{mre}}{Q}=\frac{\sqrt{k_{mre}m_{mre}}}{Q}$	(T1. 7)	
Equivalent Circuit Elements [24]	$l_x=m_{mre}$, $c_x=\frac{1}{k_{mre}}$, $r_x=c_{mre}$	(T1. 8)	l_x, c_x, and r_x are the core tank circuit in red as shown in Fig. 4
Electromechanical Coupling Factor [20]	$\eta_e=V_{PCM}\frac{\partial C_o}{\partial r}=V_{PCM}\frac{C_o}{d_0\Delta\theta}\int_{\theta_1}^{\theta_2}\frac{\Re(R,\theta')}{\Re(R,0)}d\theta'$	(T1. 9)	V_{PCM} is the voltage across the resonator-to-electrode gap, which is V_P-V_{CM} in Fig. 1. V_{CM} is the common mode bias voltage at the input and ouput of the amplifier, i.e., at the gate and drain of M_1. $\partial C_o/\partial r$ is the change in electrode-to-resonator overlap capacitance per unit radial displacement. $\Delta\theta=\theta_2-\theta_1$, where θ_1 and θ_2 are the electrode angles defined in Fig. 1(c). d_0 is the electrode-to-resonator gap spacing. ε_o is the permittivity of vacuum.
Static Overlap Capacitance Between Electrode and Disk	$C_o=2\frac{\varepsilon_o Rh\Delta\theta}{d_0}$	(T1. 10)	

produces an output current amplitude at resonance

$$i_{\text{out}}=V_{\text{PCM}}\frac{\partial C_o}{\partial t}=V_{\text{PCM}}\frac{\partial C_o}{\partial r}\frac{\partial r}{\partial t}\rightarrow$$
$$I_{\text{out}}=\frac{Q\omega_{\text{nom}}}{k_{\text{mre}}}\left(V_{\text{PCM}}\frac{\partial C_o}{\partial r}\right)^2 V_{\text{in}}=\frac{\eta_e^2}{c_{\text{mre}}}V_{\text{in}}. \quad (5)$$

The resultant device, though inherently mechanical, acts as a two-port electrical circuit, where input voltage produces resonant displacement that in turn generates an output current. Effectively, the resonant mechanical motion behaves as a high-Q tank circuit suitable for use as the frequency-selecting element in the Pierce oscillator herein.

A. Lumped Electrical Equivalent Circuit Model

Fig. 4 shows a complete small-signal equivalent circuit model of the mechanical resonator [20]. This circuit has two portions: 1) the core tank circuit in red, including series *lcr* elements and transformers with negative capacitors modeling the capacitive-gap transducers and 2) parasitic elements drawn in black. Looking first at the series *lcr* elements in red, the mechanical resonator roles of mass, stiffness, and damping equate to the inductance, capacitance, and resistance in the equivalent circuit as follows [24]:

$$l_x=m_{\text{mre}},\quad c_x=\frac{1}{k_{\text{mre}}},\quad r_x=c_{\text{mre}}. \quad (6)$$

Here, transformers model the coupling between electrical and mechanical domains, capturing both the voltage-to-force and velocity-to-current transfer functions of (4) and (5). The turns ratio η_e is the electromechanical coupling factor given in Table I.

When reflected through the transformers, the portion that equates to the base tank circuit (red) in Fig. 4 further reduces to a series *LCR* circuit sans coupling transformers, for which

the expressions for the equivalent LCR elements take the form

$$L_x = \frac{m_{\text{mre}}}{\eta_e^2};\quad C_x = \frac{\eta_e^2}{k_{\text{mre}}};\quad R_x = \frac{c_{\text{mre}}}{\eta_e^2} \rightarrow R_x \propto \frac{c_{\text{mre}} d_0^4}{V_{\text{PCM}}^2}. \tag{7}$$

The impedance seen looking into the (red) mechanical resonator may then be simply expressed as

$$Z_x = R_x + j\left(\omega L_x - \frac{1}{\omega C_x'}\right) \tag{8}$$

where C_x' is an effective capacitance after frequency pulling by electric fields [25] (to be specified further below). Here, the resonator motional resistance R_x sets the resistance that the amplifier must overcome to induce oscillation. It is important to note that the resonator tank circuit is fundamentally a three-terminal device. The simplification in (8) is only valid when the η_e values are the same for the input and output transformers in Fig. 4. (This is the case for the device used, herein.)

The C_o values in the circuit model static electrode-to-resonator capacitance and are intrinsic to the device. All other elements of the circuit in Fig. 4 are parasitic and include unavoidable trace resistances, R_{rp} and R_{VP}, parasitic capacitance at the input and output electrodes of the resonator, C_{rp1} and C_{rp2}, capacitance at the input and output bond pads, $C_{1,r}$ and $C_{2,r}$, and feedthrough capacitance between the input and output nodes, $C_{3,r}$. These parasitic components contribute to Pierce oscillator operation and set limits to performance, as detailed in Section IV.

During operation, the gap spacing between resonator and electrode changes, which in turn generates a changing electric field and hence varying electrostatic force in the gap. In a small-signal model, this force is in-phase and proportional to disk edge displacement and thus meets the definition of stiffness. Popularly termed electrical stiffness, k_e, this "softens" the equivalent stiffness of the resonator, resulting in a negative shift in the resonance frequency [25]. The electrical stiffness associated with a given electrode is best modeled via a negative C_o in series with C_x [20], giving a resultant total effective capacitance (C_x') of the tank

$$C_x' = \frac{-C_x C_o}{(2C_x - C_o)}. \tag{9}$$

The resultant resonance frequency then takes the form

$$\omega_{oe} = \sqrt{\frac{1}{L_x C_x'}} = \omega_{\text{nom}}\sqrt{1 - \frac{2C_x}{C_o}} = \omega_{\text{nom}}\sqrt{1 - \frac{k_e}{k_{\text{mre}}}} \tag{10}$$

where $k_e = 2\eta_e^2/C_o$ mimics the classic electrical stiffness equation [20].

IV. Amplifier Linear Analysis

An analytical description of oscillator operation starts with small-signal analysis of the complete amplifier–resonator system, which in turn calls for a complete small-signal model. Continuing with an impedance-based approach, the amplifier topology of Fig. 3 with the equivalent small-signal model of Fig. 4 combine to produce the complete oscillator model shown in Fig. 5, which now uses (7) to condense the tank circuit to a more manageable form. Here, Z_1', Z_2', and Z_3' contain the intrinsic transistor small-signal elements, i.e., $C_{gs1}+C_{gd3}+C_{db3}$ in Z_1', $C_{db1}+C_{gd2}+C_{db2}+C_{gs3}+C_{sb3}$ and r_{o1} in Z_2', and C_{gd1} in Z_3', and also contain nonresonator parasitic capacitors, $C_{1,r}$, $C_{2,r}$, and $C_{3,r}$.

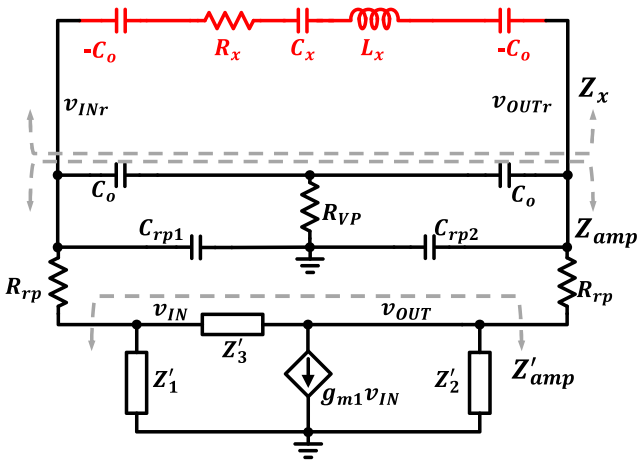

Fig. 5. Complete small-signal oscillator circuit model indicating the division between amplifier and resonator used for impedance modeling. Here, $C_{1,r}$, $C_{2,r}$, and $C_{3,r}$ in Fig. 4 absorb into Z_1', Z_2', and Z_3'.

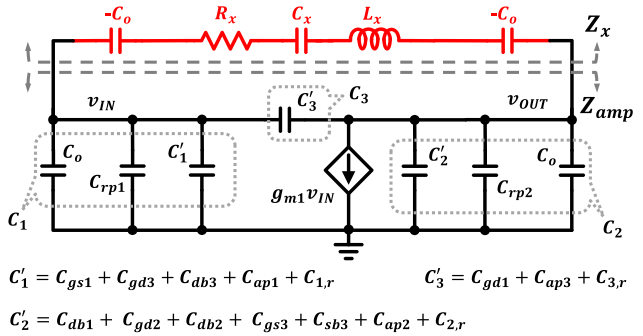

Fig. 6. Condensed small-signal oscillator circuit from Fig. 5 that models the ideal loss situation of Section IV-A.

Looking into the amplifier while excluding resonator parasitic elements (but including nonresonator parasitic capacitance) yields the impedance

$$Z_{\text{amp}}' = \frac{Z_1'Z_3' + Z_2'Z_3' + Z_1'Z_2'Z_3'g_{m1}}{Z_1' + Z_2' + Z_3' + Z_1'Z_2'g_{m1}}. \tag{11}$$

This equation plugs directly into (2) with a corresponding resonator impedance expression (including parasitic elements) to provide a model for oscillator startup behavior that accounts for all relevant loss mechanisms. However, because the complexity of the resulting model makes it somewhat opaque to design insight, it is instructive to first consider a simpler model that ignores parasitic resistive losses. Section IV-A takes this approach.

A. Ideal Loss Analysis

Pursuant to generating insights that guide oscillator startup design, this analysis first tackles an ideal lossless case that

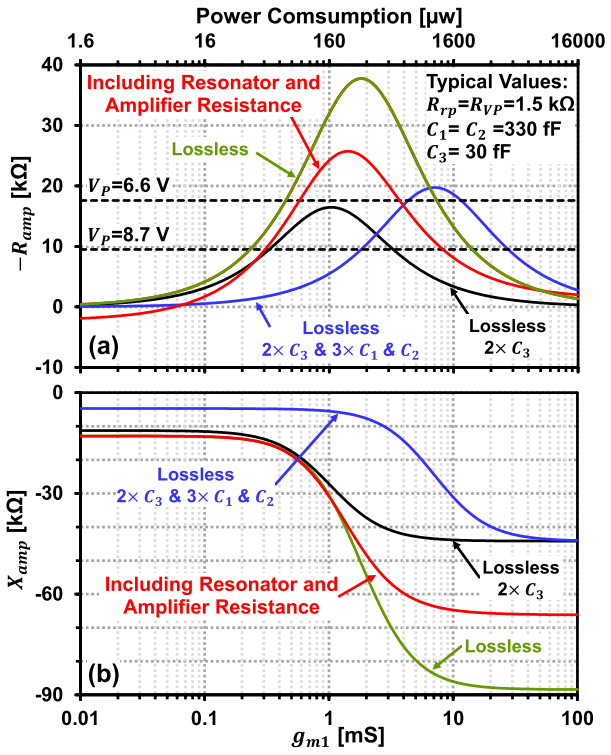

Fig. 7. (a) Theoretical plots of amplifier gain $-R_{\text{amp}}$ versus transconductance g_{m1} of the M_1 transistor, together with the required power consumption to achieve this g_{m1} using $V_{\text{DD}} = 2$ V, $V^* = 0.16$ V (i.e., the effective overdrive voltage) and (b) corresponding plots of amplifier reactance, X_{amp}. The black dashed lines correspond to the calculated motional resistances of the resonator for different V_P values. The green line corresponds to a lossless amplifier with typical values for C_{1-3} that easily generate sufficient gain for oscillation, while the black curve illustrates the detriment of increasing C_3 by two times, resulting in no oscillation for V_P of 6.6 V. Increasing C_1 and C_2 by three times allows oscillation for the $V_P = 6.6$ V case, but at the cost of burning significantly larger power as shown by the blue curve. The red curve includes typical parasitic loss/resistance of the amplifier and resonator.

considers only the micromechanical resonator's motional resistance R_x while neglecting all other resistive losses. Specifically, trace resistance is zero ($R_{rp} = 0$ and $R_{\text{VP}} = 0$) and amplifier losses are small (implying that the real parts of $Z_1 - Z_3$ are large). Absorbing capacitors, C_{rp1}, C_{rp2}, and C_o from the resonator into C_1, C_2, and C_3 as shown in Fig. 6, Z'_{amp} in Fig. 5 becomes Z_{amp}, and the resonator portion reduces to its base (red) tank circuit. The real and imaginary components of Z_{amp} take the form

$$R_{\text{amp}} = -\frac{g_{m1}C_1C_2}{(g_{m1}C_3)^2 + \omega^2(C_1C_2 + C_1C_3 + C_2C_3)^2} \tag{12}$$

$$X_{\text{amp}} = -\frac{g_{m1}^2C_3 + \omega^2(C_1+C_2)(C_1C_2+C_1C_3+C_2C_3)}{\omega[(g_{m1}C_3)^2+\omega^2(C_1C_2+C_1C_3+C_2C_3)^2]}. \tag{13}$$

Using (1) and (2), the requirements for oscillation then take the form

$$-R_{\text{amp}} = \text{Re}\{Z_x\} = R_x;\ -X_{\text{amp}} = \text{Im}\{Z_x\} = \omega L_x - \frac{1}{\omega C'_x}. \tag{14}$$

For oscillation to start, $-R_{\text{amp}}$ must be larger than the motional resistance R_x. However, C_1–C_3 constrain the achievable $-R_{\text{amp}}$ to a maximum value. The green curve in Fig. 7(a) illustrates this effect by plotting $-R_{\text{amp}}$ versus M_1's transconductance g_{m1} for typical device values, together with typical resonator R_x values (the straight dotted lines) for two different bias voltages, V_P. The green curve in Fig. 7(b) similarly shows the theoretical plot of X_{amp}. The maximum value of $-R_{\text{amp}}$ occurs when

$$g_{m1,R\max} = \omega_{oe}\left(C_1 + C_2 + \frac{C_1C_2}{C_3}\right) \tag{15}$$

with resultant $|R_{\text{amp}}|_{\max}$

$$|R_{\text{amp}}|_{\max} = \frac{1}{2C_3\omega_{oe}\left(1 + \frac{C_1+C_2}{C_1C_2}C_3\right)}. \tag{16}$$

The oscillator loop gain is greater than unity wherever the R_{amp} curve exceeds the R_x of the resonator tank. This occurs over a range of g_{m1} values, which for a given M_1 size corresponds to a range of drain currents or equivalently a range of power consumptions. For a given R_x, achieving the lowest possible power operation necessitates operating at the lowest g_{m1}. The expression for this minimum, or critical, g_{m1} takes the form

$$g_{m1,\text{crit}} = \frac{C_1C_2}{2C_3^2R_x}\left[1 - \sqrt{1 - \frac{R_x^2}{|R_{\text{amp}}|_{\max}^2}}\right]. \tag{17}$$

If $(g_{m1}C_3)^2 \ll \omega^2(C_1C_2 + C_1C_3 + C_2C_3)^2$, as is the case for the low-power MEMS-based oscillators studied here, then (17) further simplifies to the approximate form

$$g_{m1,\text{crit}} = C_1C_2\omega_{oe}^2\left(1 + \frac{C_1 + C_2}{C_1C_2}C_3\right)^2 R_x. \tag{18}$$

Since g_{m1} decreases alongside power consumption, (18) suggests that low-power operation necessitates minimizing C_1–C_3, which minimizes $g_{m1,\text{crit}}$. Equation (16) additionally sets a maximum possible gain irrespective of power budget, thus setting a ceiling on the allowable resonator motional impedance of $1/(2C_3\omega_{oe})$.

To illustrate, the black curve in Fig. 7(a) shows reduced $-R_{\text{amp}}$ when C_3 increases from that of the green curve. In this case, $|R_{\text{amp}}|_{\max}$ becomes less than the motional resistance corresponding to V_P of 6.6 V, and therefore, no oscillation can occur even with increased power consumption. To overcome this limit, one can increase C_1 and C_2 by a factor of 3 as in the blue curve, providing an increase in $|R_{\text{amp}}|_{\max}$ and thus allowing oscillation, though at a significant cost in power. In short, the goal of a low-power oscillator is best achieved by minimizing C_3.

This strong dependence on C_3 reveals why self-sustained oscillation of a micromechanical resonator is possible using a Pierce circuit, despite the resonator's large motional resistance R_x. Indeed, if R_{VP} in Fig. 5 is small (or zero, as assumed in the present ideal loss analysis), the ~25-fF C_o values from a 61-MHz wine-glass disk resonator wired as in Fig. 1 will contribute very little to C_3, instead contributing the bulk of their capacitance to C_1 and C_2. C_3 ultimately derives from transistor $C_{gd} \sim 1$ fF and parasitic feedthough capacitance above and below (i.e., through the substrate) the resonator. After adding ballpark wiring and other parasitic components,

this number might bloom to 20–50 fF [26], which is still many times smaller than the 4 pF [27], [28] of a typical 60-MHz quartz crystal, allowing $|R_{\text{amp}}|_{\max}$ to exceed the disk R_x of 18.2 kΩ for V_P of 6.6 V. In comparison, with $C_3 = 4$ pF, a typical quartz crystal cannot muster $|R_{\text{amp}}|_{\max}$ more than 157 Ω, even with C_1 and C_2 as large as 7 pF. Of course, the much smaller $R_x = 70$ Ω of a typical 60-MHz quartz crystal does not require that $|R_{\text{amp}}|_{\max}$ be so large, but the needed C_1 and C_2 values are still on the order of 10 pF. Since larger C_1 and C_2 demand higher transistor drive power, a MEMS-based Pierce oscillator circuit with a relatively small C_3 that in turn allows small C_1 and C_2 should permit much lower power consumption—a point that Section IV-C makes clear. If the resonator R_x can be further lowered, e.g., by increasing its dc-bias voltage V_P, as shown in Fig. 7(a), the power consumption of a MEMS-based Pierce oscillator should shrink. Indeed, the intersection of the green curve of Fig. 7(a) with the $V_P = 8.7$ V line shows that an increase in V_P by ∼2 V decreases the oscillation power requirement from ∼72 to ∼37 μW.

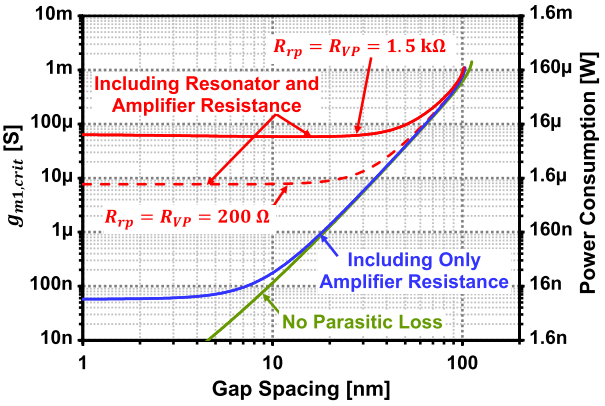

Fig. 8. Theoretical predictions of $g_{m1,\text{crit}}$ and power consumption requirements to achieve oscillation versus resonator capacitive-gap spacing. The green curve assumes the lossless case of (17), where power consumption decreases without limit as the gap shrinks. The blue curve includes amplifier loss/resistance, while the red curves also include additional resonator parasitic resistance, showing a minimum power plateau regardless of decreased gap spacing. Here, $V_{\text{DD}} = 2$ V, $V^* = 0.16$ V (i.e., the effective overdrive voltage), and $V_P = 8.7$ V with the same capacitor values as in Fig. 7.

B. Full Loss Analysis

While the ideal analysis provides good design insight, it neglects real-world parasitic losses from the resonator trace resistances (R_{rp} and R_{VP}) and the amplifier's intrinsic resistance and leakage, both of which lead to increased gain requirements, hence increased power consumption. Here, the output resistance of M_1 that dominates amplifier loss takes the approximate (long channel) form

$$r_{o1} \approx \frac{2}{\lambda g_{m1}(V_{\text{GS1}} - V_{\text{th1}})} \tag{19}$$

where λ is the channel-length modulation constant, V_{th1} is the threshold voltage of M_1, and V_{GS1} is the bias gate-to-source voltage of M_1. This output resistance, if not large enough, can steal amplifier output current away from the resonator in the feedback loop, thereby lowering the loop gain. This then raises the g_{m1} required to induce oscillation.

Including these losses produces the red curves in Fig. 7, where the amplifier must burn ∼30% more power to produce oscillation compared with the ideal-loss case. As will be seen in association with Fig. 8, the trace resistances ultimately dominate over r_{o1} among loss mechanisms that raise power consumption.

C. Minimizing Power Consumption

To better identify key dependences, this section considers a design where C_1 and C_2 are equal. Rewriting C_1 and C_2 as $(C_o + C_{p1,2})$, where $C_{p1,2}$ is the sum of all capacitance not intrinsic to the MEMS resonator at either the input or the output, allows further simplification of (18)

$$g_{m1,\text{crit}} = \frac{\omega_{oe}}{QC_x}(C_o + C_{p1,2} + 2C_3)^2 = \frac{\omega_{oe}}{Q}\frac{C_{\text{ptot}}}{(C_x/C_{\text{ptot}})}. \tag{20}$$

Equation (20) suggests that low-power operation necessitates the smallest possible stray capacitance. Here, the required $g_{m1,\text{crit}}$, and thus the needed power to oscillate, is inversely proportional to (C_x/C_{ptot}^2), where C_{ptot} is the weighted sum of capacitors inside the parentheses in the first form of (20).

For the case of a fully integrated (i.e., single-chip) system that can dispense with bond pads or ESD projection in the loop [29], [30], the C_o term can dominate over $(C_{p1,2} + 2C_3)$, leaving $(1/C_o) \cdot (C_x/C_o)$ as the governing performance metric to be maximized for lowest power consumption. Here, resonator designers will recognize (C_x/C_o) as a quantity that gauges electromechanical coupling strength [31].

Assuming that C_o dominates, low power consumption then requires a combination of small C_o and large (C_x/C_o), which in turn calls for increasing C_x (or equivalently, decreasing resonator R_x) while maintaining low parasitic capacitance. Equation (7) stipulates that increasing V_P quadratically reduces R_x—an effective approach, but possibly constrained by available supply voltages in mobile applications. Instead, reducing the sidewall electrode-to-resonator gap spacing d_0 provides a marked fourth-power decrease in resonator R_x (or increase in C_x), while C_o increases only linearly, providing an overall third-power increase in (C_x/C_o) and a corresponding quadratic decrease in operating power.

As the gap shrinks, the $C_o \gg (C_{p1,2}+2C_3)$ approximation gets even better, at which point (20) condenses to

$$g_{m1,\text{crit}} \cong \frac{\omega_{oe}}{Q}\frac{C_o}{(C_x/C_o)} \rightarrow g_{m1,\text{crit}} \propto \frac{d_o^2}{V_P^2}. \tag{21}$$

In principle, power requirements may thus scale downward entirely via reduction in gap size, subject to mainly fabrication limitations, at least when resistive losses are small.

For the case where interface capacitance swamps resonator capacitance, the dependence on gap spacing is even stronger. To illustrate, Fig. 8(a) shows the theoretical plots of $g_{m1,\text{crit}}$ and power consumption versus resonator sidewall gap when $C_{p1,2} > C_o$. For gap sizes above 100 nm, $R_x > |R_{\text{amp}}|_{\max}$ and no solution to (17) exists for the specific amplifier design of this work. As the electrode-to-resonator gap shrinks, power consumption decreases with the fourth power of decreasing gap size from 100 to 10 nm, which derives mainly from the fourth power increase in C_x. In the lossless case, represented

TABLE II
RESONATOR AND AMPLIFIER DESIGN SUMMARY

Parameter	Source	Operating Power			Unit
		110μW	78μW	43μW	
Resonator Design/Parameters					
Structure Material	-	Polysilicon			-
Radius, R	layout	32			μm
Thickness, h	layout	3.0			μm
Electrode Overlap Angle, $\Delta\theta$	layout	67			deg
Electrode-to-Resonator Gap, d_o	measured	80			nm
Density, ρ	[12]	2300			kg/m^3
Young's Modulus, E	[39]	150			GPa
Poisson Ratio, σ	[12]	0.226			-
Resonator Mass, m_{mre}	Eqn. (T1. 7)	8.06×10^{-12}			kg
Resonator Stiffness, k_{mre}	Eqn. (T1. 7)	1.15×10^{6}			N/m
Damping factor, c_{mre}	Eqn. (T1. 7)	3.8×10^{-8}			kg/s
Quality Factor in Vacuum, Q*	measured	80,000			-
Series Resistance, R_x	Eqn. (7)	18.2	13.8	9.8	kΩ
Inductance, L_x	Eqn. (7)	3.85	2.93	2.08	H
Capacitance, C_x	Eqn. (7)	1.82	2.39	3.37	aF
Electromech. Coupling, η_e	Eqn. (7)	1.45×10^{-6}	1.66×10^{-6}	1.97×10^{-6}	C/m
DC-Bias Voltage, V_P	measured	6.6	7.45	8.7	V
DC-Bias Voltage Across the Gap, V_{PCM}	calculated	5.913	6.778	8.046	V
Static Overlap Capacitance, C_o	Eqn. (T1. 10)	24.8			fF
Amplifier Design/Parameters					
M_1 Size (Width/Length)	layout	9.5/0.35	9.5/0.35	9.5/0.35	μm
M_2 Size (Width/Length)	layout	4.7/0.35	4.7/0.35	4.7/0.35	μm
Transconductance Gain of M_1, g_{m1}	simulation	571	497	410	μS
Transconductance Gain of M_2, g_{m2}	simulation	195	177	153	μS
Supply Voltage, V_{DD}	measured	2	1.7	1.3	V
Supply Current, I_{VDD}	measured	55	45.9	33.1	μA
Input/Ouput Common-Mode Voltage, V_{CM}	measured	0.687	0.672	0.654	V
Feedback Transistor Gate Voltage, V_{RF}	measured	1	0.96	1	V

* Since measured Q values hovered around 80,000 with deviations at different DC-biasings that were within the measurement uncertainty, this row just uses 80,000 for all cases.

by the green curve, this power reduction has no limit. If instead intrinsic amplifier loss is considered as in the blue curve, power consumption plateaus at a minimum value of ∼9 nW, representing the lowest power design possible. The red curves additionally add typical resonator (doped polysilicon) trace resistances of 200 Ω (dotted line) and 1.5 kΩ (solid line), showing increased minimum power consumption of ∼1 and 10 μW, respectively. Clearly, achieving the lowest possible power requires minimizing both stray capacitance and trace resistance, the latter of which could be achievable by replacing polysilicon resonator interconnect with metal.

D. Amplifier-Derived Frequency Pulling

Though the oscillation frequency depends primarily on mechanical resonance, stray capacitance and amplifier reactance produce a slight shift of oscillation frequency to meet the requirement of (14). Solving this for frequency yields

$$f_o = f_{nom}\sqrt{\left[1-\eta_e^2\left(\frac{2}{C_o}+\omega_{oe}X_{\text{amp}}\right)\frac{1}{k_{\text{mre}}}\right]} \tag{22}$$

where X_{amp} is the amplifier reactance as defined in (13) evaluated at the oscillation frequency. This effectively manifests as a correction to the total resonator stiffness comprising both the usual electrical stiffness, $2\eta_e^2/C_o$, and a second term, $\eta_e^2\omega_{oe}X_{\text{amp}}$, representing frequency pulling due to amplifier loading. The resultant total electrical stiffness then takes the form

$$k_{eL} = \eta_e^2\left(\frac{2}{C_o}+\omega_{oe}X_{\text{amp}}\right). \tag{23}$$

For the present amplifier, X_{amp} has a negative value [see Fig. 7(b)], leading to a reduction in total electrical stiffness. This permits an oscillator design that uses amplifier loading to cancel the electrical stiffness. By way of illustration, the electrical stiffness for the resonator described in Table II with $V_P = 6.6$ V is 168 N/m, while the amplifier effective stiffness is –31 N/m corresponding to a mere 7.26-ppm frequency shift. The precision of the mechanical-resonator-defined frequency here is a clear advantage of this MEMS-based oscillator over

the typical on-chip *LC* oscillator, which often requires strategic design to compensate for amplifier loading. Like a crystal oscillator, the very high Q of this MEMS-based oscillator produces a phase transition around resonance so sharp that amplifier phase shifts—e.g., caused by temperature changes, noise, and so on—barely affect the oscillation frequency. The MEMS resonator sets the frequency while suppressing amplifier environmental dependencies, and this enhances oscillator stability.

E. Oscillation Startup

Upon amplifier turn-on, a loop gain greater than unity produces oscillation growth, modeled in the small-signal regime by an exponential with time constant [32]

$$\tau = -\frac{2L_x}{R_{\text{amp}} + R_x} = -\frac{2L_x}{R_x(1-T)} \tag{24}$$

where $T = -R_{\text{amp}}/R_x$ is the loop gain. Neglecting nonlinear effects, the total time required to reach a desired steady-state amplitude takes the form

$$t_{su} = \tau \ln \frac{V_{\text{osc}}}{v_{\text{res}}(0)} \tag{25}$$

where V_{osc} is the steady-state oscillation voltage across the resonator and $v_{\text{res}}(0)$ is the initial voltage across the resonator at $t = 0$.

Fast oscillator turn-on time can be an important performance metric for applications requiring cycled oscillator startup for power savings or superregenerative receivers [33], [34] that identify RF transmitted data by measuring the rate at which oscillation grows. Equation (25) suggests two approaches to reduce oscillator startup time: 1) increase the initial starting voltage $v_{\text{res}}(0)$ and 2) decrease the time constant (τ). Typically, $v_{\text{res}}(0)$ derives from noise, which in the case of a MEMS-based oscillator derives from the Brownian motion as well as transistor noise, but may also be tailored by an appropriate switch-on procedure or injection of resonance current at startup. Assuming that the $Q \sim L_x/R_x$ of the resonator stays constant, the oscillator time constant ends up depending primarily on the loop gain. Increasing loop gain requires either an increase in amplifier gain R_{amp} or a reduction of resonator motional resistance R_x. As an increase in R_{amp} comes at the cost of increased g_{m1} and thus higher power consumption, the lowest power and fastest startup comes about by minimizing R_x, perhaps best achieved by increasing dc-bias V_{PCM} or reducing gap spacing d_0.

F. Pierce Versus Transimpedance Amplifier Oscillators

The transimpedance amplifier (TIA) used to instigate and sustain oscillation in previous work [10], [12] comprised a fully differential CMOS amplifier biased by a common-mode feedback circuit that effectively canceled common-mode noise, especially low-frequency noise caused by vibration [35]. The Pierce oscillator presented here, however, with its single-ended Pierce topology, sacrifices this common-mode feedback to achieve lower noise figure, hence lower phase noise, than TIA-based oscillators. This comes about by: 1) using only two active transistors compared with a minimum of four in the TIA of [10]; 2) using a very large shunt–shunt feedback MOS resistor M_3 for biasing compared with the much smaller gain- and bandwidth-setting resistor used by the TIA, where the larger the resistance, the smaller the current noise; and 3) using C_{BP}, at the cost of some area increase, between the gate of M_2 and V_{DD}, as shown in Fig. 2, to filter noise from bias transistors M_{b1}–M_{b3} and from V_{DD}.

Finally, the smaller transistor stack of the Pierce oscillator circuit allows it to operate at lower supply voltage V_{DD}, and hence lower power, without driving the two transistors into their triode regions. Together, these design changes enable a Pierce oscillator with not only lower power but also reduced noise when compared with the more complicated TIA configurations [36].

V. Phase Noise

Achieving low phase noise in reference oscillators is essential for wireless communications, where close-to-carrier phase noise degrades receiver noise figure by adding noise within the receiver bandwidth and, on the transmit side, risks producing excessive out-of-channel interference. The phase noise of a linear oscillator in the presence of thermal noise sources is often described by Leeson's phase noise model [37]

$$\mathcal{L}(\Delta f) = 10\log\left[\frac{2FkT}{P_{\text{sig}}}\left(1 + \frac{1}{Q^2}\left(\frac{f_o}{2\Delta f}\right)^2\right)\right] \tag{26}$$

where $\mathcal{L}(\Delta f)$ is single-sideband phase noise power in dBc, k and T are the Boltzmann's constant and Kelvin temperature, respectively, F is the amplifier noise correction factor, P_{sig} is the loop signal power, and Δf is the frequency offset from the carrier. Though this model does not always provide perfect predictive power, it serves as a useful tool in understanding avenues that reduce phase noise. To design the lowest phase noise oscillator, (26) suggests minimizing amplifier and resonator noise, increasing loop signal power; and maximizing resonator Q, with the latter having the strongest impact on close-to-carrier phase noise. Indeed, it is the high Q-factors achievable from capacitive-gap MEMS resonators that make possible the simultaneous low-power and low-phase-noise oscillators here.

However, as Leeson's equation derives from a linear model incorporating thermal noise sources alone, it does not capture many important aspects of real-world oscillator operation. In particular, the most basic model largely disregards the cyclostationary noise sources and time-varying noise-to-phase transfer processes—all inherently unavoidable aspects of large-signal oscillating systems.

To derive a more complete noise-to-phase transfer function for the linear time-varying oscillator system, we borrow from the approach of Hajimiri [38] and introduce a set of impulse sensitivity functions (ISFs), denoted as $\Gamma(\theta)$, that better characterize the instantaneous oscillation phase noise induced by current or voltage noise sources from circuit elements. Defined as the oscillation phase shift induced per normalized voltage (current) unit impulse applied at a specified oscillation phase, θ, to a specified node (branch), ISF is a dimensionless

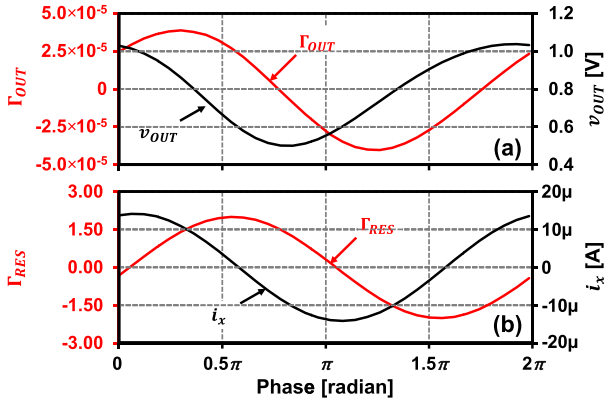

Fig. 9. (a) ISF Γ_{OUT} (red line) for current noise injected at node v_{OUT}, with oscillator output waveform for reference (black line) as a function of oscillator phase. (b) Γ_{res} (red line) for voltage noise injected in series with the resonator, together with resonator current i_x (black line) as a function of oscillation phase. Here, simulations assume the operating conditions of the 43-μW bias in Table II.

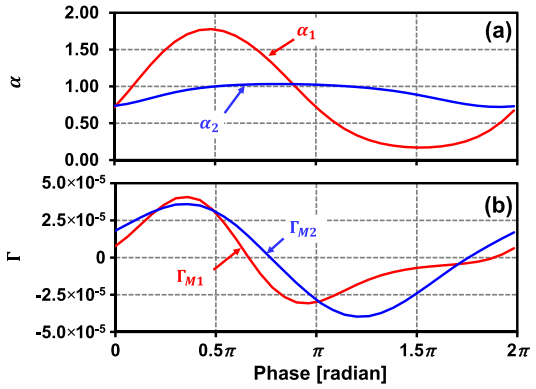

Fig. 10. (a) Phase-dependent shaping functions α, and (b) effective $\Gamma(\theta)$ functions of transistor M_1 (red line) and M_2 (blue line) operating at the 43-μW bias condition in Table II.

transfer function that relates noise sources to their oscillator phase noise contributions. The phase dependence of the ISF additionally facilitates the capture of dynamical effects that influence noise-to-phase conversion with varying periodic signal amplitude (i.e., oscillator phase). Summation of multiple independent ISF's allows the inclusion of an arbitrary number of noise sources, improving upon the single thermal noise source model of Leeson's equation.

In the Pierce oscillator, three sources of noise contribute to phase noise: 1) current noise due to the gain transistor (M_1); 2) current noise due to the bias circuitry; and 3) intrinsic thermal noise of the resonator. Modeling these sources requires an ISF for the resonator noise, along with a single ISF for transistor noise, as both the bias circuit and gain transistor inject current noise at v_{OUT}.

To simulate the ISF for current noise injected at v_{OUT}, a transient simulation is run until steady-state oscillation is achieved. Small charge impulses Δq are then injected to v_{OUT} at varying points in the oscillation cycle, and the resultant oscillation phase shift, $\Delta\phi(\theta) = \omega_o \cdot \Delta t(\theta)$, is measured. Normalizing these phase shifts by the ratio of injected charge to maximum charge produced by the oscillation itself, $q_{\max}$, then yields the desired ISF: $\Gamma(\theta) = \Delta\phi(\theta)(q_{\max}/\Delta q(\theta))$. Fig. 9(a) shows the simulated ISF $\Gamma_{\mathrm{OUT}}(\theta)$, in red, for the oscillator bias conditions corresponding to 43-μW operation in Table II, together with the oscillator output, v_{OUT}, in black. As would be expected, noise injected near oscillator zero crossings produces the greatest phase shift, while noise near oscillator amplitude peaks is largely insignificant. Similarly, Fig. 9(b) shows the simulated ISF $\Gamma_{\mathrm{RES}}(\theta)$ for voltage noise injected by the resonator (red) together with resonator current i_x (black).

With ISF functions in hand, the phase noise contribution expressions for the equivalent current noise sources at v_{OUT} readily follow. In the Pierce oscillator of Fig. 2, the relevant current noise sources comprise M_1 and M_2 drain current noise and the equivalent current noise due to the bias circuit. (Note that the near-zero current in M_3 and its large channel resistance renders its current noise contribution negligible.) The M_1 and M_2 noise takes the form

$$\overline{i_{nT,Mj}^2} = 4kT\gamma\, g_{mj}\delta f; \qquad \overline{i_{nF,Mj}^2} = \overline{i_{nT,Mj}^2}\frac{f_{cj}}{\Delta f} \tag{27}$$

where $\overline{i_{nT,Mj}^2}$ are the thermal noise and $\overline{i_{nF,Mj}^2}$ are the flicker noise current, δf is the noise bandwidth, g_{mj} is the transconductance gain, and f_{cj} is the flicker noise corner frequency, all of transistor j; γ is a process-dependent parameter equal to $\sim$0.81 for the CMOS used in this work. The equivalent current noise due to the bias circuit derives from $g_{m2}^2\overline{v_{n,B}^2}$, where $\overline{v_{n,B}^2}$ is the equivalent voltage noise of the bias circuit at the gate of M_2. Here, C_{BP} and the diode-connected transistor M_{b2} filter out HF thermal noise, leaving only flicker noise components of $\overline{v_{n,B}^2}$ that takes the form $\overline{v_{n,B}^2} = \overline{v_{nT,B}^2}\cdot(f_{c,B}/\Delta f)$, where $\overline{v_{nT,B}^2}$ and $f_{c,B}$ are the thermal noise and the flicker noise corner frequency, respectively. Meanwhile, voltage noise in series with the resonator mainly consists of the resonator's thermal noise, given by $\overline{v_{nT,\mathrm{RES}}^2} = 4kTR_x\delta f$.

Because the transistor noise sources depend on the drain current of the transistor, the resultant noise amplitude must vary periodically with the oscillation cycle. The contribution from such cyclostationary noise sources may be modeled using a second set of phase-dependent functions, $\alpha_1(\theta)$ and $\alpha_2(\theta)$, which capture the instantaneous G_m of a transistor normalized to the small-signal bias g_m. Fig. 10(a) shows the simulated $\alpha_1(\theta)$ and $\alpha_2(\theta)$ here. To model both the changing noise sources and the phase-dependence of noise source to phase noise conversion, a new set of effective $\Gamma(\theta)$ is defined as the product of $\alpha(\theta)$ functions and $\Gamma_{\mathrm{OUT}}(\theta)$

$$\Gamma_{M1}(\theta) = \Gamma_{\mathrm{OUT}}(\theta)\cdot\alpha_1(\theta); \quad \Gamma_{M2}(\theta) = \Gamma_{\mathrm{OUT}}(\theta)\cdot\alpha_2(\theta). \tag{28}$$

In contrast, resonator thermal noise is essentially constant throughout the oscillation cycle, allowing representation as a stationary source.

The phase noise power spectrum density due to the current noise from M_1 and M_2, and the bias circuit then take the

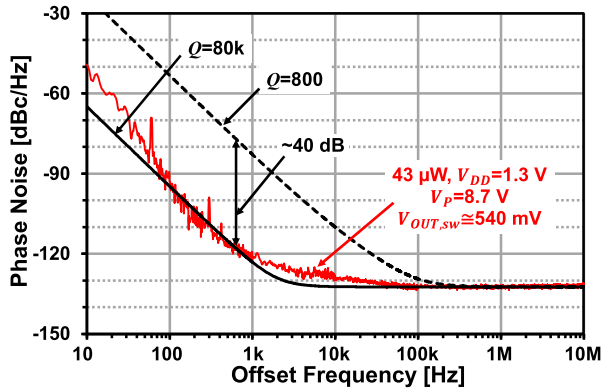

Fig. 11. Predicted phase noise plot (black solid line) generated using (31) and the simulated functions of Figs. 9 and 10 atop the measured phase noise (red line). The black dashed line predicts the phase noise performance when resonator Q (fictitiously) drops to 800 while maintaining constant motional resistance. Here, the flicker noise corner frequencies of M_1 and M_2 are found in simulation to be 16.6 and 1.6 MHz, respectively, while the flicker noise corner frequency of $\overline{v_{n,B}^2}$ is 648 kHz with the noise floor of 1.29×10^{-15} V^2/Hz.

forms [38]

$$S_{\phi,M1}(\Delta f) = \left(\Gamma_{\text{rms},M1}^2 + \frac{c_{0,M1}^2}{4} \cdot \frac{f_{c1}}{\Delta f}\right) \frac{\overline{i_{nT,M1}^2}/\delta f}{2(C_{\text{OUT}} V_{\text{OUT,sw}} \Delta f)^2}$$

$$S_{\phi,M2}(\Delta f) = \left(\Gamma_{\text{rms},M2}^2 + \frac{c_{0,M2}^2}{4} \cdot \frac{f_{c2}}{\Delta f}\right) \frac{\overline{i_{nT,M2}^2}/\delta f}{2(C_{\text{OUT}} V_{\text{OUT,sw}} \Delta f)^2}$$

$$S_{\phi,B}(\Delta f) = \frac{c_{0,M2}^2}{4} \cdot \frac{g_{m2}^2 \overline{v_{n,B}^2}/\delta f}{2(C_{\text{OUT}} V_{\text{OUT,sw}} \Delta f)^2} \quad (29)$$

where $\Gamma_{\text{rms},M1}$ and $\Gamma_{\text{rms},M2}$ are rms values and $c_{0,M1}$ and $c_{0,M2}$ are the first term ($n = 0$) in the Fourier series coefficients of $\Gamma_{M1}(\theta)$ and $\Gamma_{M2}(\theta)$, respectively; and $V_{\text{OUT,sw}}$ is the maximum voltage swing across the effective total capacitance at the output: $C_{\text{OUT}} = C_2 + C_1 C_3/(C_1 + C_3)$. The rms values of $\Gamma(\theta)$ effectively derive from conversion of HF thermal noise into phase noise, while the Fourier components, c_0, capture the conversion of the flicker noise. Since $\overline{v_{n,B}^2}$ comprises only flicker noise, $S_{\phi,B}(\Delta f)$ only has the c_0 term. Similarly, the phase noise power spectrum density due to the resonator voltage noise takes the form

$$S_{\phi,\text{RES}}(\Delta f) = \frac{\Gamma_{\text{rms,RES}}^2 \overline{v_{nT,\text{RES}}^2}/\delta f}{2(L_x I_{x,\text{sw}} \Delta f)^2} \quad (30)$$

where $I_{x,\text{sw}}$ is the maximum current swing going through the effective inductor of the resonator L_x. The total single-sideband phase noise spectrum density normalized to the carrier power (in dBc/Hz) then follows as the sum of these individual sources

$$\mathcal{L}(\Delta f) = 10 \log[S_{\phi,M1}(\Delta f) + S_{\phi,M2}(\Delta f) + S_{\phi,B}(\Delta f) + S_{\phi,\text{RES}}(\Delta f) + S_{\phi,fl}(\Delta f)] \quad (31)$$

where the final term represents the far-from-carrier (thermal) noise floor of the amplifier.

Fig. 11 shows the phase noise curve predicted by (31) using the extracted values of Table III overlaid atop measured data for the physically realized oscillator (discussed further in Section VI). In addition, the dotted curve models the same oscillator circuit with an equivalent resonator having a Q-factor of only 800. As expected, this reduced Q produces a marked reduction in the predicted phase noise performance, replicating the phenomenological behavior of Leeson's model and further emphasizing the importance of high Q to achieving low-phase-noise performance on a small power budget.

TABLE III
EXTRACTED VALUES FOR THEORETICAL PHASE NOISE PLOTS

Parameter [unit]	Q = 80k & 800	Parameter [unit]	Q = 80k	Q = 800
γ [-]	0.81	$V_{OUT,sw}$ [mV]	538	703
f_{c1} [MHz]	16.6	$\Gamma_{rms,M1}$[-]	2.13×10^{-5}	2.09×10^{-3}
f_{c2} [MHz]	1.60	$\Gamma_{rms,M2}$[-]	2.58×10^{-5}	2.32×10^{-3}
$f_{c,B}$ [kHz]	648	$\Gamma_{rms,RES}$[-]	1.40	150
$\overline{v_{nT,B}^2}/\delta f$ [V^2/Hz]	1.29×10^{-15}	$c_{0,M1}$[-]	8.46×10^{-7}	3.75×10^{-5}
C_{OUT}[fF]	357.5	$c_{0,M2}$[-]	-9.25×10^{-7}	-2.95×10^{-4}
$S_{\phi,fl}(\Delta f)$ [1/Hz]	5.79×10^{-14}	$I_{x,sw}$[μA]	28.34	43.84

For low-power applications, both phase noise performance and power consumption are important. For fair comparison of such oscillators, a figure of merit (FOM) that accounts for the total power consumption required to achieve a given phase noise takes the form

$$\text{FOM} = 10 \log\left(\mathcal{L}(\Delta f) \cdot \frac{P_{\text{diss}}}{1\ \text{mW}} \cdot \left(\frac{\Delta f}{f_o}\right)^2\right) \quad (32)$$

where P_{diss} is oscillator power consumption. Use of this FOM then allows even comparison of oscillators designed with differing power budgets and operating at different frequencies.

VI. Experimental Verification

To verify the oscillator operation model, a low-power amplifier IC was designed per the topology of Fig. 2 and fabricated using a 0.35-μm CMOS technology. Table II includes design and operating information for the constructed amplifiers. Here, the operation of M_2 with significantly reduced g_m compared with M_1 minimizes the noise contribution from the bias circuit, while C_{BP} effectively filters out high-frequency thermal noise. Although the entire die, shown in Fig. 12(a), occupies an area

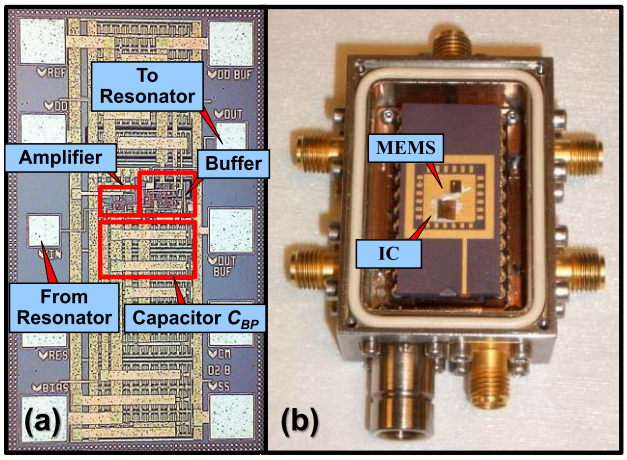

Fig. 12. (a) Die photograph of the custom-made IC. (b) Photograph of the packaged oscillator in a custom-designed vacuum box.

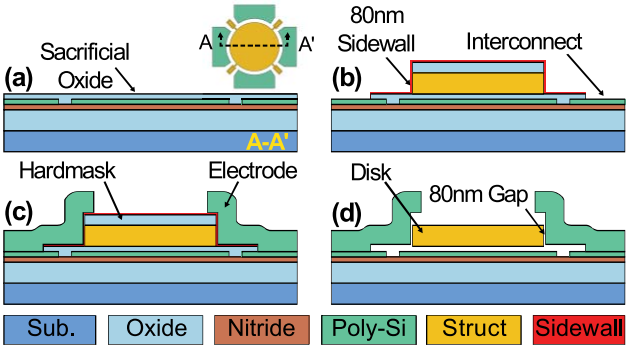

Fig. 13. Fabrication process flow for the polysilicon micromechanical disk resonator. (a)–(c) Resonator construction through repeated LPCVD polysilicon and oxide film depositions, lithography, and plasma etches, followed by a 49% HF wet etch process to remove the sacrificial oxide to yield the final released structure of (d).

of 900 μm $\times$ 500 μm, the actual sustaining amplifier with its biasing circuits only consumes about 60 μm $\times$ 45 μm, while the 44-pF C_{BP} occupies about 200 μm $\times$ 100 μm. The attenuation of noise at node V_b in Fig. 2 depends on the pole, $g_{m,b2}/C_{BP}$, where $g_{m,b2}$ is the transconductance of diode-connected transistor M_{b2} in Fig. 2 and $1/g_{m,b2}$ is the resistance looking into M_{b2}. This pole is at 137 and 175 kHz for oscillators operated at 43 and 110 μW, respectively. For the same attenuation, the area of C_{BP} can be reduced easily by 2–4 times by simply decreasing $g_{m,b2}$. The rest of the IC area comprises an on-chip buffer used to drive the 50 Ω desired for external measurement systems, 2) bypass capacitors to further reduce noise on dc supply lines, and 3) bond pads.

Using (3) together with Table I, a wine-glass disk MEMS resonator was designed for operation at 61 MHz, which calls for a disk radius of 32 μm. Fig. 13 summarizes the surface micromachining process used for fabrication based on the process mentioned in [6]. Here, phosphorus-doped polysilicon deposited via low-pressure chemical-vapor deposition (LPCVD) at 615 °C provided all resonator structure, electrode, and electrical interconnect material. A high-temperature oxide (HTO) sidewall sacrificial deposition defined the 80-nm

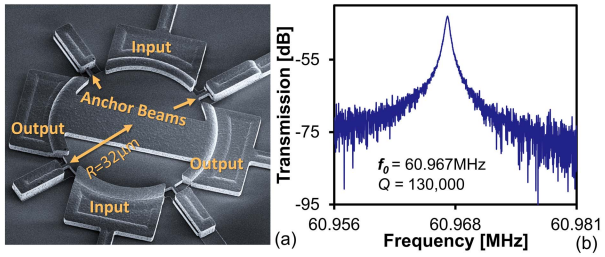

Fig. 14. (a) SEM of a fabricated MEMS disk resonator. (b) Measured frequency response with $V_{PCM} = 5$ V.

resonator-to-electrode gaps. A chemical–mechanical polishing (CMP) step before structural polysilicon deposition and patterning provided the planar surface desired for precise resonator structure lithography. Following fabrication, structures were released in 49% HF to yield the final device imaged in the SEM of Fig. 14(a), which sits alongside a measured frequency characteristic for one of the better devices, showing a device Q of about 130 000. Note that this Q is higher than that of most others, which averaged around 80 000. It is possible that this resonator had thinner supports with better placement than others, which perhaps allowed it to better suppress energy loss through anchors. Devices with fewer supports, e.g., two instead of four, also consistently exhibited the highest Q values.

Fig. 12 shows the complete oscillator, comprising the amplifier die bond-wired to the resonator and package leads. To maintain high (i.e., over 50 000) resonator Q as needed to minimize phase noise, as well as maintain the required loop gain [37], the MEMS-based oscillator must operate in a stable vacuum environment. Here, a custom-made miniature vacuum chamber, shown in Fig. 12(b), provides the needed environment while enclosing a printed circuit board (PCB) that houses the MEMS/CMOS device package. The chamber also provides electrical feedthroughs to allow connecting to outside instrumentation. The output of the oscillator was measured using an Agilent E5500 phase noise test setup configured to use a low-noise PLL-based measurement.

When biased with an appropriate value of V_P (see Table II) that "turns on" the MEMS resonator and provides positive loop gain, the oscillator generates the typical output waveform shown in Fig. 15(a), with equivalent output spectrum in Fig. 15(b). Fig. 16 gauges oscillator startup time, with the red curve demonstrating startup at a bias point just above that needed to produce oscillation, showing a modest 13-ms time constant. Slightly increasing resonator bias voltage from 7.4 to 7.8 V increases total loop gain, producing the blue curve with a much smaller 5-ms time constant, as predicted by (25).

Fig. 17 shows the measured phase noise data for the Pierce oscillator alongside comparison data for a TIA-based oscillator [12], employing the same MEMS resonator design. Here, the Pierce oscillator achieves -117 dBc/Hz at 1-kHz offset and -139 dBc/Hz at far-from-carrier offsets from its 61-MHz oscillation frequency. Comparing this phase noise performance with that predicted by the analysis of Section V in Fig. 11 yields excellent agreement with theory. The slight increase in phase noise at offset frequencies below 50 Hz from that

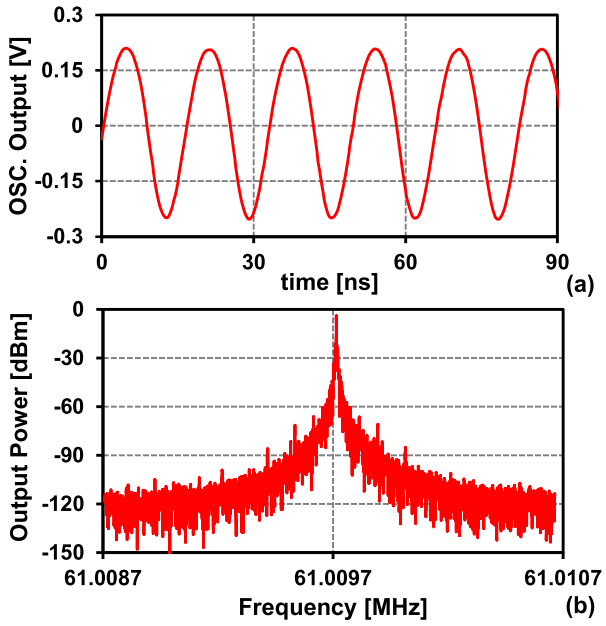

Fig. 15. (a) Pierce oscillator output waveform measured on an oscilloscope and (b) output spectrum as measured on a spectrum analyzer.

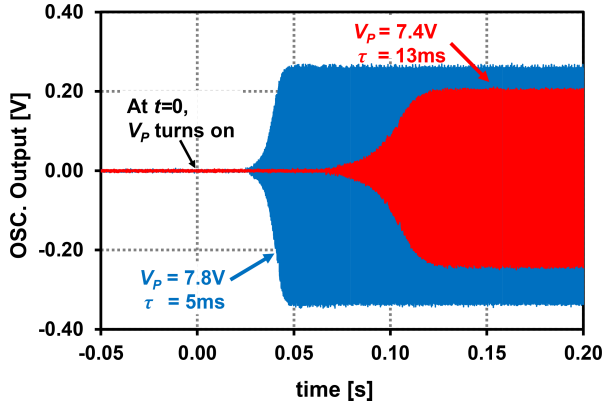

Fig. 16. Measured startup time response of the oscillator when resonator bias voltage, V_P, is turned on at $t = 0$. The increase in resonator bias voltage increases the total loop gain, thereby decreasing the startup time of the blue curve compared with the red as, expected from (25).

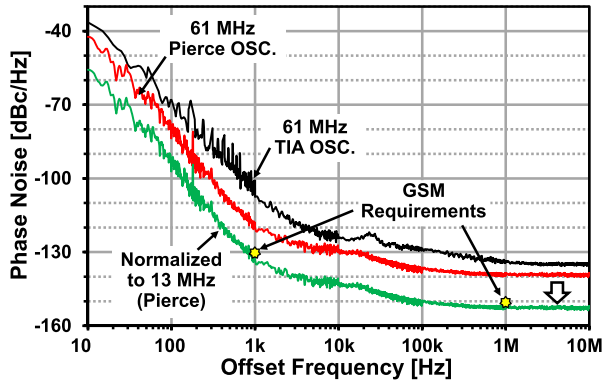

Fig. 17. Measured phase noise of 61-MHz oscillators comparing the new Pierce topology and an older TIA topology similar to [12], as well as the Pierce oscillator phase noise divided down to 13 MHz (for later comparison with other oscillators).

predicted is likely due to additional random-walk variations from thermal, noise aliasing, or other factors that are not captured in the phase noise model [15], [41].

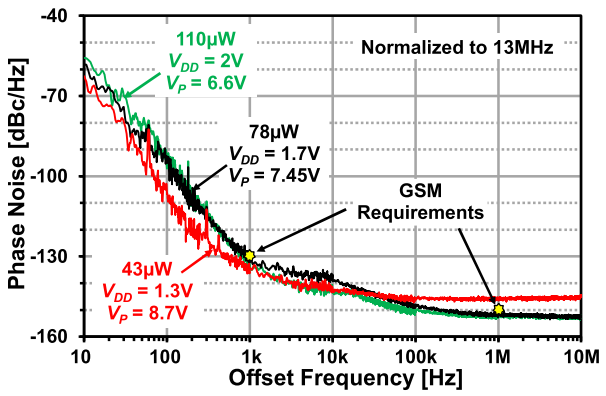

Fig. 18. Measured phase noise of the oscillator operating on varying resonator and supply voltages. A reduction in V_{DD} and I_{BIAS} can be seen to decrease power consumption by 61% with only a modest decrease in phase noise performance.

TABLE IV
OSCILLATOR PERFORMANCE COMPARISON

DEVICE TYPE	This work		WG array [10]	AlN [18]	AlN [42]	FBAR [16]	Quartz [43]
	43μW	78μW					
f_O [MHz]	61	61	61	4.9	204	2000	10
Power [μW]	43	78	350	120	47	25	~1500
IC Process	0.35μm CMOS		0.35μm CMOS	0.18μm CMOS	65nm CMOS	0.18μm CMOS	N/A
V_{DD} [V]	1.3	1.7	3.3	1	0.55	0.35	N/A
$\mathcal{L}(\Delta\omega)$ @1kHz [dBc/Hz][1]	-135	-130	-136	-130	-101	-122	-135
$\mathcal{L}(\Delta\omega)$ Noise Floor [dBc/Hz][1]	-147	-152	-150	-147	-141	-183	-150
FOM @1kHz [dB]	-231	-225	-223	-221	-202	-220	-211

[1]Normalized to 13 MHz.

When divided down to 13 MHz (for comparison with other oscillators), these phase noise marks correspond to −130 dBc/Hz at 1-kHz and −152 dBc/Hz far-from-carrier. This Pierce oscillator not only provides phase noise improvements of 7 dB at 1-kHz offset and 7-dB far-from-carrier versus the TIA version of [12] using a similar single disk; it also reduces power consumption down to 78 μW, a factor of 4.5 times smaller.

Fig. 18 shows the phase noise measurements for the Pierce oscillator that investigates the degree to which the increase in resonator dc-bias V_P allows lower supply voltages and, hence, lower power consumption. Here, a 0.85-V increase in V_P allows V_{DD} and I_{BIAS} reductions that decrease overall power consumption from 110 to 78 μW, with very little degradation of phase noise. A further increase in V_P to 8.7 V allows yet lower power consumption of 43 μW, though at the cost of slight increases in far-from-carrier phase noise due to the resultant decrease in oscillator swing. Use of (32) yields Table IV, where the present Pierce oscillator achieves the top FOM at 1 kHz amongst the published chip-scale oscillators to date.

VII. Conclusion

The demonstrated 61-MHz capacitive-gap transduced wine-glass disk Pierce oscillator capable of meeting mobile phone specifications while using only 78 μW of power marks a milestone for MEMS-based frequency control technology. Compared with previous TIA-based renditions, this oscillator reduces power and area consumption by 4.5 times and 10 times, respectively. Increasing the bias voltage of the resonator by just 1.25 V allows operation at a still lower 43 μW of power, at the cost of only a few decibels in far-from-carrier offset phase noise. When power consumption is considered, to the best of our knowledge, this now posts the highest FOM of any published chip-scale oscillator to date for 1-kHz offset frequency. In addition, the circuit analysis presented here predicts that the power consumption can be further reduced to single-digit μW or lower by reducing device electrode-to-resonator gap spacing, as well as minimizing trace resistance and parasitic capacitance, e.g., via bond pad size reduction. Circuit design optimizations, e.g., adjusting overdrives, should also garner further reductions in power consumption.

Whether or not such further improvements are achieved, the power reduction already demonstrated while achieving mobile phone-compliant phase noise marks makes a compelling case for application to future low-power wireless applications. Certainly, the demonstrated oscillator bests traditional crystal oscillator technologies and their battery-unfriendly milliwatts of power while offering the single-chip form factor desired for mobile electronics. Pierce oscillators such as these will likely improve traditional wireless transceiver performance and may even see action in future fully MEMS-based architectures [33], [44], [45].

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In 1995, he joined the faculty of the University of Michigan, Ann Arbor, MI, USA, where he was a Professor with the Department of electrical engineering and computer science until mid-2006. In 2006, he joined the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, where he is currently the Conexant Systems Distinguished Professor and a Co-Director of the Berkeley Sensor & Actuator Center. His research interests focus upon microelectromechanical systems (MEMS) and include integrated micromechanical signal processors and sensors, merged circuit/micromechanical technologies, optomechanical devices, RF communication architectures, and integrated circuit design and technology. In 2001, he founded Discera, Inc., San Jose, CA, USA, a company aimed at commercializing communication products based upon MEMS technology, with an initial focus on the very vibrating micromechanical resonators pioneered by his research in past years. He served as the Vice President and the Chief Technology Officer (CTO) of Discera until mid-2002, at which point he joined the Defense Advanced Research Projects Agency (DARPA) on an IPA, where he served for four years as the Program Manager of ten different MEMS-centric programs in the Microsystems Technology Office of DARPA.

Dr. Nguyen received the IEEE Cady Award in 2006, the IEEE Robert Bosch Micro and Nano Electro Mechanical Systems Award in 2017, and together with his students has garnered more than 12 best paper awards from IEEE conferences and journals focused on frequency control and MEMS. He was the Technical Program Chair of the 2010 IEEE International Frequency Control Symposium and the Co-General Chair of the 2011 Combined IEEE International Frequency Control Symposium and European Frequency and Time Forum, as well as the Co-General Chair of the 2017 IEEE International Micro Electro Mechanical Systems Conference. From 2008 to 2013, he served as the Vice President of Frequency Control in the IEEE Ultrasonics, Ferroelectrics, and Frequency Control Society, after which he became the society President from 2016 to 2017. He is currently the Acting President of the IEEE MEMS Technical Community. From 2007 to 2009, he served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society.