Fabrication of Linear Array and Top-Orthogonal-to-Bottom Electrode CMUT Arrays With a Sacrificial Release Process

Benjamin A. Greenlay and Roger J. Zemp

Abstract—**The microfabrication processes for sacrificial-release-based capacitive micromachined ultrasound transducer arrays are provided with an emphasis on top-orthogonal-to-bottom electrode 2-D arrays. These arrays have significant promise for high-quality 3-D imaging with reduced wiring complexity compared with fully wired arrays. The protocols and best practices are outlined in significant detail along with design considerations and notes of caution for pitfalls and factors impacting yield.**

***Index Terms*—Capacitive micromachined ultrasound transducers (CMUT), microelectromechanical systems, microfabrication, process flow, sacrificial release, yield factors.**

I. Introduction

SINCE their inception, capacitive micromachined ultrasound transducers (CMUTs) have captured the attention of an increasing number of research labs and companies throughout the world for a wide variety of applications including biomedical ultrasound imaging, therapy, imaging therapy, nondestructive testing, and air-coupled ultrasonics [1]–[4]. While a variety of fabrication methods and architectures have emerged, many of the methods can be summarized as falling into categories of wafer-bonded or sacrificial release [5]–[9]. Often these fabrication techniques are provided in summarized form, yet there are many best practices and pitfalls to be aware of. It is the purpose of this paper to outline a detailed story of the microfabrication process involved in two CMUT architectures of key interest to researchers and companies today: linear arrays and the so-called top-orthogonal-to-bottom-electrode (TOBE) 2-D CMUT arrays.

We focus on sacrificial release-based fabrication and provide substantial detail about the fabrication methods with specific attention to TOBE arrays. These TOBE arrays offer significant promise for 3-D ultrasound imaging with significantly reduced wiring complexity compared with fully wired arrays. Our TOBE architecture is shown in Fig. 1. Similar piezoelectric-based crossed electrode arrays were first proposed by Morton and Lockwood [10] and Démoré *et al.* [11] and developed by others such as Daher and Yen [12] and Yen [13]. These were later developed as CMUT arrays by Rasmussen and Jensen [14], Chee *et al.* [15], Christiansen *et al.* [16], and Wygant *et al.* [17]. TOBE CMUT arrays allow operation modes not possible with previous piezoelectric crossed electrode arrays. Examples of these arrays are already being tested in practice by Nikoozadeh *et al.* [18] and Zahorian *et al.* [19] with TOBE ring arrays integrated into catheters for 3-D imaging. By biasing a column and transmitting or receiving along a row with all other rows and columns grounded, dominant element actuation and sensitivity is achieved at the row–column intersection [9], [20]. The concept of dominant element sensitivity is potentially powerful because more complicated pulse sequences can be built up using the principle of superposition. The ability to control biasing in parallel with transmit–receive operations on only rows and columns promises potential image quality improvements over more traditional orthogonal linear array operations involving one-way transmit focusing with orthogonal one-way receive focusing.

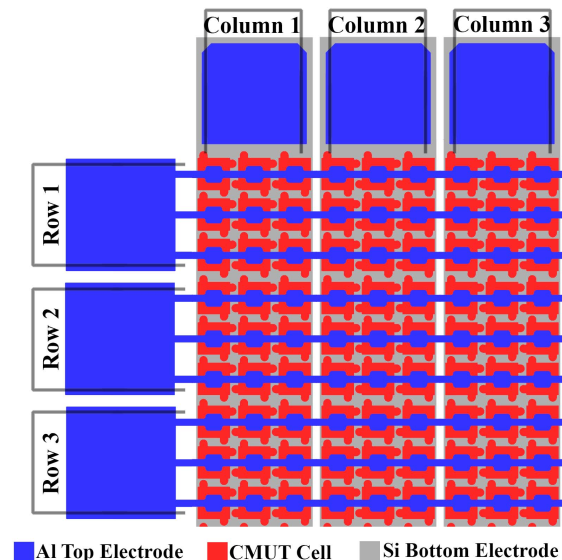

Fig. 1. TOBE architecture with orthogonal aluminum row electrodes and silicon column electrodes.

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TOBE arrays promise the potential of very large arrays, potentially occupying a whole wafer for whole organ imaging such as breast cancer screening. Such arrays could be the ultrasound equivalent of X-ray flat-panel detector arrays and could help to decouple operator dependence in ultrasound scanning in place of automated electronic scanning. Larger arrays, which do not yet exist, offer a larger field of view, allowing operators to more easily find and image the area of interest, but could require additional operator training and equipment to ensure proper sensor contact. To reach this aim, robust designs and fabrication schemes are needed with very high yield. In addition, such arrays need to be robust to dead elements in a way that does not compromise entire rows or columns or even whole arrays. We present a fabrication method and architecture, which shows promise to meet these high standards. We outline this process in detail and hope it will prove to be of value to researchers and industrial parties.

The fabrication methods are similar to originally proposed sacrificial release processes; however, we present two new additions to these processes specific to the fabrication of TOBE arrays [7], [9]. Previously described fabrication methods used deep reactive ion etching (DRIE) to separate the bottom electrode columns. This differs from previous linear array sacrificial release fabrication. These trenches can cause a number of fabrication challenges in subsequent steps. For example, unwanted metal would often accumulate in these trench areas, after top electrode patterning, and would be difficult to remove. This had a consequence of short-circuiting rows in an undesirable fashion. In addition, residual polysilicon from the sacrificial layer can also remain in these trench areas. When etched, these films can compromise device hermeticity. In this paper, we introduce an anisotropic etching step producing angled bottom electrode trench sidewalls, which improves lithography and enhances overall functionality and device yield. We detail both the previous DRIE approach and the proposed anisotropic etching process, which can both be fabricated using the same photomasks. Many papers provide only brief mention of fabrication details. This paper, in contrast, is meant to provide significant fabrication details and highlight points of significance, practices, and pitfalls relevant to TOBE arrays for researchers with less experience with standard microfabrication techniques.

II. Design Considerations

A. Starting Materials

Original sacrificial release CMUTs were fabricated on doped silicon prime wafers, which is appropriate when a contiguous bottom electrode is sufficient. TOBE CMUT arrays require bottom electrode patterning. To accommodate this, we choose silicon-on-insulator (SOI) wafers with a highly doped device layer that will be patterned to form bottom electrodes. The thickness of the device layer is of significance. If the layer is too thin, bottom electrode traces will experience significant resistive losses, which could degrade performance along traces. If the device layer is too thick, it will create significant challenges for routing top metal electrode traces in the orthogonal direction for TOBE arrays. Wafer-bonded CMUTs may prove advantageous in this regard as bottom electrodes can be made arbitrarily thick. Metal traces are not feasible for the bottom electrode in our approach as process temperatures will exceed their melting point. In this paper, we use 4-μm-thick device layer SOI wafers and introduce methods for patterning this device layer to form bottom electrodes. We chose boron-doped device layers with 0.01–0.02 Ω cm resistivity with a 0.4-μm buried oxide (BOX) layer and 505-μm undoped handle (Okmetic, BSOI 500–0.4–4). For the architecture in question, the BOX layer is meant as an etch-stop and isolation layer between the bottom electrodes and the substrate silicon.

B. Transducer Modeling and Design Considerations

Modeling the CMUT performance prior to mask design or fabrication is a key task. While it is beyond the scope of this paper to go into any detail regarding this modeling, we mention some key papers and tools of significance to our work.

Key design parameters impacting acoustic performance include gap height, membrane thickness, membrane size, and intercell spacing. These parameters impact the resonance frequency in air and immersion, snapdown voltage, and electromechanical efficiency.

Analytical models for static membrane deflection exist as described by Cour *et al.* [21] and Wygant *et al.* [22] for circular and square membranes, although these models do not necessarily account for residual stress. More recently, Engholm *et al.* [23] have developed a general multilayer anisotropic plate equation for modeling a CMUT cell with residual film stresses. These models can prove important for calculations of snapdown voltage and estimates of unbiased resonance frequencies of the first modal frequency. Higher order modal shapes and rectangular membranes currently require finite-element packages for simulation. These finite-element simulations are often limited to simulating only a few CMUT cells due to the mesh complexity and processing time. Other modeling approaches, such as the work described in [24], are able to simulate large number of CMUT membranes using a 2-D surface mesh to greatly reduce the processing time and resources. The analytic static deflection models may include membrane anisotropy. These models have been extended to equivalent circuit models of dynamic operation including electrical–mechanical and membrane-acoustic effects important for electrical and acoustic impedance matching analysis [25]–[27]. Recent equivalent circuit models permit full and accurate nonlinear capabilities rather than linearized small-signal approximations originally introduced. They also permit large-scale simulations including important effects of mutual acoustic impedance, which can impact net center frequency and bandwidth and potentially account for resonances associated with Rayleigh–Bloch waves that degrade imaging performance [28]. Presently, such mutual acoustic impedance effects have primarily been modeled using equivalent circuit simulators with only circular membrane geometries.

We use analytic calculations and finite-element models to estimate single membrane static and dynamic behavior, and equivalent circuit models to estimate behavior of multiple membranes in arrays.

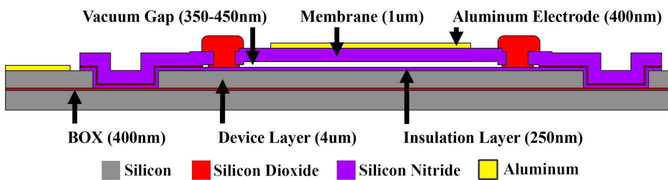

Fig. 2. Cross-section schematic of a basic CMUT sacrificial release cell.

In our work, we targeted ~2.5-MHz immersion operation and were practically constrained to make gaps no smaller than ~250–300 nm. Gaps smaller than this mean even thinner etching channels are required for sacrificial release (currently ~100 nm in thickness), which create challenges for efficiently etching these layers. Present gap thicknesses may lead to high but usable operation voltages; future work will also aim to develop smaller gap heights, potentially smaller than 100 nm similar to [29]. In addition, while thinner gaps may lead to high receive sensitivity, reduced membrane motion is possible, potentially limiting transmit power in precollapse mode. We use ~1-μm membrane thicknesses. With this membrane thickness, we target 52-μm square membranes to produce the desired immersion resonance frequencies. The collapse voltage for these membranes was simulated to be ~115 V with a resonance frequency of ~2.7 MHz in immersion and ~7.0 MHz in air, using a model similar to [30]. The cross section of a basic CMUT cell is shown in Fig. 2.

It should additionally be mentioned that we currently design CMUTs to operate in precollapse mode and test them with a bias voltage close to 80% of the snapdown voltage. At this bias voltage, this electromechanical efficiency is only ~20%. This provides a safe operation zone to avoid membrane collapse due to variability in the snapdown voltage caused by process nonuniformities. With additional testing of membrane uniformity, this bias voltage can be increased for better performance of the devices. An electromechanical efficiency of ~80% can be expected at bias voltages closer to the snapdown voltage of these devices. It has previously been shown that collapse-mode or collapse snapback operation can lead to greater transmit powers [31], [32]. However, collapse-mode operation devices are susceptible to dielectric charging challenges, which can lead to altered device performance and permanent membrane collapse, thus reducing reliability. Recent work suggests that such charge effects can be greatly minimized or eliminated by engineering dielectric quality and minimizing surface roughness to reduce Fowler–Nordheim and other dielectric tunneling mechanisms [33]–[35]. In this paper, we simply aim to avoid such charging effects by keeping to precollapse operation modes.

III. Fabrication Overview

Fig. 3 shows an overview of our fabrication scheme. An SOI wafer with a boron-doped device layer is patterned using a highly anisotropic DRIE [or potassium hydroxide (KOH) etching, to be discussed] to define bottom electrodes, with the BOX layer serving as an etch-stop [Fig. 3(a)]. Then a low-pressure chemical vapor deposition (LPCVD) silicon nitride is deposited as a bottom

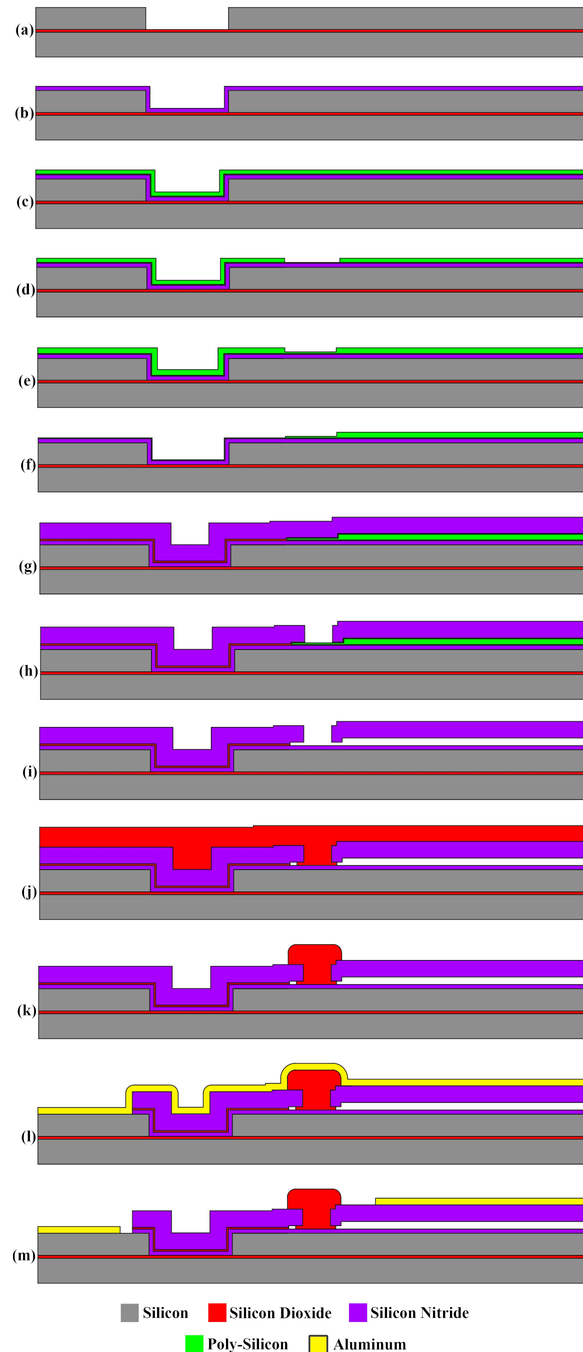

Fig. 3. Our modified sacrificial release CMUT fabrication process starting on an SOI wafer using the DRIE trench etching process. (a) Etching of the SOI device layer. (b) Deposition of silicon nitride isolation film. (c) Deposition of silicon dioxide protection layer and first poly-silicon sacrificial layer. (d) Etching of the first sacrificial layer. (e) Deposition of the second poly-silicon sacrificial layer. (f) Etching of both sacrificial layers. (g) Deposition of second silicon dioxide protection layer and thick membrane silicon nitride film. (h) Etching access holes in silicon nitride membrane to expose the sacrificial region. (i) Chemical etching of combined sacrificial layers and release of the membrane structure. (j) Conformal deposition of silicon dioxide sealing film. (k) Patterning the silicon dioxide sealing film into plugs. (l) Etching through the silicon nitride films to access the bottom silicon electrode and sputtering the aluminum film. (m) Etching the aluminum film to form top and bottom electrodes.

dielectric layer and KOH etch-stop [Fig. 3(b)]. Plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide is next deposited and will act as an etch-stop layer for reactive ion etching (RIE) of the sacrificial layers. LPCVD polysilicon

is next deposited as the first sacrificial layer [Fig. 3(c)]. This is patterned to define the gap area [Fig. 3(d)]. Another LPCVD polysilicon deposition [Fig. 3(e)] and patterning step provides definition of low-height etching channels, while slightly increasing the height of the sacrificial polysilicon in the gap area [Fig. 3(f)]. A second PECVD silicon dioxide layer is then deposited as a top protection layer and RIE etch-stop. LPCVD silicon nitride is then deposited as the device membrane over the sacrificial layers [Fig. 3(g)].

Following the LPCVD deposition of the silicon nitride membrane, holes are etched through the membrane to access the polysilicon layer [Fig. 3(h)]. Sacrificial etching is next performed using KOH wet etching until membranes are released [Fig. 3(i)]. Although the etch rate of silicon dioxide is much slower than polysilicon, the silicon dioxide layer beneath the gap and etch-channel areas will be completely etched away during the long sacrificial etches. Any overetching along the dual silicon dioxide interface should be minimal, due to this low selectivity (typically between 50:1 and 100:1) and timed sacrificial etching. Etch holes are sealed using low-stress PECVD silicon dioxide [Fig. 3(j)], which is etched to form sealing plugs without coating the CMUT gap [Fig. 3(k)]. CMUT cavity formation and sealing is complete after this step. Next, access holes to the bottom silicon electrodes are formed by RIE. Finally, aluminum metallization [Fig. 3(l)] and patterning is performed to form the top membrane, top interconnects, top electrode bond pad, and bottom electrode bond pad [Fig. 3(m)]. This aluminum film is deposited using a magnetron sputtering system.

This process is similar to but different from the original sacrificial release fabrication schemes [7]. An advantage of this method is an etch-stop for each important etching step, permitting high-etch-rate high-throughput DRIE to be used in an industrial fab without optimizing the etch depths and without worrying about consequences of overetching for a majority of the process steps. Some careful timed etching is still required for the etching of the sacrificial release holes to prevent etching through the bottom silicon nitride insulation layer. For the sacrificial layers, we opted to use two patterned layers of polysilicon to create the gap structure. This allows for the full gap thickness to be defined as the thickness of the combined layers, while the remaining polysilicon in the sacrificial release channels is much thinner to allow for easier silicon dioxide sealing through PECVD and to improve the overall yield of the devices. This patterned SOI sacrificial release process architecture also permits independent patterning of top and bottom electrodes, key to the success of the proposed device.

IV. Mask Design Considerations

In designing masks for fabrication, a number of things must be considered. In particular, we must note that minimum feature sizes in our designs are limited by our mask writer (Heidelberg Instruments, DWL200) to 1 μm. In addition, there are alignment tolerances present for each mask alignment system, and with contact lithography, this error could be around 2 μm even with best efforts. Thus, for every mask step, one must consider consequences of misalignment and

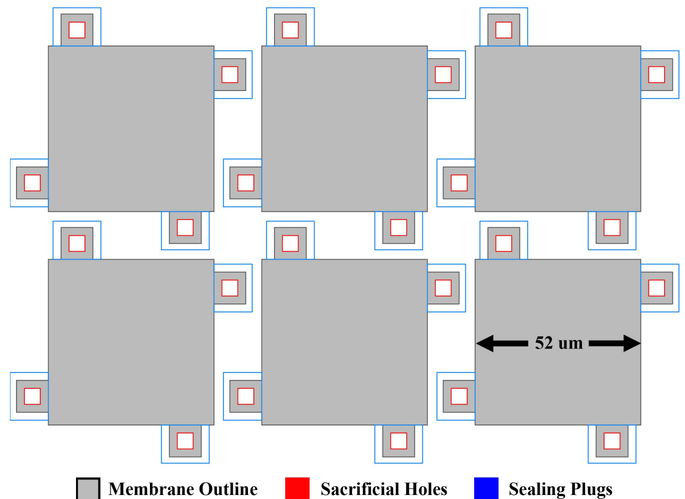

Fig. 4. Top view of CMUT cell design. Each membrane has four separate sacrificial etching channels to prevent any defects or damage to one membrane from compromising the hermeticity of neighboring membranes.

design the masks to allow for small errors. One example of such a consequence is if etch holes are misaligned. This could lead to the absence of an etch-stop and etching into the bottom electrode with disastrous consequences during a sacrificial etch. These issues eventually determine how close together CMUT membranes can be. An additional consideration concerns consequences of local breaches of membrane hermeticity. If one membrane is compromised, it should not ideally compromise neighboring membranes, which would be the case if CMUT etching channels connected multiple cells. Our approach is to have an etching channel for each membrane, which is isolated from other membranes as shown in the mask design of Fig. 4.

V. Fabrication Details

For this procedure, the devices being fabricated have lateral dimensions on the order of micrometers and heights and layer thicknesses less than a micrometer. Therefore, it is important that these devices should be fabricated in a cleanroom environment to help eliminate particle defects and improve the fabrication yield.

This process contains several optimized steps and suggests different methods for patterning the doped silicon device layer to potentially improve upon the device yield. At the beginning of the process flow, there is a section that discusses two different methods for patterning the silicon device layer, either by DRIE or KOH etching. One of the main factors that determine the thickness of the bottom electrode device layer is the aluminum electrode deposition. If the trenches are too deep during this first process step, then it is possible that the aluminum may fully coat these trenches, thus failing to connect the top electrodes of each membrane. This creates a tradeoff between minimizing resistance in the silicon traces and allowing for successful fabrication of these devices.

One alternative to this DRIE process is using KOH chemical etching of the silicon layer. Due to the crystal orientation of the SOI wafers, this etching process will create slanted sidewalls with an angle of 54.7° [36]. This should allow for a more gradual transition between the top and the bottom of these trench

features and improve the aluminum deposition and patterning in these regions. The tradeoff with this process is that these diagonal walls will add additional design requirements to the height and width of the trench masks to ensure that sufficient separation still exists between the electrodes following the etch. In addition, this chemical etching requires a different masking material, as photoresist will be rapidly etched in the KOH solution. For the outlined process, a thin silicon dioxide film was grown using thermal oxidation and patterned with an extra few process steps to serve as a masking material. The thickness of this masking film needs to be carefully calculated based on the thickness of the silicon device and the KOH etching selectivity (typically between 50:1 and 100:1). After the wet chemical etch, the remaining silicon dioxide film should be thinner than 50 nm to allow for a short buffered oxide etch to remove the remaining mask before etching too far into the BOX layer of the SOI wafer.

A. Caution and Safety During the Fabrication Process

There are many safety considerations that need to be assessed before working with the equipment and etching processes outlined in this process flow. Some of the process steps involve high temperatures, dangerous gases, ultraviolet radiation, high voltage, and mechanical equipment. The required safety precautions and personal protective equipment specific to each user's facility should be addressed before attempting any of the following processing steps. Several of the chemical etching processes used to fabricate these devices have dangerous properties and require extra safety measures.

B. Lithography Procedure

The following lithography process is repeated several times throughout the fabrication process. While the type of photoresist, spinning speeds, exposure, and development times change for some of the lithography steps, the main process is unchanged. Refer to these steps for each of the lithography processes.

i) Pour ∼5 mL of photoresist onto the center of the wafer. **CRITICAL**: Perform this step slowly to prevent any air bubbles from forming in the poured photoresist.
ii) Spin the photoresist coated wafer first at the spreading speed for 10 s to spread the photoresist, before ramping up the spinning speed to the desired speed.
iii) Transfer the wafer to a hot plate and soft bake for the desired time and temperature for the given photoresist. For HPR photoresist, this baking step is 90 s at 120 °C. **CRITICAL**: Ensure that the hot plate is level to prevent unwanted changes in the photoresist thickness.
iv) Remove the wafer from the hot plate and allow it to cool and rehydrate at room temperature for 15 min.
v) Load a photomask and the photoresist coated wafer onto a mask aligner, roughly center the wafer for the first mask, or carefully aligning the alignment marks for subsequent masks, and bring them into contact.
vi) Expose the wafer to UV light for the required photoresist dosage.
vii) Place the wafer in photoresist developer for the required development time and gently agitate the solution until the photoresist is visibly developed. Our developer solution is composed of a 1:4 dilution of Microposit 351 developer (Dow Electronic Materials, 10016652) to deionized water.
viii) Once developed, quickly remove the wafer from the developing solution and rinse both sides with deionized water to prevent overdevelopment of the wafer.

C. Wafer Preparation and Cleaning

Before beginning the fabrication process, it is important to properly clean the silicon substrates to remove any organic contaminants and native oxides that may cause defects in the devices.

1) Piranha clean the wafers in a 3:1 solution of sulfuric acid (J.T. Baker, 9684-05) and hydrogen peroxide (J.T. Baker, 2190-03) for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
2) Use pressurized filtered nitrogen or air to dry to wafer.
3) Etch any native oxide on the wafers with a buffered oxide etching solution (J.T. Baker, 5175) for 1 min. Following the oxide etch, rinse the wafers five times in a deionized water dump rinser.

D. Patterning of the Bottom Device Layer Electrodes for Cross Electrode Designs

For TOBE device fabrication, the silicon device layer of an SOI wafer must be patterned into strips of silicon for each of the bottom electrode rows. When fabricating linear array devices using highly doped silicon prime wafers, this section of the process flow can be omitted and instead proceed with Step 6 and the fabrication of the polysilicon sacrificial layers.

4) Patterning and etching of the bottom device layer trenches to create rows of separated elements. This procedure can be performed either using a DRIE process (A) for a very anisotropic profile or through KOH chemical etching (B) to create slanted sidewalls on the trenches. Method (A) was previously discussed [9]; however, method (B) is a new approach that provides fewer problems for the top electrode metallization patterning, which will be highlighted in Section V.
   a) *Reactive Ion Trench Etching:*
      i) Lithography mask 1, photoresist patterning of the device layer trenches using the recipe in Table I. Approximate photoresist thickness 1.2 μm.
      ii) RIE of the silicon device layer using an Oxford Estrelas etching system or equivalent. This Estrelas uses a Bosch etching process with alternating polymer deposition and etching steps to create very anisotropic sidewalls. The etching recipe is shown in Table II for a 4-μm silicon etch with a standard overetch included. A total of 55 cycles were used, with a time of ∼1.2 s per combined deposition and etching cycle.
      Troubleshooting: Calibration of this etch rate is required for reliable patterning of the silicon

TABLE I

STANDARD HPR-504 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

TABLE II

OXFORD ESTRELAS SILICON BOSCH ETCHING RECIPE

Deposition	C4F8 Flow Rate (sccm)	160
	SF6 Flow Rate (sccm)	10
	Pressure (mTorr)	65
	ICP Power (W)	1500
	Temperature (C)	0
Etching	C4F8 Flow Rate (sccm)	10
	SF6 Flow Rate (sccm)	360
	Pressure (mTorr)	80
	ICP Power (W)	2250
	Temperature (C)	0

device layer. This can be achieved using stylus step height measurements, with an AlphaStep or Dektak machine, or interference measurements with an ellipsometer. This process can be safely overetched by 10%–20% to ensure complete etching of the small trench features as the Oxford Estrelas system with this recipe has a high etch selectivity between silicon and silicon dioxide (∼200:1).

iii) Remove the photoresist by sonicating the wafer for 5 min in an acetone (J.T. Baker, 9005-05) bath, before rinsing with isopropanol (J.T. Baker, 9079-05).

b) *KOH Trench Etching Process:*

i) Dry thermal oxidation to create the 100-nm silicon dioxide mask. Load wafers onto a quartz boat and push the boat into the center of a Thermco MiniBrute stack furnace, or equivalent. Oxidize the wafers at 1100 °C for 3 h using an oxygen and nitrogen gas mixture.
Troubleshooting: Actual oxidation time will depend on calibration curves run on each system and the combination of gases available. For a more precise oxidation, pure nitrogen can be used during the temperature ramping and then switched over to dry oxygen for the actual processing once the furnace reaches 1100 °C. Similarly, pure nitrogen can also be used when cooling down the furnace to prevent further oxidation past the required thickness.

ii) Prime the oxidized wafer for lithography by coating them in hexamethyldisilizane (HMDS) to promote better adhesion between the photoresist and the silicon dioxide film. This can be deposited by using a Yield Engineering Systems vapor prime tool, or equivalent, with a standardized recipe shown in Table III.

iii) Lithography mask 1, photoresist patterning of the device layer trenches with the recipe shown in Table IV. Approximate photoresist thickness 1.2 μm.

TABLE III

HMDS VAPOR PRIME DEPOSITION RECIPE

Deposition Pressure (Torr)	1
Deposition Temperature (C)	150
Deposition Time (min)	5

TABLE IV

STANDARD HPR-504 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	2.5
Development Time (s)	25

iv) Etch the exposed silicon dioxide layer with a buffered oxide solution for 2.5–3 min. Following the oxide etch, rinse the wafers five times in a deionized water dump rinser.
Troubleshooting: Etching times depend on a calibration with the etching solution to be used. Film can be safely overetched as the selectivity to silicon is effectively infinite.

v) Remove the photoresist by sonicating the wafer for 5 min in an acetone bath, before rinsing with isopropanol.

vi) Etch the exposed silicon layer in a heated KOH chemical bath. Prepare a solution of 32% KOH by mixing stock KOH (J.T. Baker, 3144-03) with deionized water. Heat the solution to 90 °C and stir using a magnetic stirring rod. Etch the wafers for 5–6 min in the heated solution before rinsing five times in a deionized water dump rinser.
Troubleshooting: Actual etching times should be calibrated to the equipment being used. Precise timing for this etch is important as the KOH solution is also slowly etching the silicon dioxide mask and overetching may completely remove this mask and allow for etching of the entire silicon device layer. The thickness of the masking oxide was chosen to allow for nearly complete etching in the KOH solution, so the following oxide etching step would be short enough to prevent too much over etching of the BOX while removing the remaining masking oxide.

vii) Etch the remaining silicon dioxide mask layer with a 1-min buffered oxide etch. Following the oxide etch, rinse the wafers five times in a deionized water dump rinser.
CRITICAL: As there is also an exposed BOX layer, it is important to properly time this etch to avoid unnecessary isotropic etching of this secondary oxide layer.

E. Fabrication of the Polysilicon Sacrificial Layers

A two-layer patterned polysilicon sacrificial layer is fabricated following the trench etching for TOBE devices or following the wafer cleaning for linear arrays. This two-layer construction facilities the formation of the gap structure with

TABLE V
LPCVD THIN SILICON NITRIDE DEPOSITION RECIPE

Temperature (C)	835
Pressure (mTorr)	250
NH_3 Flow Rate (sccm)	20
Dichlorosilane Flow Rate (sccm)	100
Time (m)	55

TABLE VI
PECVD PROTECTION SILICON DIOXIDE RECIPE

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	24

the combined thickness of the two polysilicon layers, while only leaving the thinner layer in the sacrificial tab region. This smaller void is easier to seal using the silicon dioxide plug deposition that will be discussed later.

5) Piranha clean the wafers in a 3:1 solution of sulfuric acid and hydrogen peroxide for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
6) LPCVD of the bottom silicon nitride insulation layer; 250-nm silicon nitride deposition using the recipe shown in Table V with a Tystar furnace stack, or equivalent.
Troubleshooting: Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process and prevent contamination of the processing tube. Deposition should also include a blank silicon prime wafer to use for thickness measurements and calibration of the following etching steps.
7) PECVD of a silicon dioxide protection layer; 50-nm deposition using the recipe shown in Table VI with a Trion Technology PECVD, or equivalent.
8) Piranha clean the wafers in a 3:1 solution of sulfuric acid and hydrogen peroxide for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
9) LPCVD of the first large grain polysilicon sacrificial layer; 250-nm polysilicon deposition using the recipe shown in Table VII with a Tystar furnace stack, or equivalent.
Troubleshooting: Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process and prevent contamination of the processing tube. Deposition should also include the nitride coated silicon prime wafer for thickness measurements and calibration of the following etching steps.
10) Lithography mask 2, photoresist patterning of the first sacrificial layer with the recipe shown in Table VIII. Approximate photoresist thickness 1.2 μm.
Troubleshooting: The exposure time for this lithography step is much higher than that required for the expected photoresist thickness of $\sim$1.2 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate polysilicon patterning. This is further explained in Section VI.
11) RIE of the 250-nm polysilicon sacrificial layer. Etching using the recipe shown in Table IX with a Trion Technology RIE, or equivalent.
CAUTION: Careful calibration of the etching time is required to prevent overetching into the silicon nitride insulation layer. Moderate etch selectivity ($\sim$5:1) to silicon dioxide is available with the proper selection of gases for the RIE process, so the deposited layer of silicon dioxide is used as an overetching stop to prevent damage to the insulation nitride layer.
12) Remove the photoresist by sonicating the wafer for 5 min in an acetone bath, before rinsing with isopropanol.
13) Piranha clean the wafers in a 3:1 solution of sulfuric acid and hydrogen peroxide for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
14) LPCVD of the second large grain polysilicon sacrificial layer; 100-nm polysilicon deposition using the recipe shown in Table X with a Tystar furnace stack, or equivalent.
Troubleshooting: Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process and prevent contamination of the processing tube. Deposition should also include the nitride and polysilicon coated silicon prime wafer for thickness

TABLE VII
LPCVD THICK POLYSILICON DEPOSITION RECIPE

Temperature (C)	600
Pressure (mTorr)	300
SiH_4 Flow Rate (sccm)	75
Time (m)	12.5

TABLE VIII
OVEREXPOSED HPR-504 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

TABLE IX
RIE SILICON RECIPE

Pressure (mTorr)	50
SF_6 Flow Rate (sccm)	25
RF Power (W)	30
Time (s)	200

TABLE X
LPCVD THIN POLYSILICON DEPOSITION RECIPE

Temperature (C)	600
Pressure (mTorr)	300
SiH_4 Flow Rate (sccm)	75
Time (m)	5

TABLE XI
OVEREXPOSED HPR-504 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

TABLE XII
RIE SILICON RECIPE

Pressure (mTorr)	50
SF_6 Flow Rate (sccm)	25
RF Power (W)	30
Time (s)	300

measurements and calibration of the following etching steps.

15) Lithography mask 3, photoresist patterning of the second polysilicon sacrificial layer with the recipe shown in Table XI. Approximate photoresist thickness 1.2 μm.
Troubleshooting: The exposure time for this lithography step is much higher than that required for the expected photoresist thickness of ~1.2 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate polysilicon patterning. This is further explained in Section VI.
16) RIE of the 350-nm polysilicon sacrificial layer. Etching using the recipe shown in Table XII with a Trion Technology RIE, or equivalent.
CAUTION: Careful calibration of the etching time is required to prevent overetching into the silicon nitride insulation layer. Moderate etch selectivity (~5:1) to silicon dioxide is available with the proper selection of gases for the RIE process, so the deposited layer of silicon dioxide is used as an overetching stop to prevent damage to the insulation nitride layer.
17) Remove the photoresist by sonicating the wafer for 5 min in an acetone bath, before rinsing with isopropanol.
18) PECVD of a silicon dioxide protection layer; 50-nm deposition using the recipe shown in Table XIII with a Trion Technology PECVD, or equivalent.
19) Piranha clean the wafers in a 3:1 solution of sulfuric acid and hydrogen peroxide for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
20) LPCVD of the top silicon nitride membrane layer; 1.0-μm silicon nitride deposition using the recipe shown in Table XIV with a Tystar furnace stack, or equivalent.
Troubleshooting: Proper cleaning prior to this deposition will help prevent defects caused by organic contaminant burning off at the high temperatures of this process and prevent contamination of the processing tube. Deposition should also include a blank silicon prime wafer to use for thickness measurements and the polysilicon and silicon nitride coated prime wafer for calibration of the following etching step.

TABLE XIII
PECVD PROTECTION SILICON DIOXIDE RECIPE

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	24

TABLE XIV
LPCVD THICK SILICON NITRIDE DEPOSITION RECIPE

Temperature (C)	835
Pressure (mTorr)	250
NH_3 Flow Rate (sccm)	20
Dichlorosilane Flow Rate (sccm)	100
Time (m)	220

TABLE XV
OVEREXPOSED HPR-506 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	6.5
Development Time (s)	35

TABLE XVI
RIE SILICON NITRIDE RECIPE

Pressure (mTorr)	150
CH_4 Flow Rate (sccm)	45
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	660

F. Etching of the Sacrificial Layer

After deposition of the silicon nitride membrane layer, the following processing steps are used to etch small holes through the membrane to access the sacrificial layer and to allow for wet chemical etching of the polysilicon.

21) Lithography mask 4, photoresist patterning of the sacrificial release holes with the recipe shown in Table XV. Approximate photoresist thickness 2.5–3.0 μm.
Troubleshooting: The exposure time for this lithography step is much higher than that required for the expected photoresist thickness of ~2.75 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate sacrificial hole etching. A consequence of this additional exposure time could be a small enlargement of these holes. This is further explained in Section VI.
22) RIE of the 1.0-μm silicon nitride membrane layer. Etching using the recipe shown in Table XVI with a Trion Technology RIE, or equivalent.
CAUTION: Careful calibration of the etching time is required to prevent overetching through the sacrificial polysilicon layers. There is a low etch selectivity (<2:1) between silicon nitride, silicon dioxide, silicon, and photoresist for this recipe, so it is important to deposit a thicker photoresist layer to prevent any excess etching of unwanted areas of the membrane. This etching step also

needs to etch entirely though the silicon nitride membrane but stop somewhere in the polysilicon sacrificial layers to ensure proper sacrificial etching in the KOH solution.

23) Remove the photoresist by sonicating the wafer for 5 min in an acetone bath, before rinsing with isopropanol.
24) Etch the exposed poly-silicon layers in a heated KOH chemical bath. Prepare a solution of 32% KOH by mixing stock KOH with deionized water. Heat the solution to 90 °C and stir using a magnetic stirring rod. Etch the wafers for 30 min in the heated solution to ensure complete etching of the sacrificial layer. Rinse the wafers in three large containers of deionized water to dilute any remaining KOH.
Troubleshooting: Actual etching times should be calibrated on a test wafer as the size and spacing of the sacrificial etching holes and dimensions of the membranes will determine the amount of time required to fully etch the polysilicon. Test membranes should still be processed with critical point drying, as it is difficult to visually determine the etching progress with fluid remaining the membranes. Overetching should not otherwise damage the wafer as KOH does not etch silicon nitride, but any stray pinholes or other damage to the silicon nitride layers could lead to etching of the silicon substrate.
CRITICAL: It is important to not wash these wafers in a dump rinser, as it is possible that the jets of water may damage the released membranes before they are properly sealed. These devices should also be quickly transferred from the final container of water into a container of high-purity isopropanol to prevent any unwanted drying and stiction effects.
25) Transfer the wafers into a container of high-purity isopropanol.
Note: Isopropanol was chosen as it was compatible with the critical point drying equipment used in the following step. This solvent can be substituted depending on the equipment available.
26) Critical point drying of the membranes using a Tousimis AutoSamdri 815B, or equivalent. Fill the chamber with high-purity isopropanol before transferring the wafers quickly.
Troubleshooting: Inspection of the membranes after critical point drying can be used to calibrate the amount of time required for sacrificial etching as well as the quality of the drying process. If the wafers are allowed to dry anytime between the sacrificial etching and critical point drying, then some membranes may be visibly snapped down from stiction forces, thus affecting the yield of the devices.
27) PECVD of silicon dioxide to seal the sacrificial release holes; 1.6-μm deposition using the recipe shown in Table XVII with a Trion Technology PECVD, or equivalent.
28) Prime the oxidized wafer for lithography by coating them in HMDS to promote better adhesion between the photoresist and the silicon dioxide film. This can be achieved using a Yield Engineering Systems vapor prime tool, or equivalent, with a standardized recipe shown in Table XVIII.
29) Lithography mask 5, photoresist patterning of the sacrificial release hole plugs with the recipe shown in Table XIX. Approximate photoresist thickness 2.5–3.0 μm.
Troubleshooting: The exposure time for this lithography step is much higher than that required for the expected photoresist thickness of $\sim$*2.75* μ*m. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate sacrificial plug etching. A consequence of this additional exposure time could be slightly undersized plugs. This is further explained in Section VI.*
30) RIE of the silicon dioxide plug layer; 1.2-μm etching process using the recipe shown in Table XX with a Trion Technology RIE, or equivalent.
CAUTION: This etching step is designed to etch approximately 80% of the plug oxide layer while maintaining an anisotropic etching profile. This etching recipe has a low selectivity (<3:1) to both photoresist and silicon nitride, so a thick layer of photoresist is required to prevent any etching of the silicon dioxide in the plug regions.
31) Etch the remaining exposed silicon dioxide layer with a buffered oxide solution for 8.5–9.0 min. Following the oxide etch, rinse the wafers five times in a deionized water dump rinser.

TABLE XVII
PECVD SILICON DIOXIDE PLUG RECIPE

Temperature (C)	300
Pressure (mTorr)	800
Oxygen Flow Rate (sccm)	85
TEOS Flow Rate (sccm)	100
RF Power (W)	60
Time (s)	1000

TABLE XVIII
HMDS VAPOR PRIME DEPOSITION RECIPE

Deposition Pressure (Torr)	1
Deposition Temperature (C)	150
Deposition Time (min)	5

TABLE XIX
OVEREXPOSED HPR-506 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	6.5
Development Time (s)	35

TABLE XX
RIE SILICON DIOXIDE RECIPE

Pressure (mTorr)	40
CHF_3 Flow Rate (sccm)	40
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	1800

TABLE XXI
STANDARD HPR-506 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	2000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	5.0
Development Time (s)	35

TABLE XXII
RIE SILICON NITRIDE RECIPE

Pressure (mTorr)	150
CH_4 Flow Rate (sccm)	45
Oxygen Flow Rate (sccm)	5
RF Power (W)	125
Time (s)	1200

CAUTION: The combination of RIE and wet chemical etching of the plugs is designed to create plugs with a mostly anisotropic profile while preventing any etching of the silicon nitride membranes. This wet etch needs to be carefully timed to prevent any excess etching of the plugs while still removing all the silicon dioxide covering the membranes.

32) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.
CAUTION: After the membranes have been released, any further sonication of the devices may damage the membranes.
Troubleshooting: If any photoresist remains on the wafer after rinsing with acetone and isopropanol, then an additional cleaning step using an oxygen plasma or wet piranha etching process can be used to strip this material.

G. Patterning of the Top and Bottom Electrodes

The final processing step, after the fabrication and etching of the sacrificial layers to form the vacuum membrane structure, is the deposition and patterning of the metal electrodes.

33) Lithography mask 6, photoresist patterning of the bottom electrode openings with the recipe shown in Table XXI. Approximate photoresist thickness 2.5–3.0 μm.
34) RIE of the silicon nitride membrane, silicon dioxide protection layers, and silicon nitride insulation layer; 1.7-μm etching process using the recipe shown in Table XXII with a Trion Technology RIE, or equivalent.
CAUTION: This etching step is designed to etch through all the deposited layers and into the silicon substrate. This is possible due to the low etch selectivity between silicon nitride, silicon dioxide, and silicon; however, it also etches with low selectivity toward photoresist. Therefore, a thicker layer of photoresist is required to protect the membrane from overetching.
35) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol.
CAUTION: After the membranes have been released, any further sonication of the devices may damage the membranes.
36) Piranha clean the wafers in a 3:1 solution of sulfuric acid and hydrogen peroxide for 15 min. Following the piranha etch, rinse the wafers five times in a deionized water dump rinser.
Troubleshooting: Proper cleaning of the wafer and removal of any remaining organic contaminants and particles is critical to reducing defects during aluminum sputtering. Any organic compounds could also off gas and contaminate the sputtering chamber, thereby affecting future processes.

TABLE XXIII
ALUMINUM SPUTTERING RECIPE

Pressure (mTorr)	7.0
Argon Flow Rate (sccm)	10.5
RF Power (W)	300
Time (min)	44.5

TABLE XXIV
OVEREXPOSED HPR-504 PATTERNING RECIPE

Spread Speed (rpm)	500
Spin Speed (rpm)	4000
Exposure Intensity (mJ/cm^2)	60
Exposure Time (s)	4.5
Development Time (s)	25

37) Sputtering deposition of the aluminum electrodes. Sputter 400-nm aluminum using the recipe shown in Table XXIII with a Kurt J. Lesker Company magnetron sputtering system, or equivalent.
Troubleshooting: Due to the required metal contiguity across the trench features, it is not advisable to deposit aluminum using an evaporation system. Likewise, with the added difficulty of properly exposing lithography features in the trenches, it would be difficult to use a liftoff approach for patterning the metal layer. Actual sputtering time should be calibrated to the available equipment as the deposition rate varies from system to system.
38) Lithography mask 7, photoresist patterning of the aluminum electrode layer with the overexposed recipe shown in Table XXIV. Approximate photoresist thickness 1.2 μm.
Troubleshooting: The exposure time for this lithography step is much higher than that required for the expected photoresist thickness of ~1.2 μm. Extra time is added to ensure that the thicker photoresist that builds up in the trenches is properly exposed to allow for accurate metal patterning. A side effect of this extra exposure is a shrinking of the top metal features, though this should only minimally affect the shape of these large pads.
39) Wet aluminum etching in a solution of AD aluminum etch: Semiconductor Grade (Fugifilm Puretch #881772) for 14.5–15.0 min. Following the aluminum etch, rinse the wafers five times in a deionized water dump rinser.
Troubleshooting: Aluminum etching process can be observed visually, and the exact time depends on the etching solution, concentration, age, and other factors. To ensure complete aluminum etching in the trenches, the total etching time should be 10%–20% longer then the time required to visibly remove the aluminum in the chemical bath.

40) Remove the photoresist by rinsing the wafer with acetone several times, before rinsing with isopropanol. **CAUTION**: After the membranes have been released, any further sonication of the devices may damage the membranes.

VI. Troubleshooting the Fabrication Process and Discussion of Device Yield

A. Adjusting Exposure Timing for Trench Features

For this process flow, two different positive photoresists were used to pattern the various features: HPR-504 and HPR-506. These positive resists require a proper dosage of UV radiation to allow for complete development in the diluted Microposit 351 developer solution. While this can be easily calculated for uniform thin films of photoresist, it is more difficult to estimate the photoresist thickness in trenches with depths larger than the photoresist thickness. As a result of these areas of thicker photoresist, a longer exposure time is required to pattern features inside these trenches. An attempt at patterning a metal layer in the DRIE trenches with the standard exposure time is shown in Fig. 5(a), where there are aluminum remnants remaining in the corners of the trenches, which can result in short circuiting between electrode rows. The results of increasing exposure time and switching to the KOH etched trenches, when patterning the photoresist, are shown in Fig. 5(b), with proper patterning of the metal traces.

The results of improper lithography exposure times are easily apparent when patterning metal layers, but have equally been affecting all the lithography steps with patterning in the trenches. These effects are shown in Fig. 6 where the cross sections of the completed devices are examined using helium ion microscopy. In both devices, there are visible cavities etched under the trenches as a result of polysilicon layers still present in the trenches after failed lithography and etching. There are also thick layers of PECVD silicon dioxide leftover from the sacrificial plug etching due to the same process defects. There are some improvements shown in the KOH etched devices as the polysilicon sacrificial layers are etched much further into the trenches.

This problem can be addressed by increasing the UV exposure for the masking step to fully expose the trench regions, but this will result in overexposure of the features on the membrane. This has less of an impact on large features, such as the metal electrodes, but could change the shape of the smaller sacrificial etching holes. Depending on the depth of the trenches being used for the devices, it may be required to adjust the mask design to account for the enlargement or reduction of certain features. Due to these exposure inconsistencies, it is also recommended to avoid placing any noncritical features into these trenches on the mask designs. For the first generation of masks used in this process flow, there were additional sacrificial release tabs overlapping the trench regions. The resulting underexposure in the trench regions failed to pattern these tabs, often compromising membrane hermeticity and in some cases stressing and deforming the membrane, causing a change in resonant frequency. These effects are shown in Fig. 7.

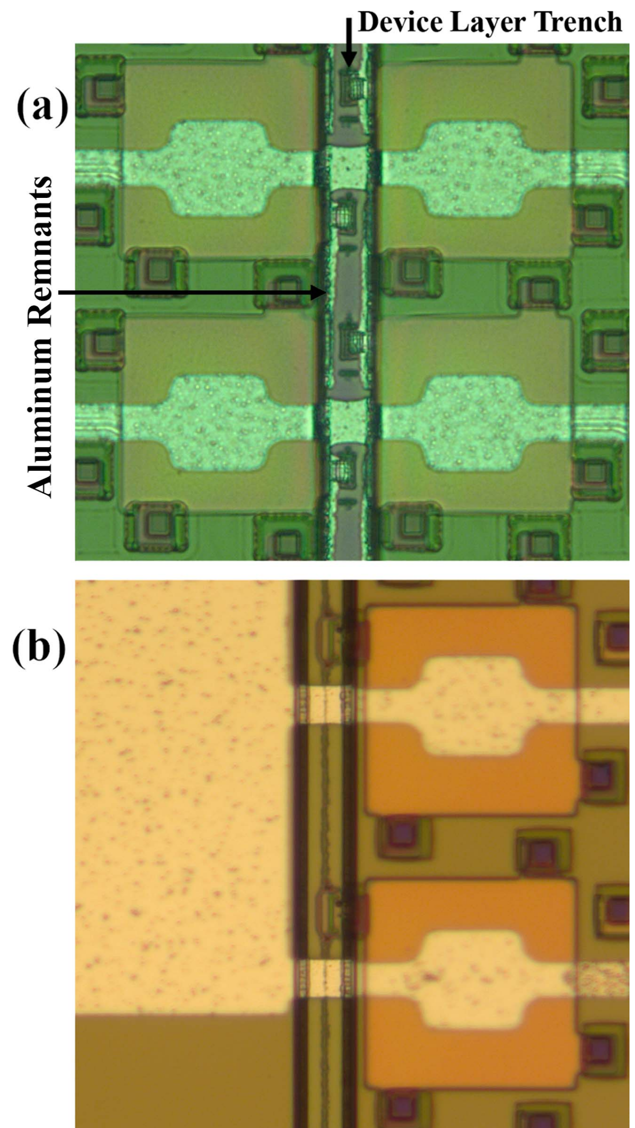

Fig. 5. Lithography errors from thicker films of photoresist in trench regions. (a) Excess aluminum remaining in the DRIE trench region following etching due to protection from partially exposed photoresist. (b) Proper lithography and aluminum etching in the KOH trench with the extra lithography exposure time to account for thicker photoresist films.

B. Etching Selectivity and Timed Etching Processes

Several of the steps in the outlined process flow require carefully timed etching processes to pattern specific layers without damaging other parts of the device. Wet chemical etching often has the highest etching selectivity, but also creates an isotopic etching profile, while RIE allows for more anisotropic etching, but often has a much lower etch selectivity. In order to ensure more accurate etching steps, process flows can utilize thin film etch-stops, but these are not suitable for every etching process. Two examples of these thin film etch-stops are used in the outlined process flow. In Step 4A-ii, the silicon device layer is patterned using a reactive ion Bosch etching process, with a buried silicon oxide layer acting as an etch-stop. With a selectivity of over 100:1 when etching silicon: silicon dioxide, the process can be safely overetched by 10%–20%, to ensure complete separation of the bottom electrodes without etching

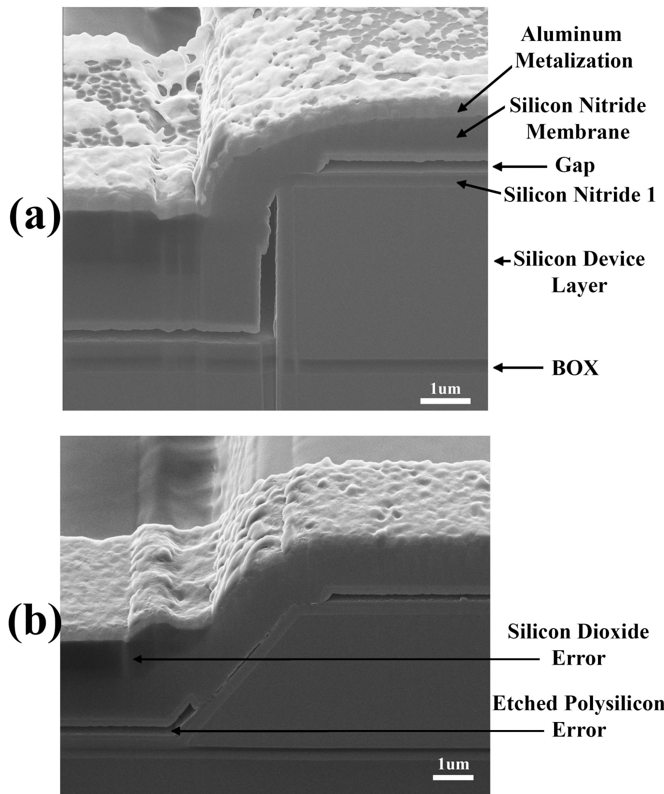

Fig. 6. Cross-sectional helium ion microscopy images of both the (a) DRIE etched and (b) KOH etched trench areas. Labeled layers are common to both structures. Films of silicon dioxide and unwanted cavities are observed in both structures as a result of failed etching of the sacrificial plugs and polysilicon sacrificial layers in these areas.

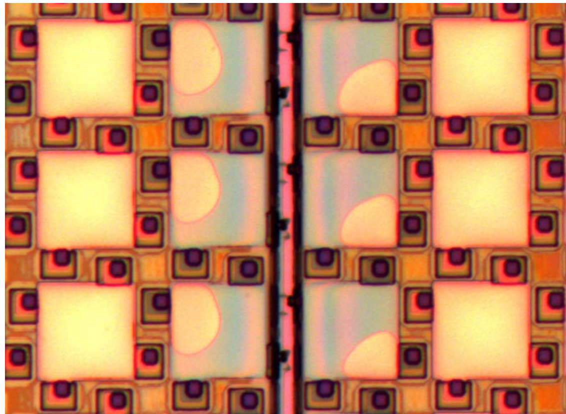

Fig. 7. Fluid leakage into the membranes along the trench region as a result of underexposed photoresist in the trenches causing errors during most etching processes. Membranes in the center of elements are unaffected and were properly fabricated.

significantly into the BOX. A similar etch-stop is used in Steps 13 and 20, where the 50-nm protection oxide is used as an etch-stop when patterning the polysilicon sacrificial layers. This protection layer allows for overetching of the polysilicon layers to account for thickness nonuniformities across different areas of the wafer without concerns of etching into the silicon nitride isolation film.

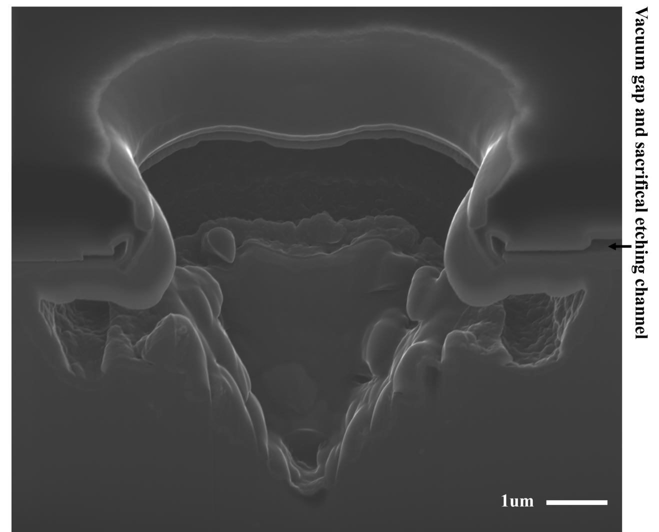

Fig. 8. Helium ion microscope cross-sectional image of the results of overetching during the silicon nitride sacrificial plug RIE. Etch proceeded through the insulation silicon nitride film and into the silicon substrate. Exposed silicon substrate was then etched with KOH during the sacrificial release process. Resulting cavity was then partially filled with silicon dioxide from the PECVD plug deposition.

While these processes have excellent selectivity for etching silicon films, it is more challenging to etch silicon nitride films with high selectivity. The silicon nitride RIE recipe used in Steps 28 and 42 has a low selectivity and etches silicon, silicon dioxide, and photoresist at nearly the same rate as the target silicon nitride. Therefore, it is very important to calibrate the etch rate for the system and to time the etch rate accordingly. These deeper etches also require thicker layers of photoresist to prevent the etch process from etching through the masking layer and into undesired areas of the silicon nitride membrane. One example of an overetched Step 28 sacrificial plug etching process is shown in Fig. 8. In this case, the processing time was too long and ended up etching though the bottom silicon nitride insulation layer into the silicon device layer. The following KOH sacrificial etch process then proceeded to etch the characteristic diagonal walls into the silicon device layer. This mistimed etching process created a large cavity in the sacrificial plug holes and compromised the deposited silicon dioxide sealing of these sacrificial openings.

For the process outlined above, there is a small buffer for the silicon nitride etching in Step 28, as it is acceptable to stop this etching process anywhere in the polysilicon sacrificial layer or protection oxide layers, with a combined thickness of 200 nm. Ideally, the target etching depth should be halfway into the polysilicon sacrificial layer as this would provide a sufficient etching depth for a range of silicon nitride thicknesses caused by a nonuniform LPCVD of the thick membrane film across the wafer. One testing method for determining the etching depth, and therefore rate, is with the use of a laser confocal microscope. One measurement taken of this etching step is shown in Fig. 9. Combining the height data gathered with the laser confocal microscope with the average thickness of the silicon nitride membrane (measured with an ellipsometer on a silicon prime test wafer included in the LPCVD process)

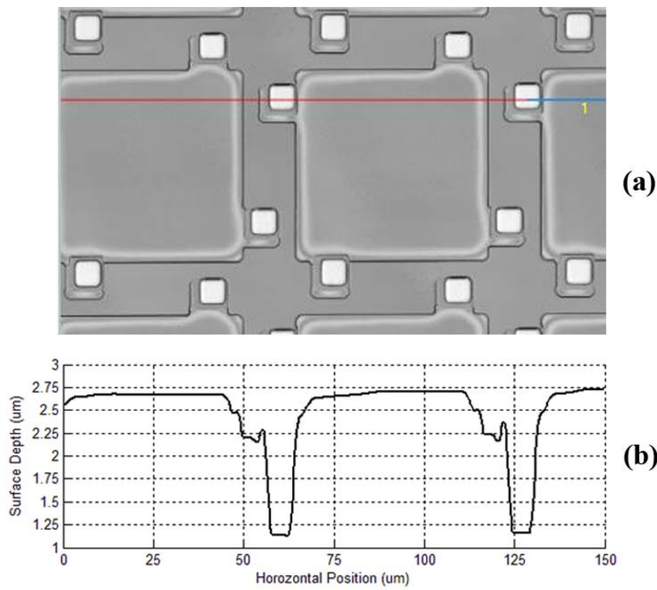

Fig. 9. Laser confocal microscope measurements following sacrificial hole etching process. (a) Microscope measurement with different grayscale shades representing depth information. (b) Cross-section depth slice through the sacrificial holes to measure the etching progress and calibrate etch rate.

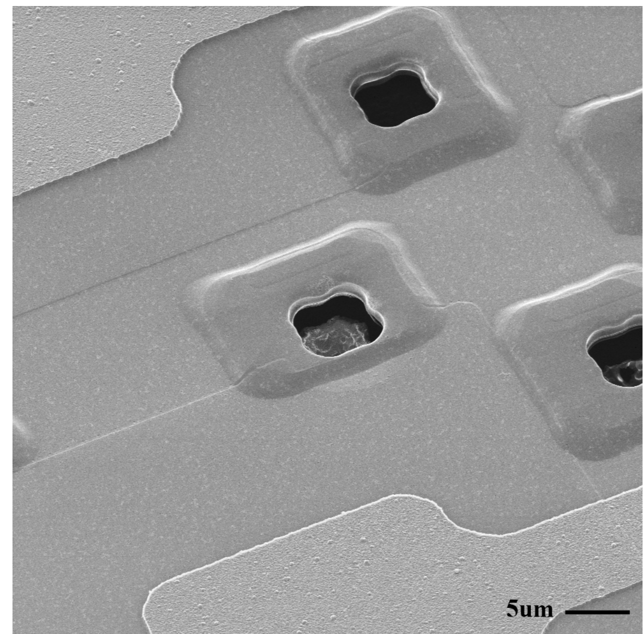

Fig. 10. Helium ion microscope image of the patterned silicon dioxide sealing plugs. Edges of the plugs have a curved shape as a result of the combined RIE and wet chemical etching process.

will give a good estimate of the etching process and indicate if more etching is required for a successful sacrificial etching process.

While many etching processes are used independently, it is occasionally beneficial to combine plasma and wet chemical etching processes. An example of this combined etching is used in Steps 37 and 38. A thick silicon dioxide layer was deposited and patterned into plugs for sealing the sacrificial release holes. The desired plug shape would have anisotropic sidewalls; however, the RIE process required could overetch and damage the silicon nitride membranes. Therefore, the majority of the etching was implemented with an anisotropic RIE process before finishing with a timed buffered oxide etch to ensure high selectivity to the silicon nitride while maintaining a mostly anisotropic plug shape. The results of this combined etching process are shown in Fig. 10.

VII. Device Characterization and Testing

During the device fabrication, it is difficult to assess the devices beyond visual inspection with microscopes, thickness measurements with optical equipment (such as ellipsometer and laser confocal microscopes), or physical step height measurements using a stylus or atomic force microscope. While these are excellent techniques for evaluating the thickness of deposited layers, the depth of various etching steps, or the alignment between mask steps, none of these measurements are able to assess the operation of these transducers.

To fully characterize these ultrasound sensors, measurements of the membrane velocity or displacement as a function of time will analyze the frequency response of the device. These can be measured using a PolyTec MSA-500 microsystem analyzer laser Doppler vibrometer, or equivalent. A measurement of the frequency response membrane displacement is shown in Fig. 11 for these 52-μm sacrificial release devices. Resonance frequencies in air were measured as ~6.3 MHz, close to the predicted values of ~7.0 MHz. The differences between these results can be explained by thickness and tensile stress variations in the membrane, or small differences between the standard values of density and Young's modulus compared with those deposited with our LPCVD system. The collapse voltage for these devices is measured in the range of 100–120 V, similar to the predicted snap down voltage of ~115 V found from our models.

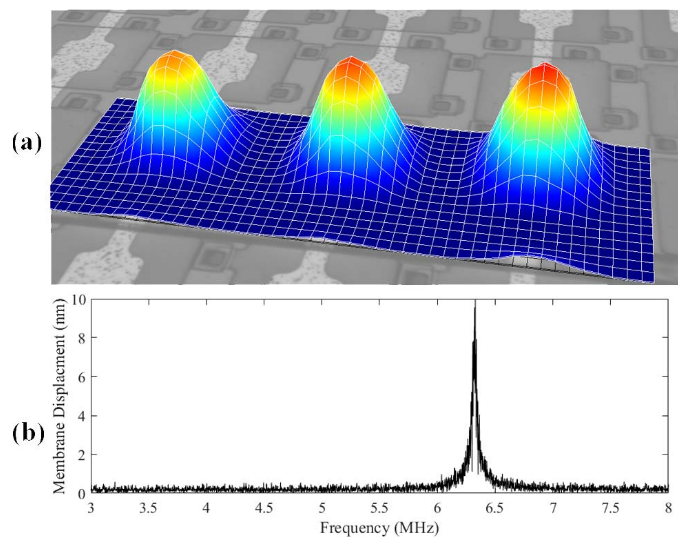

Fig. 11. Sample laser Doppler vibrometry measurements. (a) 2-D scan showing static membrane displacement for a given frequency. (b) Single-point measurement using an 8-V pseudorandom ac signal with a 40-V dc bias. Peak indicates the optimum resonant frequency of the device for the given bias conditions.

Vibrometry measurements are an excellent source of information for individual or small groups of membranes, but to fully characterize an entire sensor, the diced device needs to be packaged and integrated into a scanning system. In most cases, this would require wirebonding the individual row and column elements into a larger package or directly onto a printed circuit board. Based on the approach being used, the packaging process can also add additional design considerations into the fabrication process. It may dictate minimum contact pad sizes or require alternative metals for proper bonding.

Other electrical characterization can also be used to characterize these devices. Vector network analyzers and CMOS testing equipment can be used to measure the capacitance response of the system to various current and frequency inputs. While these measurements can be invaluable for assessing the operation of these devices, most of these electrical and vibrometry measurements are only measuring individual or small clusters of membranes. Final testing should be performed by interfacing complete devices with an ultrasound system and evaluating their performance in an immersion system. These types of measurements could include hydrophone testing, where local pressure profiles can be measured for individual elements, or phantom imaging where these devices are used to image various scattering phantoms to determine imaging quality and signal-to-noise ratio and to identify any grating lobes or other imaging artifacts.

VIII. Lessons Learned About Device Yield

While this paper outlines a number of fabrication details, practices, and pitfalls, there are issues addressed that are specific to the fabrication of TOBE arrays. One problem shown is that the addition of bottom electrode trench etching creates challenges for subsequent lithography steps. Figs. 6 and 7 illustrate the consequences of unwanted polysilicon remaining in the trenches following an incomplete exposure in these regions, leading to compromised membrane hermeticity and changes in the resonant frequency of these devices. Fig. 5 illustrates similar effects leaving residual metal in the trenches, potentially short circuiting different rows of membranes. We found that using KOH etching to pattern these trenches, along with additional lithography exposure, helps to mitigate these problems at the cost of electrode separation.

The fabrication yield of these ultrasound membranes is impacted by a number of different factors throughout the process flow outlined above. The most critical factors affecting device yield are some of the timed etching processes mentioned earlier. Without successful silicon nitride etching into the sacrificial layer, the membranes will not be released and will not function. Likewise, if the sacrificial silicon etching is not fully completed, then there will be silicon pillars in the center of each membrane, which will cause large changes in the resonance frequency of the devices. Another important silicon nitride etch is the electrode etch for exposing the bottom silicon electrode prior to aluminum electrode metallization. If this etch is not completed, then there will be no electrical connection between the aluminum contact pad and the silicon electrode and the devices will not function. While these etching errors can cause complete device failure, several measurement and inspection steps can be included during the process flow, such as laser confocal microscope measurements, to measure each etching step and determine if more time is required.

Other issues that were outlined in the process flow include omission of the cleaning steps, incomplete removal of the photoresist following etching steps, or defects in the photoresist. These issues contribute to localized membrane defects and lower total device yield. Many of the cleaning steps are included to remove any trace organic or particulate contamination on the devices, which would cause defects during lithography or high-temperature film depositions. These factors should not disable the entire device, but can impact imaging performance if some imaging elements have a different number of active membranes.

IX. Conclusion

In this paper, we present a complete fabrication procedure for both linear and TOBE CMUT arrays using a sacrificial release process. This process demonstrates two separate methods for patterning the bottom electrode for a TOBE device. Using DRIE to pattern the substrate silicon has the advantage of better etching control with the buried silicon dioxide layer as an etching stop. We propose that replacing this step with a KOH chemical etch of the silicon device layer may increase device yield though more reliable patterning of the various layers in these trench areas, but adds additional processing steps and requires careful optimization of an extra silicon dioxide masking step.

Successful fabrication of CMUTs requires careful process control, and we present several troubleshooting points for calibrating etch rates and properly timing the various etching steps. With proper simulation, mask design, and an optimized process flow, there is the potential for robust and high yield CMUT fabrication using this sacrificial release process. While the recipes presented may require modification for other tools sets, the presented approach should offer valuable starting parameters for further process optimization. These arrays are excellent candidates for medical imaging applications and, with development of larger arrays, could allow for whole organ high-resolution 3-D imaging.

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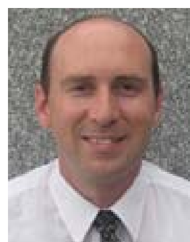

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