High-Performance Electrode-Post CMUTs: Fabrication Details and Best Practices

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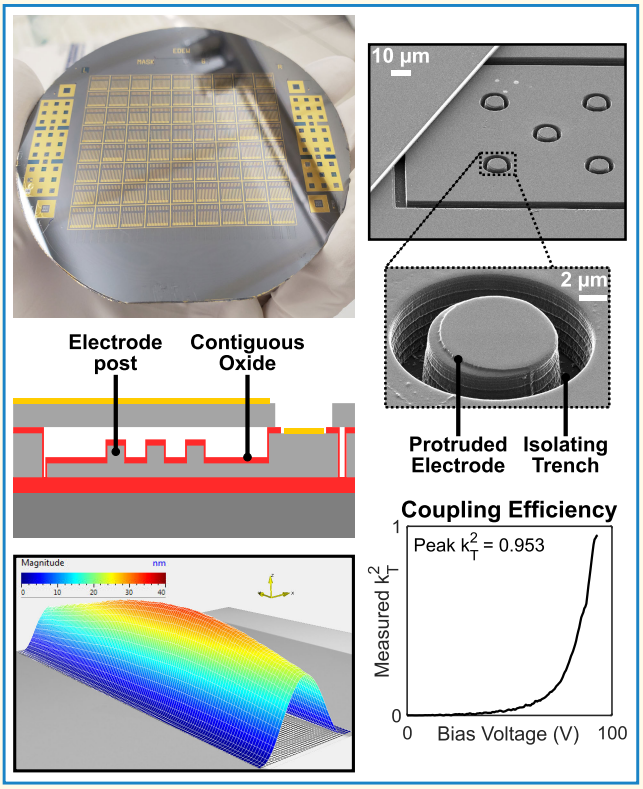
***Abstract*—Capacitive micromachined ultrasound transducers (CMUTs) have been investigated for over 25 years due to their promise for mass manufacturing and electronic co-integration. Previously, CMUTs were fabricated with many small membranes comprising a single transducer element. This, however, resulted in suboptimal electromechanical efficiency and transmit performance, such that resulting devices were not necessarily competitive with piezoelectric transducers. Moreover, many previous CMUT devices were subject to dielectric charging and operational hysteresis that limited long-term reliability. Recently, we demonstrated a CMUT architecture using a single long rectangular membrane per transducer element and novel electrode-post (EP) structures. This architecture not only offers long-term reliability, but also provides performance advantages over previously published CMUT and piezoelectric arrays. The purpose of this article is to highlight these performance advantages and provide details of the fabrication process, including the best practices to avoid common pitfalls. The objective is to provide sufficient detail to inspire a new generation of microfabricated transducers, which could lead to performance gains of future ultrasound systems.**

***Index Terms*—Capacitive micromachined ultrasound transducer (CMUT), dielectric charging, electrode posts (EPs), microelectromechanical systems (MEMS), microfabrication, process flow, rectangular membranes, reliability, silicon fusion bonding, transducer characterization, wafer bonding, yield factors.**



I. Introduction

PIEZOELECTRIC materials have served as a gold-standard transducer technology for decades. Since the development of capacitive micromachined ultrasound transducers (CMUTs), the ultrasonics community has anticipated that CMUTs may provide competitive advantages over piezoelectric technology. However, despite some commercial successes, micromachined transducers have not provided the expected performance and reliability to justify switching away from piezoelectric materials. The recent Restrictions of Hazardous Substances legislation in the European Union has provided impetus for development of lead-free alternatives to common lead-based piezoceramics and single-crystal devices. While some lead-free materials are under investigation, they have not yet found their role in mainstream ultrasound systems. Micromachined transducers have been commercialized in some niche applications, but are not yet widespread.

Some challenges associated with such micromachined transducers have included the following. First, dielectric charging, impacting long-term reliability [1]. Second, operational hysteresis, meaning that a membrane collapse voltage is different than the snap-back voltage, resulting in unpredictable behavior when operating near the collapse point [2]. Third, when multiple small membranes comprise a single transducer element, some membranes collapse unintentionally, since such membranes have a range of collapse voltages. Membranes in such a collapsed state behave differently than uncollapsed

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Highlights

- **Electrode-post CMUTs are a recently introduced architecture that may offer improved reliability and sensitivity.**
- **Electrode post CMUTs with one long rectangular membrane per element were shown to outperform previous transducers while further providing robustness against charging and minimizing hysteresis.**
- **Previously CMUTs exhibited poor transmit performance. Our EP-CMUTs outperform piezoelectric transducers and thus could have significant impact. Extensive details of fabrication are provided.**

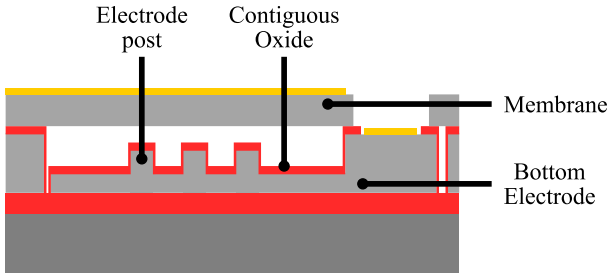


Fig. 1. Cross-sectional view of an EP CMUT. The EPs consist of elevated portions of the bottom electrode, surrounded by an insulating layer. These EPs serve to reduce the effective gap between electrodes in the post regions, increasing electrostatic attraction. The height of the EPs is also calibrated to prevent membrane collapse, thus mitigating hysteresis.

membranes and are more susceptible to charging. Fourth, when biasing a membrane below the collapse voltage to avoid such problems, the electromechanical efficiency is low. The range of collapse voltages of an ensemble of membranes can, thus, lead to degraded performance compared with a single membrane [3]. Fifth, multiple membranes do not always work in synchrony. Mutual acoustic coupling between membranes within an element can lead to parasitic and counterproductive motion, reducing overall device performance [4], [5]. Sixth, unintended dielectric breakdown of even a single membrane within an element can lead to the whole element being inoperative [6]. Seventh, low active real estate in multiple membrane CMUTs results in suboptimal performance.

Even with some progress toward mitigating these problems, CMUTs have not yet provided performance advantages compared with piezoelectric transducers. To both mitigate above problems and to achieve needed performance gains, we recently introduced electrode-post (EP) CMUTs with long rectangular membranes [7]. Rather than fabricate many small membranes per transducer element, we use a single long rectangular membrane, where the membrane width principally determines the resonance frequency. This appears to mitigate electromechanical efficiency problems and asynchronous motion problems described above. Furthermore, so-called isolation posts, dielectric posts with minimal bottom electrode area were previously introduced in the literature to mitigate dielectric charging problems, since any dielectric charging would occur in a small real estate [8]. However, in our experience, lack of dielectric coverage on bottom electrodes due to isolation post patterning substantially increases the risk of breakdown, especially if any defects occur in the fabrication process [6]. Our so-called EP architecture avoids such breakdown issues, while both offering robustness against charging and hysteresis, and while simultaneously providing performance gains. In brief, our EPs include bottom electrode protrusions capped by dielectric insulation as illustrated in Fig. 1. The height of these posts is engineered so as to capture the membrane at the collapse point. The upward protrusions of electrode material in these posts are designed to achieve greater local electrostatic force, which we showed could have a significant impact on overall device performance, despite the low fractional real estate associated with these EPs [7].

This recent paper demonstrated improved transmit efficiency and electromechanical efficiency compared with recent work using piezoelectric transducers. These promising data could motivate additional work in the field on the path to high-performance and reliable CMUT arrays. However, the development of these devices took many years and involved much failure associated with the design and fabrication. It is the purpose of this article to outline some of the pitfalls, and best practices we discovered to achieve outstanding devices. We provide a detailed process flow and summarize some lessons learned that we hope will be advantageous to the community.

II. Background

CMUTs have a long-standing history spanning more than 25 years [9]. Although CMUT fabrication was initially restricted to sacrificial release techniques [10], [11], recently wafer-bonding approaches have gained popularity due to increased control over important dimensions and the capacity to fabricate large membranes [12]. Wafer bonding can also be realized by multiple bonding techniques [13], [14], which enables a broader material selection [15], including transparent and flexible materials [16], [17]. Our EP CMUTs are fabricated using a wafer-bonding approach with some key differences from other fusion bonding processes. Many silicon wafer-bonding approaches have relied on thermal oxidation to create dielectric standoff or support structures. However, as observed by Christiansen et al. [18], this can lead to oxidation cusps that reduce the bonding yield significantly. This primarily occurs when a two-step oxidation is performed, a second oxidation done after patterning a first oxide layer. Our approach is to use a single oxidation and rely on patterning of the silicon bottom electrode substrate rather than patterning of oxide layers.

Many solutions to dielectric charging have been suggested, including optimization of film surface roughness [19] and quality [20], investigation of different dielectrics [15], [21], and architectural adjustments, such as isolation posts [8], [22], [23]. However, optimization of films alone does not fully eliminate charging. The drawback to isolation post approaches is the patterned dielectric results in bare bottom electrode surface area. In a recent thesis from our group, Greenlay [6] illustrates that this can lead to dielectric breakdown. Moreover,

Huang et al. [8] observed considerably reduced transmit and receive sensitivity in their isolation post devices compared with equivalent contiguous-dielectric (CD) CMUTs. Several groups have extended the isolation post concept to include patterned electrodes around isolation posts to reduce the transdielectric electric field in the post regions [6]. These devices include an anodic bonding approach for dual-frequency CMUTs [14], isolated isolation posts (IIPs) [6], [7], and a sacrificial release approach with posts attached to hexagonal membranes [24]. Patterning electrodes to minimize the electric field through the dielectric posts is a sound strategy to further improve charging robustness; however, this comes at the cost of active electrode real estate and, thus, reduced performance compared with other CMUT architectures [7]. Notably, we recently demonstrated that the EP CMUTs can exhibit comparable charging robustness to CMUTs with IIPs, while exhibiting substantially improved performance [7].

Some groups have sought to improve CMUT performance by achieving piston-like membrane motion. These works demonstrate promising performance gains, but require complicated fabrication processes that may be difficult to fabricate with high yield [23], [25], [26], [27], [28]. These approaches typically also use multiple membranes per element, leading to dangers of asynchronous operation withing an element. Our approach follows Zhang et al. [19], which used a long-rectangular membrane per element. While our devices do not achieve plane piston motion, they make better use of active real estate compared with most circular, square, or hexagonal membranes previously published [7].

In our recent paper, we not only investigated EP CMUTs, but also compared them with other architectures. A simple electrostatic model was used to compare against conventional isolation posts (IP), showing enhanced force and sensitivity with EPs in a parallel plate model. We also used these models to compare our EP design against traditional CMUTs with contiguous bottom electrode (CD CMUTs), and with so-called IIP devices. In IIP devices, a trench is patterned into the bottom electrode around each post structure, leaving the 'isolation post' electrically floating. Experimentally, we fabricated devices with EPs and compared with CD and IIP devices and found that EP devices exhibited enhanced performance, in particular, better electromechanical efficiency and improved receive sensitivity than the other architectures.

III. Design Considerations

The dimensions of our devices were chosen to be similar to our previous work [7], [19]. In this work, single-membrane rectangular CMUTs were fabricated with a 3.0-mm-long and 120-μm-wide membrane. The membrane was designed to be 5-μm thick, with a 500-nm vacuum cavity and 360 nm of oxide insulation. For the EP and IIP CMUTs that we fabricated, the posts were 320-nm tall, with the remaining 180 nm of space available for the membrane to deflect. A discussion of bond-pad design and the spacing of post structures is presented in our previous work, along with a parallel-plate electrostatic model to predict collapse voltage and other important properties [7]. Further analytical and computational modeling of single-membrane CMUTs would further assist in optimizing these devices, however, that is beyond the scope of this manuscript.

In terms of post design, there are a number of considerations, starting with the type of post used. In our previous work, we explored EPs and IIPs. IIPs are similar to EPs, but include a circular trench patterned around each post to isolate the elevated post from the bottom electrode. This serves to minimize the electric field magnitude through the post and further reduce opportunities for dielectric charging to occur. CMUTs with either EPs or IIPs have demonstrated significantly improved reliability over conventional designs without posts. However, EPs have also been shown to improve electromechanical efficiency and receive sensitivity. By contrast, IIPs reduce electromechanical efficiency, but completely eliminate hysteresis when calibrated appropriately [7]. In our devices, the EP structures had a diameter of 10 μm, while each EP CMUT had 176 EPs, comprising 4.2% of the total cavity area. As discussed in our previous work, increasing the area occupied by EPs increases the electrostatic attraction between the top and bottom electrodes [7]. However, more area of elevated electrode also corresponds to more dielectric exposed to large electric field magnitudes and, thus, potentially reduced robustness to charging. As each IIP represents a removed portion of the bottom electrode, it is desirable to minimize the area occupied by IIPs while maintaining enough posts to prevent membrane collapse.

Aside from device dimensions, the most important consideration is the starting material. Whether fabricating EP CMUTs, IIP CMUTs, or traditional CD CMUTs, our process requires two silicon-on-insulator (SOI) wafers. These wafers need not be identical—different SOI wafers may be selected for the "top" and "bottom" wafers to optimize the parameters for the membrane and bottom electrode, respectively. As fusion bonding is extremely sensitive to the surface roughness of each wafer, a quality polish on the device layer of each SOI wafer is critical. We exclusively used double-side-polished (DSP) SOI wafers, as a nonuniform surface of the handle wafer may lead to uneven distribution of force from the bonding tool.

The device layer of the bottom SOI wafer determines the properties of the bottom electrode; thus, the doping and thickness of the device layer are the most important properties. In general, high doping is desirable, as some authors have observed unusual behavior in wafer-bonded CMUTs due to semiconductor effects from electrodes with low doping [6]. This issue was resolved by increasing the doping within the silicon electrodes. As demonstrated by Havreland et al. [29], the CMUT performance suffers when the resistance across the bottom electrode is too high. The bottom electrode resistance depends on its cross-sectional area (function of the width of the element and thickness of the device layer), length of the electrode, and the resistivity (doping) of the bottom device layer. Based on this calculation, it would appear that CMUT performance would be optimized with the maximum possible doping and maximum possible device thickness (thus minimizing the resistance of the bottom electrode). However, there are some important practical considerations. The first is that any features etched through the bottom electrode (such as IIPs or trenches to isolate parasitic capacitance) may be difficult to etch if the bottom electrode is too tall (due to limited

deep reactive ion etching (DRIE) aspect ratio and selectivity). However, a more important consideration is thermal oxide quality.

Several authors have suggested that the mechanism for dielectric charging involves trapping charge within existing traps as opposed to the creation of new ones [19], [30], [31]. For this reason, maintaining oxide quality is critical for device performance and reliability [19]. Even for EP and IIP architectures, which are robust to charging, this is an important consideration, as sufficiently poor oxide is susceptible to charging from weak precollapse electrode fields. Although post structures mitigate charging from collapse states, devices are still susceptible to precollapse charging if the oxide quality is sufficiently poor.

From our experience, we have achieved acceptable oxide quality with boron-doped silicon at the resistivities of 0.01–0.02 Ωcm; however, this level of doping requires a thick bottom electrode to achieve acceptable electrode resistance. With more highly boron-doped silicon (<0.005-Ωcm resistivity), it was challenging to achieve reasonable oxide quality. Ultimately, we had the most success with highly arsenic-doped device layers. The high doping levels (<0.005-Ωcm resistivity) allowed acceptable bottom electrode resistivity, while the arsenic doping appeared to have fewer deleterious effects on thermal oxide quality. We speculate that arsenic doping may yield higher quality thermal oxide than boron doping in scenarios where dry thermal oxide is grown on extremely highly doped silicon. This hypothesis is somewhat consistent with previous work, which has shown that during thermal oxidation of highly doped silicon, donors, such as arsenic, induce fewer interface charges than acceptors, such as boron [32]. Similarly, donor atoms have been demonstrated to diffuse less into the oxide layer at a $Si–SiO_2$ interface during thermal oxidation [33]. However, this idea requires further study to confirm.

Finally, for the top SOI wafer, the thickness of the device layer determines the thickness of the membrane. If supplies of SOI wafers are limited, a thicker device layer can be thinned using wet oxidation or chemical mechanical polishing (CMP) to achieve the desired dimension, however, this adds additional process steps. If this is done, extreme care must be used to ensure surfaces have near atomic-layer smoothness for successful wafer bonding. Alternatively, membrane thinning can be done with wet oxidation and removal or by RIE after handle removal from the double-SOI-bonded wafers, as surface roughness in this scenario is less critical. High doping of the top SOI wafer's device layer is also desirable, although less critical than the bottom electrode as a metal contact is also typically deposited on the top electrode. The type of dopant is also less important for the top electrode, since thermal oxide is not grown on this layer (in the case of membrane thinning, the grown oxide is removed).

IV. Fabrication Overview

Our fabrication process is summarized in Fig. 2. Processing begins on the bottom SOI wafer [Fig. 2(a)], which is patterned using RIE to define post structures (such as EPs or IIPs) from the rest of the cavity [Fig. 2(b)]. The depth of this etch determines the height of the posts, which was 320 nm for our devices. This step can be skipped if one only intends to fabricate traditional CD CMUTs. The second lithography step allows the entire cavity to be etched using silicon RIE, as illustrated in Fig. 2(c). This etch determines how much room is available for the membrane to deflect before contacting the posts in the cavity (180 nm for our devices).

Trenches are then defined around each element (to isolate parasitic capacitance) and around each post (in the case of IIP CMUTs) with the third lithography step. These trenches are etched using Bosch DRIE, as demonstrated in Fig. 2(d). Following DRIE and extensive cleaning, 360 nm of thermal oxide is grown on the bottom of wafer using dry oxidation [Fig. 2(e)]. The processed bottom wafer is then bonded to a second SOI wafer, known as the "top" or "lid" wafer. These wafers are bonded, such that the device layers face each other and annealed, as illustrated in Fig. 2(f).

In order to use the newly bonded device layer as a membrane, the handle and buried oxide (BOX) layer of the top wafer must be removed. However, bulk etching the entire top handle risks accidentally destroying the handle of the bottom wafer as well. For this reason, we protect the backside (bottom) SOI wafer's handle with plasma-enhanced chemical vapor deposition (PECVD) oxide prior to bulk etching, as depicted in Fig. 2(g). Bulk etching of the lid wafer's handle is then completed [Fig. 2(h)] using a combination of DRIE processes and wet etchants, such as tetramethylammonium hydroxide (TMAH). After the handle is completely removed, the BOX layer of the top wafer (and optionally the PECVD protection) can be removed using buffered oxide etching (BOE) solution [Fig. 2(i)].

Access holes through the newly bonded device layer are then patterned in mask step 4. These access holes are also patterned using DRIE, as displayed in Fig. 2(j). The fifth patterning step defines a smaller access hole within the thermal oxide below, which is etched using RIE to access the bottom electrode [Fig. 2(k)]. Finally, metal contacts are deposited using magnetron sputtering and patterned in the final lithography step. These contacts are patterned using wet etching processes, as shown in Fig. 2(l)].

V. Mask Design Considerations

In our process, there are several important factors to consider when designing masks. As wafer bonding is the most yield-critical step in this process, every step prior to bonding is designed to minimize deleterious impacts on bonding yield. This philosophy also extends to mask design. In particular, this means that bondable area should be maximized by etching as few areas of the wafer as possible during the first three lithograph steps. Masks for these steps should look similar to Fig. 3 (assuming positive-tone photoresists), where the only exposed portions of the wafer are the device areas, alignment marks, and a small number of features used for characterization.

A secondary (but also significant) reason to minimize unnecessary etching of nondevice areas of the wafer relates to photoresist coverage. Mask steps 3 and 4 involve using DRIE to etch through the device layer of a wafer. If this device layer is more than several micrometers thick (as is often desirable), the height variation between the etched and unetched portions

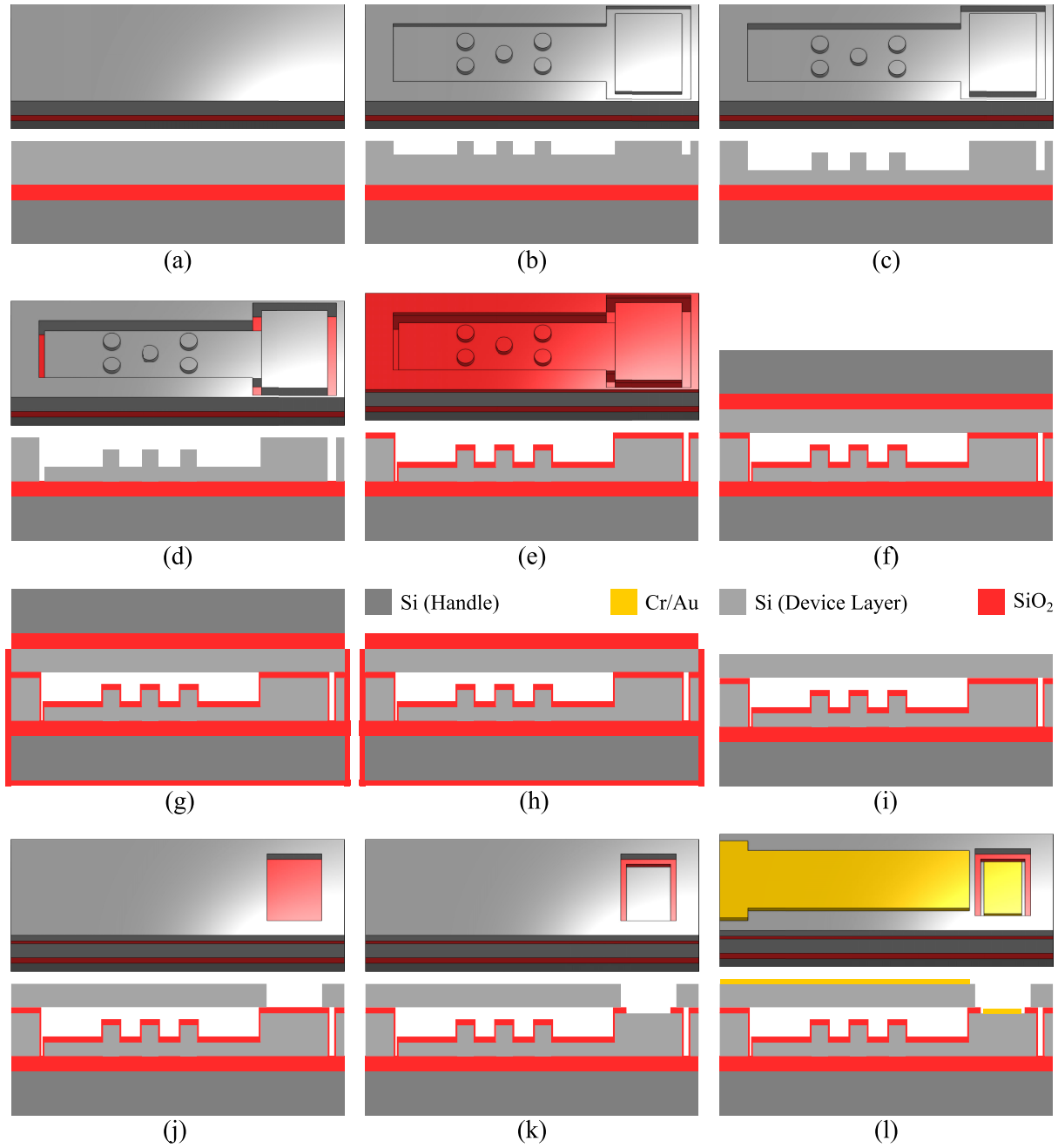


Fig. 2. Cross sections (bottom) and 3-D models (top) representing each step of our fabrication process. (a) Bottom SOI wafer is cleaned. (b) First mask step and silicon etching step define posts from the rest of the cavity. (c) Second mask step, and second silicon etch step etches entire cavity downward allowing room for membrane to deflect. (d) Third mask step and DRIE patterns trenches into the bottom electrode. (e) Dry thermal oxidation used to grow oxide layer. (f) Fusion bonding of top and bottom SOI wafers. (g) Backside protection using PECVD oxide. (h) Bulk etching of top wafer handle using DRIE or TMAH. (i) Removal of top BOX layer (and optionally backside protection) using BOE. (j) Access holes are etched into the top device layer (lithography 4 and DRIE). (k) Smaller access hole etched into thermal oxide, exposing bottom electrode. (l) Metal contacts are sputtered, patterned, and etched.

of the wafer can cause problems with photoresist coverage. As illustrated in Fig. 4(a), photoresist is typically poured into the center of the wafer and then spreads outward due to the rotation of the wafer. Any deep trenches can shield the outer portions from being uniformly covered with photoresist. An example of this effect during our fabrication process is shown in Fig. 4(b).

Even with very careful process design and pristine execution of each process step, there is always a risk of bond voids rendering portions of the wafer unusable. For this reason, we designed each mask to include multiple sets of alignment marks on each side. This reduces the chance of a bond void near a critical alignment mark complicating subsequent lithography steps.

The consequences of misalignment during lithography should also be considered, as some degree of misalignment is inevitable in an academic cleanroom. To account for this, masks were designed with tolerances for misalignment, particularly for lithography steps after wafer bonding occurs. In particular, mask step 4 (defines an access hole to the bottom

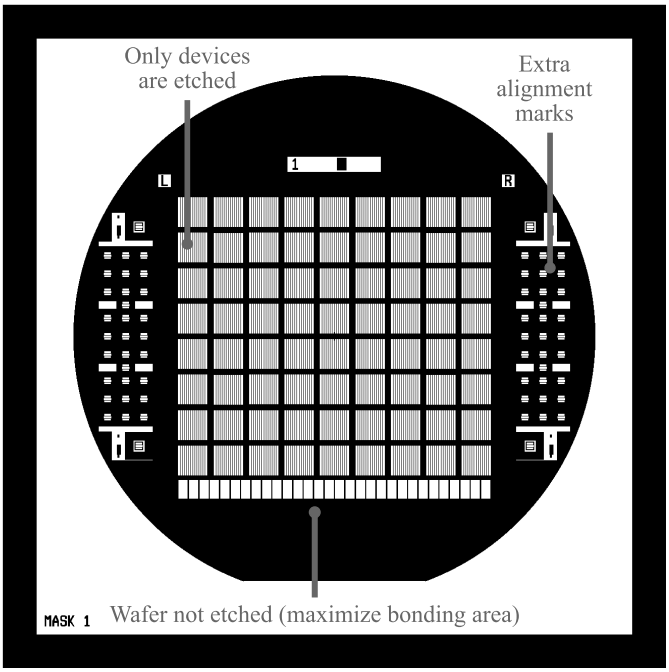


Fig. 3. Computer-aided design (CAD) representation of a photomask used for the first lithography for single-membrane EP CMUTs. Note that the only exposed areas are in the devices, alignment marks, and some features used for characterization. This approach maximizes bondable area. Also, note that there are extra alignment marks (although the amount pictured is excessive) to prevent an unlucky bond void from complicating subsequent alignment steps.

electrode) could ruin the hermetic seal within the CMUT cavity if it is misaligned on to the trenches defined by mask 3. Similarly mask step 6 (electrical contacts) could short the top and bottom electrodes if improperly aligned.

Note that in this process, it is important to design the access hole in mask 4 (etching through silicon) to be considerably larger than the access hole in mask 5 (etching thermal oxide). This leaves an oxide rim around the bond pads, which prevents electrical shorting between the top and bottom electrodes. Without the oxide rim, shorting would occur through the relatively small air gap between the two layers [6]. It is also ideal to define separate trenches around each element in mask 3, so that one compromised element does not compromise the hermetic seal of the entire array.

Finally, the minimum feature size possible on each mask should be considered. As we fabricated single-membrane CMUTs with large membranes, and reasonably large posts, using a 10-mm lens on a Heidelberg DWL-200 (2-μm minimum feature size) was sufficient for our purposes. However, minimum feature size limitations may be more critical for high-frequency devices or traditional multiple-membrane CMUT designs.

VI. Fabrication Details

In this process, the fabricated devices have features on the order of micrometers and layers less than one micrometer thick. It is, therefore, critical that these fabrication steps be performed in a cleanroom environment. In addition, these fabrication steps involve dangerous solvents, high temperatures, hazardous gases, and ultraviolet (UV) radiation. It is, therefore, imperative that anyone attempting to follow these procedures be properly trained on each process step and wear the appropriate personal protective equipment (PPE).

TABLE I
Standard Lithography Parameters

Spread Speed (RPM)	500
Spread Duration (s)	10
Spin Speed (RPM)	4000
Spin Duration (s)	40
Angular Acceleration (RPM/s)	1500
Bake Temperature (°C)	115
Bake Duration (s)	90
Exposure Dose (mJ/cm^2)	100
Development Time (s)	22

A. Starting Materials

In our fabrication, we used different SOI wafers for the top and bottom substrates. Both wafers were 100 mm in diameter, with double-sided polishing. The bottom SOI wafer was ordered from Silicon Valley Microelectronics (Santa Clara, CA, USA). These wafers had a 10-μm-thick device layer, <0.005-Ωcm device resistivity from high arsenic doping, a 500-μm handle with identical doping to the device layer, and a 300-nm-thick BOX layer. The lid SOI wafers were custom-ordered from Ultrasil (Hayward, CA, USA). These top wafers featured highly boron-doped device layers (0.001–0.005-Ωcm resistivity) that were 5-μm thick. The BOX thickness was 0.5 μm, and the handle was 400 μm thick, with high resistivity (1–30 Ωcm).

B. Lithography Procedure

We used a modified version of the lithography procedure presented by Greenlay [6], [34] for HPR 504. This lithography procedure is repeated six times throughout our process, with varied parameters. In all lithography steps except 6 (metal patterning), lithography is preceded immediately by a standard piranha cleaning and hexamethyldisilazane (HMDS) coating to improve adhesion. Standard parameters for lithography are given in Table I. This procedure yields a resist coating ~1.2-μm thick. The following steps are completed in each lithography procedure.

1) Pour ~5 mL of HPR 504 photoresist in the center of the 100-mm wafer.
   a) *Note:* This step should be completed slowly enough to prevent air bubbles from forming in the resist. However, also avoid taking so long that the resist completely covers the wafer and reaches the backside of the wafer. Dried backside photoresist may make the wafer uneven during mask alignment.
2) Spin the wafer at the "spread" speed for the "spread" duration; then, accelerate the wafer to the "spin" speed. See Table II for important spinning parameters.
3) Soft bake the wafer at 115 °C for 90 s. Ensure the hot plate is flat prior to baking. After the soft bake, remove the resist-coated wafer from heat.
4) Wait 15 min for the photoresist to rehydrate.
5) Align the photomask to the wafer using the alignment marks. For the first lithography step, a coarse alignment can be performed.

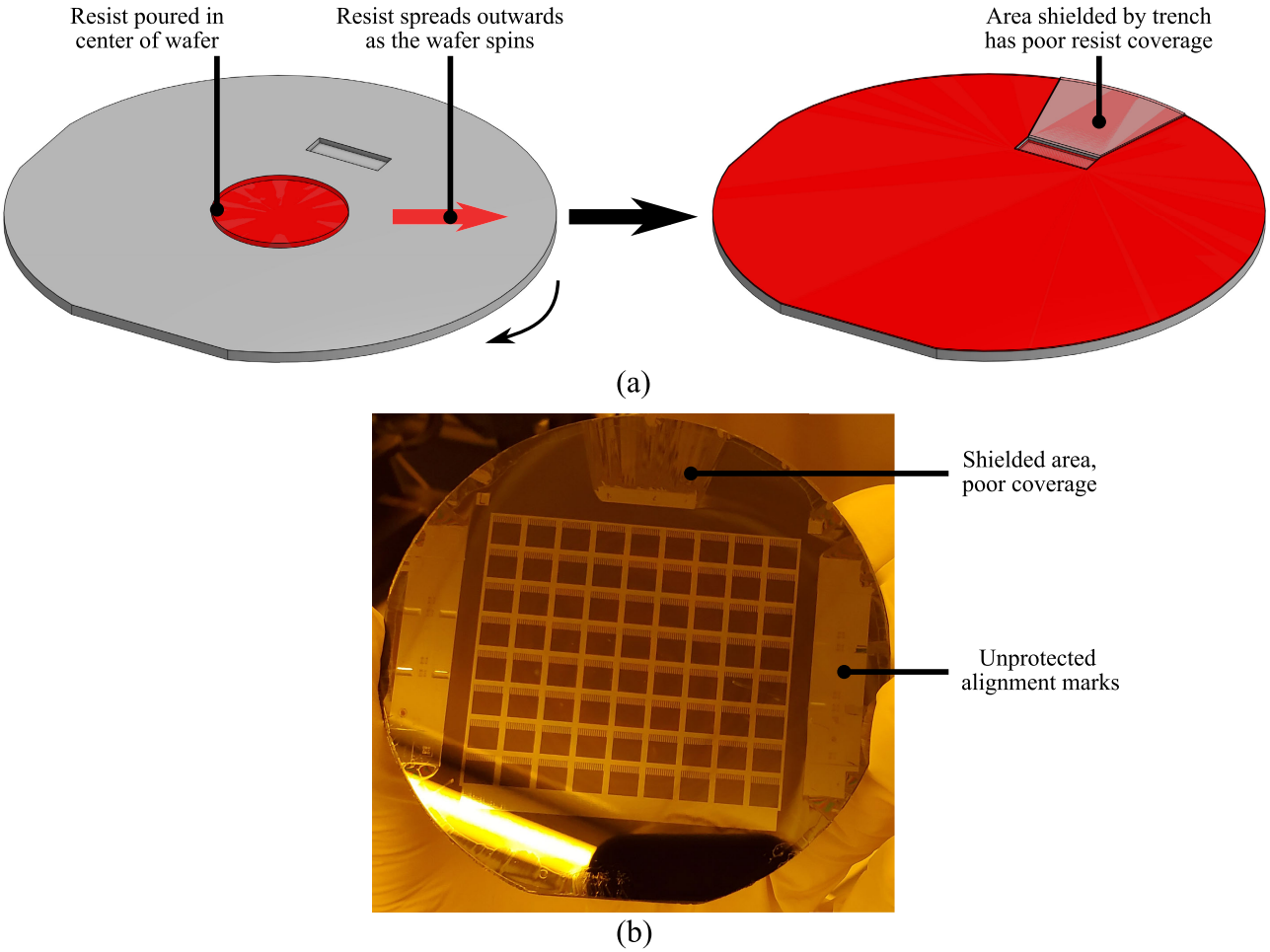


Fig. 4. (a) Illustration of photoresist coverage issues that may occur due to large height variations across the wafer. The photoresist is placed in the center and spreads outward across the wafer. However, a deep trench may prevent the resist from spreading outward at a consistent uniformity and height. (b) Photograph of a wafer after the lithography step is completed. Note the poor resist coverage in shielded areas. In addition, note that the alignment marks are not protected; thus, subsequent lithography steps do not have to be aligned through the bonded device layer.

6) Expose the photoresist to ∼100 mJ/cm^2 of UV and visible radiation using an MA6 Mask aligner (SÜSS MicroTec, Garching, Germany) or equivalent. See Table III for dose recommendations for specific lithography steps.
7) Place the wafer in a bath of diluted Microposit 351 developer (4:1 ratio between deionized (DI) water and 351). Agitate gently while developing for ∼22 s or until visual endpoint. Rinse immediately afterward with DI water.

C. Additional Considerations for Lithography

There are several instances throughout our process where deviations from the standard parameters presented in Table I are beneficial. One of these scenarios occurs after the wafer-bonding step, where a significant amount of topography is present on the surface of the wafer. This leads to difficulties achieving adequate photoresist coverage across the surface of the wafer, particularly when the trenches are greater than 5 μm in depth. Although careful mask design can mitigate these concerns (as illustrated in Fig. 4), minor changes to the standard lithography parameters can also greatly improve outcomes.

To compensate for these height variations, we suggest using ∼10 mL of photoresist for lithography steps 4–6. Using more than 10 mL did not appear to be beneficial, as the excess resist just spun off the wafer. In addition, we recommend using a longer spread step when spinning the resist and slower angular acceleration between steps, as detailed in Table II. Moreover, to compensate for greater potential variations in photoresist thickness, we recommend using an additional 20 mJ/cm^2 when exposing these wafers. The exposure doses we used for each lithography are displayed in Table III. Note that other users may have to fine-tune these values based on their available equipment and features present on their mask.

TABLE II
PHOTORESIST SPIN-COATING PARAMETERS

	Mask Step #1-3	Mask Step #4-6
Spread Speed (RPM)	500	500
Spread Duration (s)	10	15
Angular Acceleration (RPM/s)	1500	500
Spin Speed (RPM)	4000	4000
Spin Duration (s)	40	40
Photoresist Quantity (mL)	5	10

D. Cleaning and Photoresist Removal

Prior to processing, we used a standard piranha cleaning procedure to remove organic contaminants from our wafer.

TABLE III
RECOMMENDED UV EXPOSURE DOSE FOR EACH MASK STEP

Lithography Step #	Exposure Dose (mJ/cm^2)
1	100
2	100
3	90
4	120
5	120
6	400

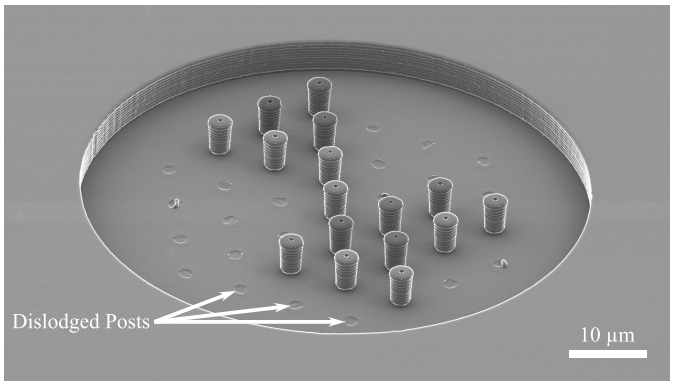


Fig. 5. Circular CMUT cavity with many dislodged posts as a result of using ultrasonic agitation to remove photoresist. Although the dimensions of this test structure (5.0-μm tall posts) are more susceptible to damage than typical designs (~300-nm height for EPs), this device illustrates the risk of using sonication in CMUTs with IIPs or EPs.

Piranha cleaning involves submerging the wafer into a 3:1 mixture of 96% sulphuric acid (J.T. Baker, 9684-05) and 30% hydrogen peroxide (J.T. Baker, 2190-03) for 15 min. Afterward, the wafer is rinsed five times in a DI water bath or dump rinser. Following the rinse, the wafer is dried using a spin rinse dryer (Semitool 870-S, Sitek, Rocklin, CA, USA). After piranha cleaning, one could optionally remove the native oxide from the wafer prior to other processing using BOE solution for 1 min (J.T. Baker, 5175). After BOE, use the same rinsing procedure as for piranha.

We found it most effective to remove photoresist by first rinsing the wafer in acetone followed by isopropyl alcohol (IPA). After the acetone/IPA rinse, the majority of the photoresist should be removed. However, there may be certain difficult-to-remove portions remaining. In this case, we used a piranha cleaning step. There are several reasons why we preferred piranha as opposed to other popular methods of resist removal, such as ultrasonic agitation (while in an acetone bath), or oxygen plasma.

The first reason is that piranha solution hydroxylates the silicon surface, preparing the wafer for HMDS coating, and the next lithography. Moreover, both oxygen plasma and ultrasonic agitation may have undesirable impacts on fabrication yield. In the case of oxygen plasma, there is a risk of increasing the surface roughness of the silicon device layer, potentially worsening bonding yield [35]. In the case of ultrasonic agitation (sonication), there is a risk of damaging membranes, or post features during later steps. An example of this effect is shown in Fig. 5, where numerous post structures etched with DRIE were destroyed after a sonication bath was used to remove photoresist. Thus, the procedure we used to remove photoresist and prepare the wafer for the next lithography is as follows.

1) Rinse the wafer in acetone.
2) Rinse the wafer in IPA.
3) Dry the wafer using filtered pressurized nitrogen.
4) Perform a standard piranha clean for 15 min.
5) Rinse at least five times in DI water.
6) Dry in spin rinse dryer.

E. Cavity and Post Patterning

Once the bottom SOI wafer has been cleaned as described in Section VI-D, processing can begin. The first three lithography steps define any post structures within the CMUT cavity, the CMUT cavity, and any trenches etched into the bottom electrode, respectively. Thus, this process can be used to fabricate traditional CD CMUTs with a trench to isolate parasitic capacitance, EP CMUTs, IIP CMUTs, or all three designs simultaneously depending on mask design. Note that in the case of CMUTs without posts, mask steps 1 and 2 could be replaced with just one mask step and a longer silicon etching time.

1) Perform a standard piranha cleaning on the bottom SOI wafer; then, apply a coating of HMDS to the wafer surface using a standard HMDS vapor prime process in a Yield Engineering Systems HMDS oven or equivalent.
2) Complete the first lithography step, using the parameters detailed in Tables I–III for spin coating, baking, exposure, and development.
3) Etch silicon to the desired depth (~320 nm for our devices) using an Oxford PlasmaPro 100 Cobra ICPRIE system or equivalent. Clean and precondition the chamber for 15 min prior to etching. We had best results using a Cl_2-based recipe with the parameters detailed in Table IV.

   Troubleshooting: The etch rate of this recipe should be calibrated for the specific masks used for lithographies 1 and 2 using an AlphaStep or other profilometer tool. It is also possible that the etch rate of this recipe depends on the doping of the wafer, as even with careful calibration and conditioning, we had differences in etch rate between our test wafers and fabricated devices.

   Note: Undercut was not an issue for our devices due to our relatively large features and shallow etch depths. However, this may be a consideration for taller or thinner posts.
4) Remove photoresist using acetone rinse followed by IPA rinse. Ensure resist is completely removed with standard piranha clean.
5) Apply coating of HMDS (shortly after piranha clean), and then, complete lithography step 2 using the parameters detailed in Tables I–III.
6) Etch silicon to the desired depth (~180 nm for our devices) using an Oxford PlasmaPro 100 Cobra ICPRIE system or equivalent. Clean and precondition the chamber for 15 min prior to etching. Use the same etching recipe as for the previous silicon etch, but note that the

TABLE IV
SILICON RIE RECIPE FOR OXFORD COBRA SYSTEM

Cl_2 Flow Rate (sccm)	25
ICP Power (W)	1000
RF Power (W)	25
Pressure (mTorr)	10
Etch Rate (nm/min)	~140
Selectivity (Si:HPR 504)	~1.5:1

etch rate may vary between masks, as the amount of exposed silicon varies.

7) Remove photoresist using acetone rinse followed by IPA rinse. Ensure resist is completely removed with standard piranha clean.

F. Patterning Trenches

This section is dedicated to patterning trenches through the bottom electrode. This is used for fabrication of IIP CMUTs [7] and for isolating the CMUT element from parasitic capacitance [as illustrated in Fig. 2(d)]. These steps could conceivably be skipped for EP or CD CMUTs; however, there may be negative impacts on performance. Also note that with the masks demonstrated in this work, this step is required to electrically isolate CMUT elements within an array from each other.

8) Apply a coating of HMDS, and then, complete lithography step 3 using the parameters detailed in Tables I–III. Note that a slightly lower exposure dose is recommended than the previous two lithography steps, as using the same dose led to slightly overexposed resist in the post regions during our experiments.

   Note: The following etch step etches through the device layer. If the bottom SOI wafer has a thick device layer, one may wish to use a thicker photoresist than HPR 504 for this lithography step. We observed ~50:1 selectivity between silicon and 504 for our Bosch DRIE recipe.

9) Etch through the device layer to define any trench structures using DRIE recipes from an Oxford PlasmaPro 100 Estrelas DRIE system or equivalent. As usual, run a chamber clean recipe and condition the chamber prior to etching actual devices. We used our tool's standard "Bosch High Aspect Ratio" etch recipe. This step can safely be overetched to ensure completion across the wafer, as there is a BOX layer that serves as an etch stop, and Bosch etching processes have reasonable selectivity between silicon and oxide. This BOX layer can also be used as a visual indicator that the etch has completed. If the BOX layer is visible, the etch has completed. If etching a thin trench through a thick device layer (typical for IIP devices), users should confirm that the aspect ratio of their DRIE recipe is suitable for etching the trench to completion using a test wafer.

   Troubleshooting: One should be careful to avoid overheating the photoresist during DRIE, as this can lead to difficulties removing the resist without the use of oxygen plasma. Thermal concerns can be particularly relevant to academic cleanroom users, as they may be required to mount their 100-mm wafers onto a larger substrate to be compatible with the DRIE machine configuration. In these situations, we recommend modifying the Bosch etching recipe to include a waiting period (~30 s) between every five cycles to allow the wafer to cool.

TABLE V
WAFER-BONDING RECIPE PARAMETERS

Tool Force (N)	1500
Bonding Duration (s)	300
Temperature (°C)	50
Pressure (mTorr)	5

10) Remove photoresist using acetone rinse followed by IPA rinse. Perform a 30-min piranha clean to ensure that resist and sidewall polymer from DRIE are removed.

    We recommend a longer piranha cleaning step to ensure sidewall polymer is adequately removed.

G. Thermal Oxidation

As the quality and smoothness of the thermal oxide are critical to device performance, care should be taken to optimize this step. We recommend performing a piranha or RCA cleaning process immediately prior to thermal oxidation. We also recommend including several "baffle" wafers in front of and behind the device wafers to optimize gas flow, as we observed poor uniformity on the wafers at the front of the tube.

11) Perform a dry thermal oxidation at 1100 °C using a Tystar Tytan-Mini or equivalent. Oxidation for 5 h and 36 min should yield a 360-nm-thick thermal oxide. Include at least one prime wafer to measure oxide thickness.

H. Wafer Bonding

Wafer bonding is the most challenging and yield-critical step in this process, and the utmost care should be taken to ensure optimal cleanliness of each wafer prior to bonding. We recommend performing every step of the RCA cleaning process immediately prior to bonding, and then annealing immediately after all wafers are bonded.

12) Perform RCA cleaning on both the processed bottom SOI and the top "lid" SOI wafer.
    a) RCA clean should be performed with unique glassware that is not used for other processes to minimize contamination.
    b) *Standard Clean 1 (SC1):* Mix a 5:1:1 solution of DI water, hydrogen peroxide (J.T. Baker, 2190-03), and ammonium hydroxide (Sigma Aldrich, 40205), respectively. Heat solution to 80 °C. Immerse wafers for 10 min.
    c) Rinse wafers in DI water six times.
    d) *HF Dip:* Prepare a 50:1 solution of DI water and 49% hydrofluoric acid (J.T. Baker, 9564-06). Insert wafer for 30 s. Etching of the thermal oxide during this process should be negligible.
    e) Rinse wafers in DI water six times.
    f) *Standard Clean 2 (SC2):* Mix a 6:1:1 solution of DI water, hydrogen peroxide (J.T. Baker, 2190-03),

TABLE VI
STANDARD OXIDE ETCHING RECIPE FOR TRION PHANTOM RIE

Forward RF Power (W):	125
CHF_3 Flow Rate (sccm)	40
O_2 Flow Rate (sccm)	5
Pressure (mTorr)	40
Etch Rate (nm/min)	~35
Selectivity (SiO_2:HPR 504)	~1:1

and hydrochloric acid (J.T. Baker, 9539-05), respectively. Heat solution to 80 °C. Immerse wafers for 10 min.

g) Rinse wafers in DI water six times.

h) Spin dry bottom and top SOI wafer pair, and then, immediately insert into wafer bonder.

Critical: For batch processes of multiple wafers, leave each wafer in the DI rinse until it is ready to be spin-dried and bonded. Exposure to cleanroom air for any longer than necessary can lead to contamination that severely impacts bonding yield.

13) Insert each wafer pair into the wafer bonder (SÜSS MicroTec CB6L or equivalent). Bond recipe is given in Table V.

14) Anneal the bonded wafers as soon as possible at 1100 °C for 70 min in nitrogen gas using a Tystar Tytan-Mini or equivalent.

Be very careful removing the bonded wafers from the quartz wafer holders, as they are often slightly too thick for the holders. This can lead to small chips breaking off of the wafers, which makes them more susceptible to breakage or unwanted etching in the subsequent steps.

I. Bulk Si Etching

The next set of process steps is centered around removing the handle portion of the lid SOI wafer, such that the device layer can be used as a membrane. The two main processes available for this task are DRIE processes and TMAH. However, due to nonideal uniformity in DRIE machines and insufficient selectivity between the oxide and the silicon in dry etching processes, use of wet etching is necessary. However, the drawback of TMAH etching is that it also etches the handle of the bottom SOI wafer, leading to unwanted wafer fragility. It is viable to complete our process using only TMAH etching. However, we recommend using DRIE to remove approximately two-thirds of the top SOI wafer's handle to reduce the amount of time the wafer spends in TMAH.

15) Place the bonded wafers upside down into a Trion Orion PECVD or equivalent, such that the bottom SOI wafer is facing upward. The bottom SOI wafer should be easily identified due to the thermal oxide layer present. Deposit up to 1600 nm of PECVD oxide to protect the backside of the wafer.

One could probably use a much smaller amount of PECVD oxide to protect the wafer, due to the high selectivity between TMAH and silicon dioxide. However, our tool deposits poor quality films, with poor uniformity, so we deposited an excessive amount to ensure the backside was adequately protected.

16) There will be a ring of oxide on the handle of the lid (unoxidized) SOI wafer. Remove this using the standard "oxide" recipe of any RIE machine, as it will reduce the bulk silicon etch rate around the edges of the wafer. An example oxide etching recipe is given in Table VI.

17) Use a DRIE machine to etch approximately two-thirds of the lid wafer handle using an unswitched SF_6 process (polymer deposition is unnecessary for bulk etching).

18) Place the wafers in a bath of TMAH (J.T. Baker, 5879-03) heated up to 95 °C. Ensure that this step is performed inside a fume hood with a condenser above the TMAH bath. The TMAH bath should also be agitated by a magnetic stir rod. Note that the native oxide on the top silicon handle should be removed using RIE prior to putting the wafer in TMAH, as even the native oxide considerably slows the etching process. Leave the wafers in TMAH until the top Si handle is removed and the BOX layer on the top wafer is visible. Rinse the wafer with DI water five times.

In our experiments, we observed much faster etch rates at 95 °C as compared with 88 °C.

J. Handling Fragile Wafers

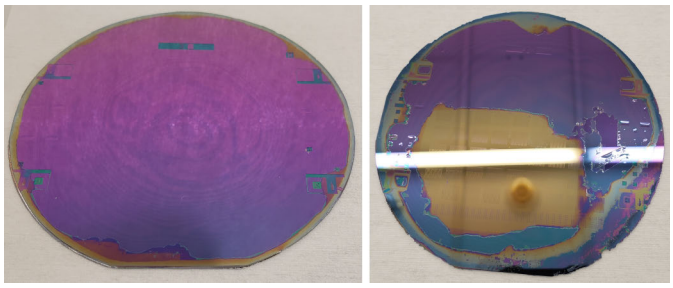
Depending on the amount of time the wafers spent in TMAH, they may now be quite fragile around the edges. To reduce the likelihood of the wafer breaking, we recommend avoiding automatic dump rinsers for any rinses after the wafers are etched in TMAH. Instead, one should fill two large baths with DI water, and alternate moving the wafer between baths, then replacing the DI water of the unoccupied bath. The wafer should still be rinsed at least five times after any process involving dangerous solvents to minimize safety hazards and risk of contamination. However, this approach is more gentle than an automatic dump rinser. Some users may also prefer handling wafer edges with a clean set of gloves in certain scenarios as opposed to metal wafer tweezers.

K. Assessing Bonding Yield

After removing the handle, but before removing the BOX layer of the top SOI wafer is an ideal time to assess bonding yield. In places where the wafer successfully bonded, the BOX layer of the top SOI wafer should be visible, while locations with poor bonding will instead show the bottom wafer (with a different thickness of oxide that is often easily distinguishable as a different color). Examples of good and poor bonding are displayed in Fig. 6.

L. Etching Access Holes

These steps are designed to etch access holes through the top device layer in order to access the bottom electrode, as shown in Fig. 2. At this point in the process, the wafer begins to have a greater degree of height variation. Thus, the parameters in Table II should be used to ensure complete resist coverage.



(a) (b)

Fig. 6. Photographs of wafers after handle removal illustrating (a) good and (b) bad bonding yield.

To compensate for increased uncertainty in the thickness of the photoresist, we also suggest using slightly higher exposure doses during lithography (Table III). For the following steps, remember that the wafer is fragile and should be handled carefully.

19) Remove the BOX layer of the lid SOI wafer using BOE. For a 500-nm BOX layer, this should take ∼15 min (including some overetching time). Rinse the wafer at least five times using DI water baths.
20) Perform a standard piranha cleaning on the bonded wafer pair, and then, apply a coating of HMDS.
21) Complete lithography step 4 using the parameters detailed in Tables I–III.

    Note: Users with old lithography systems may have difficulty aligning through the newly bonded device layer. However, this was quite simple using a SÜSS MA6 system.

    Note: If the bonded (top membrane) device layer is very thick, one may wish to use a thicker photoresist for this lithography, as the following etching step etches through it. In our tests, we had ∼50:1 selectivity between our Bosch DRIE recipe and HPR 504.
22) Etch access holes through the top silicon layer using DRIE recipes from an Oxford PlasmaPro 100 Estrelas DRIE system or equivalent. Clean and precondition the chamber prior to etching. Use the same recipe as for the trench DRIE etch. Some degree of overetching is allowable for this step, but as much of the bottom oxide should be left intact as possible.

    The same considerations from the previous DRIE step about photoresist heating apply. Although now that the wafers are bonded, using oxygen plasma to remove any hard baked photoresist is less likely to adversely affect yield.
23) Remove photoresist using acetone rinse followed by IPA rinse. Ensure resist is completely removed with standard piranha clean.
24) Apply coating of HMDS (shortly after piranha clean) then complete lithography step 5 using the parameters detailed in Tables I–III.
25) Etch the silicon dioxide using the "oxide" RIE recipe on any RIE machine, leaving the bottom electrode exposed. Slight overetching is not problematic for this step. An example oxide-etching recipe is provided in Table VI.
26) Remove photoresist using acetone rinse followed by IPA rinse. Ensure resist is completely removed with standard piranha clean.

M. Contact Deposition and Patterning

27) Ensure that the wafer has been recently piranha cleaned, and remove any native oxide using an RIE machine or BOE. Then, deposit ∼250 nm of Cr/Au using magnetron sputtering. For our devices, we used 26 nm of Cr and ∼250 nm of Au. Note that it may be difficult to wire bond to contacts less than 200-nm thick.
28) Perform lithography step 6 (no piranha or HMDS beforehand) using the parameters detailed in Tables I–III. Note that this final step is usually deliberately overexposed to account for resist thickness variations inside the access holes. As a result, we avoided designing small features on this mask.
29) Wet etch the gold using a solution of potassium iodide, iodine, and DI water. This solution can be prepared by dissolving 75 g of iodine and 300 g of potassium iodide in 3000 mL of DI water. It is highly preferred to define contacts by wet etching, as sputter-etching (ion milling) risks redepositing the gold within the access holes, potentially leading to electrical shorts.
30) Wet etch the chromium using commercial chromium etchant (Chrome Mask Etchant 9030, Transene, Danvers, MA, USA). Again, wet etching is highly preferred over sputter etching for this step.
31) Remove the photoresist using acetone rinse followed by IPA rinse. The devices are now complete. Optionally perform wafer-level characterization before dicing and packaging steps.

Images of the completed devices are available at various magnification levels in Fig. 7(a)–(e).

VII. Characterization

During fabrication, there are limited means of characterizing CMUTs. In the cleanroom, one can visually inspect for defects, examine the size of features, and measure the thicknesses of films or etched trenches. However, this information often does not fully predict which devices will function, or how well they will perform. Nevertheless, once fabrication is completed, researchers have many powerful characterization options at their disposal.

For users with access to an automated semiconductor characterization tool, such as the Keithley 4200-Semiconductor Characterization System, capacitance–voltage (CV) measurements can be an easy and valuable method of assessing device functionality. Although CV sweeps only capture the static behavior of the membrane, these measurements can provide valuable insights, such as the collapse voltage of the membrane and the electromechanical efficiency [3], [36]. CV testing can allow researchers to identify bad elements without performing more time-consuming tests. Repeated CV measurements can also be used to induce charging, allowing one to evaluate the device's reliability [7]. An example electromechanical

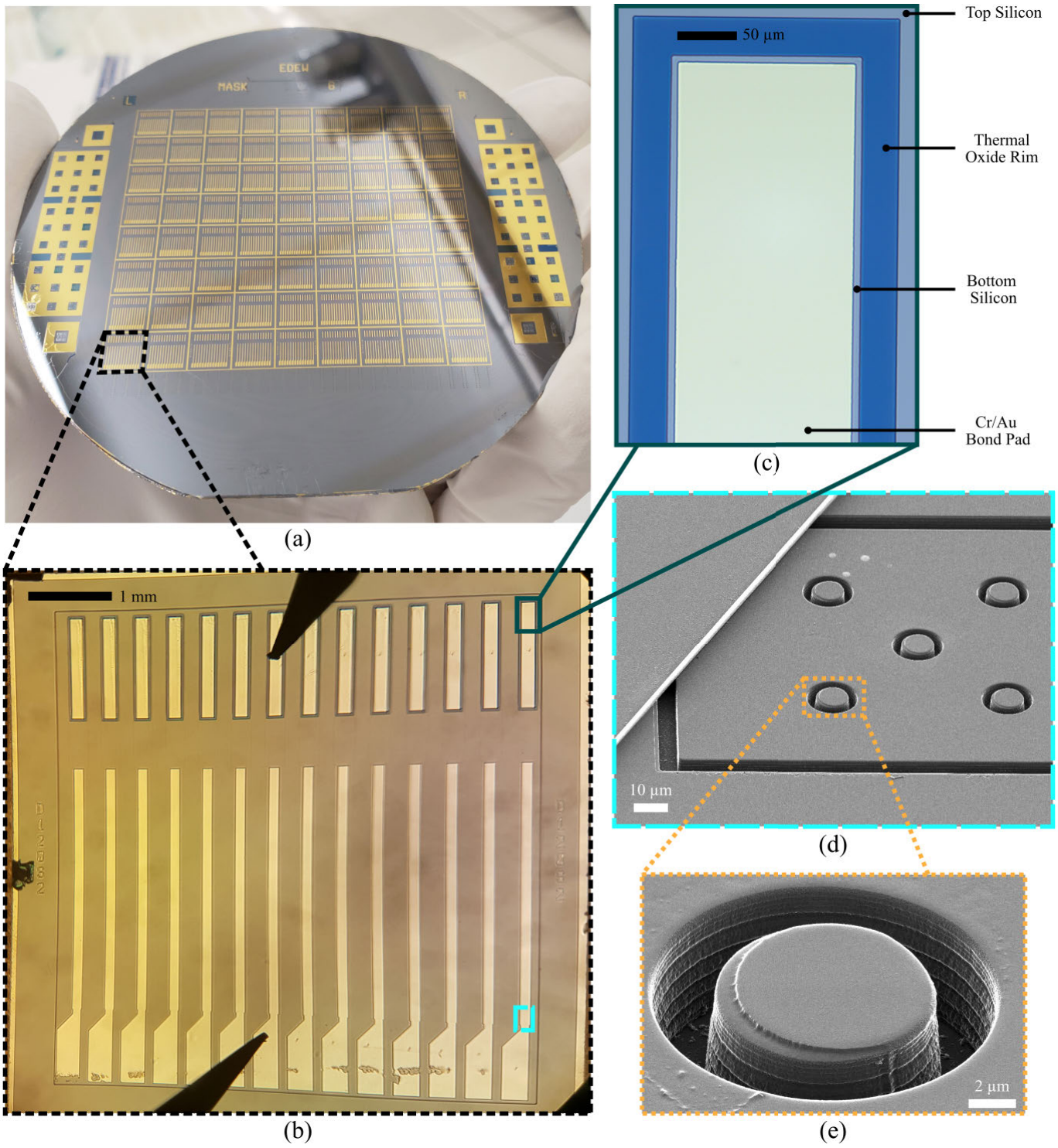


Fig. 7. Completed devices. (a) Completed 100-mm wafer. (b) Microscope image of a single die of IIP CMUTs during electrical testing. The two dark objects connected to the bond pads of the seventh element are probe tips. (c) High magnification microscope image of the bond pads of a single CMUT element. Note that a large thermal oxide rim is necessary to separate the top and bottom electrodes, or else the air gap between the top and bottom silicon becomes an avenue for dielectric breakdown. (d) Helium ion microscope image of a dissected IIP CMUT (rotated 90° clockwise relative to the previous views). This image includes a portion of the membrane, the isolation trenches, bottom electrode, and IIP structures. (e) Close-up view of a single IIP (helium ion microscopy). The slightly misaligned circular portion in the center is the EP, although it is electrically floating in this instance. Note that the periodic large "scallops" in the sidewalls are due to a waiting step between every five Bosch etching cycles.

efficiency curve for an EP CMUT is provided in Fig. 8. The measured electromechanical efficiency values of traditional CD CMUTs, EP CMUTs, and IIP CMUTs are compared in Table VII.

The static behavior of CMUT elements can also be investigated using an optical profilometer, such as the NewView 5000 (Zygo Corporation, Middlefield, CT). Assuming the relevant CMUTs are opaque, profilometers can be used to measure

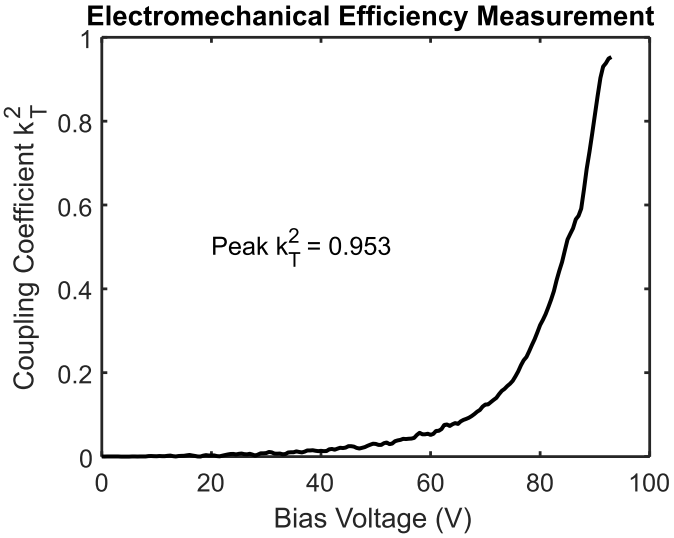


Fig. 8. Electromechanical efficiency of a single-membrane EP CMUT as derived from CV testing. See [7] for more detailed characterization results, and comparisons with other designs.

TABLE VII
ELECTROMECHANICAL EFFICIENCY MEASUREMENTS (TAKEN FROM [7])

Device Type	Mean k_T^2	k_T^2 Standard Deviation	Max k_T^2	Lowest k_T^2
CD CMUT	0.84	0.02	0.87	0.81
EP CMUT	0.92	0.02	0.95	0.88
IIP CMUT	0.69	0.03	0.75	0.62

the deflection of the membrane for a given bias voltage [Fig. 9(a) and (b)]. This can be used to compare with predictions from finite-element or analytical models, determine the collapse-point, or measure the hysteresis present in a CMUT element.

The dynamic behavior of a CMUT element may be measured in air using a laser-Doppler vibrometer (MSA-500, Polytec, Baden-Württemberg, Germany). The signals generated by the vibrometer can be superimposed on a dc bias from an external power supply using a bias tee, allowing characterization of the CMUT's resonant frequency for any bias voltage. Typically, the vibrometer will be used to measure the membrane movement in response to pseudorandom signals to determine the resonance frequency, as shown in Fig. 10(a). Once the resonance frequency is determined, one can apply a sinusoidal driving signal at the membrane's resonance frequency, and then scan the vibrometer to observe the vibration of the entire membrane. An example of this for single-membrane CMUTs is shown in Fig. 10(b).

To obtain measurements in immersion, the devices must be diced and packaged appropriately. In a research setting, it is common to wire bond a CMUT array to a custom printed circuit board (PCB), and then use waterproof sealant to attach a tank to the PCB. Although the CMUTs are not electrically isolated, and thus cannot be used in water, this configuration allows one to easily perform immersion measurements in vegetable or mineral oil.

The immersion frequency response of a device can be characterized with an impulse-response measurement. This

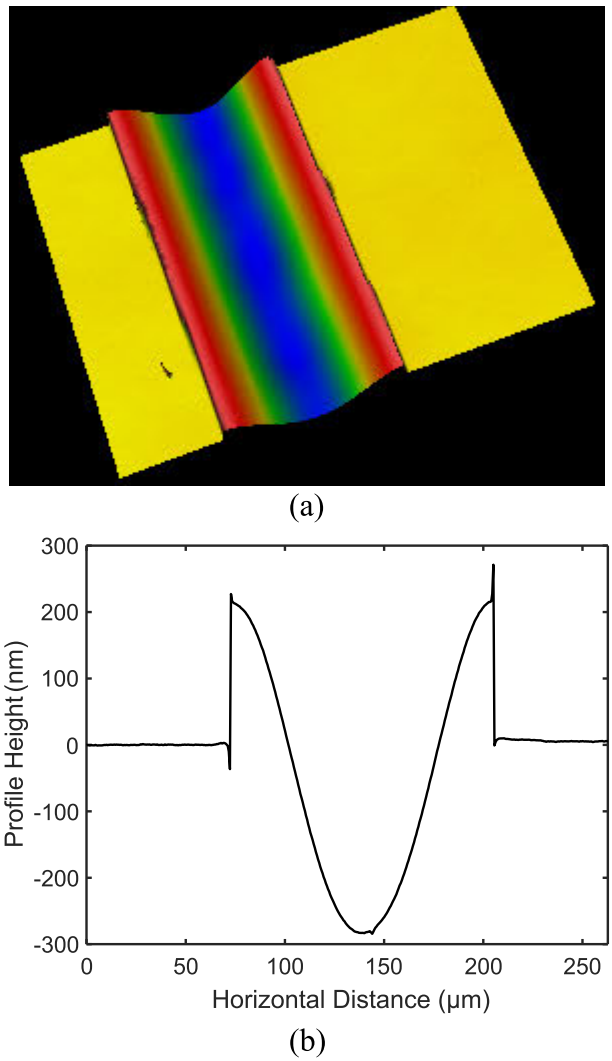
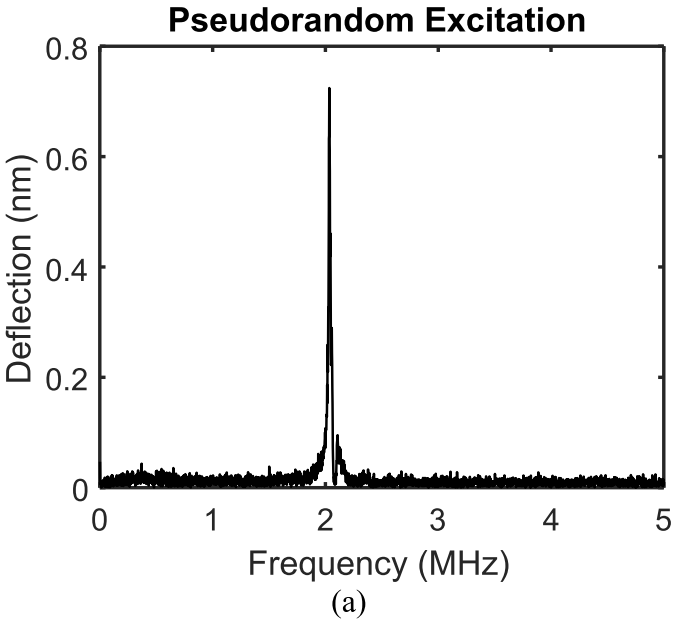


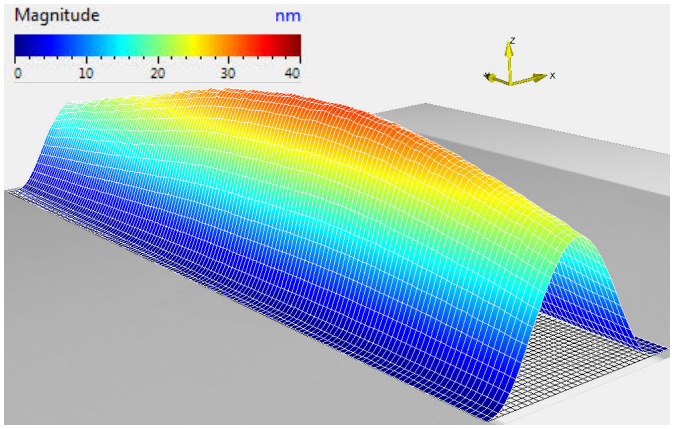
Fig. 9. Profilometer measurements of a single-membrane CD CMUT. (a) 3-D model of the measured profile near the center of a collapsed membrane. (b) Measured height profile used to determine membrane deflection. Note that the 200-nm height increase is due to the Cr/Au contact on top of the membrane, as illustrated in Fig. 7(b).

involves receiving the transmitted signal with a hydrophone (HNP-400, Onda Corporation, Sunnyvale, CA) while applying a sharp (broadband) voltage pulse to the CMUT. An example waveform obtained from a single EP CMUT element driven with a pulser–receiver (5800PR, Olympus Corporation, Shinjuku, Tokyo, Japan) is shown in Fig. 11. However, note that the voltage pulse from a pulser–receiver may have a peak–peak amplitude of greater than 200 V and, thus, may cause dielectric breakdown. As a result, many researchers may prefer to use smaller amplitude step function or pulse inputs from an arbitrary function generator instead.

Other valuable measurements include receive sensitivity [8], noise-equivalent pressure (NEP) [37], transmit efficiency [7], [27], and impedance measurements [8]. However, techniques for these measurements are well described in other works. In the case of transmit efficiency, note that it is common to report the estimated surface pressure, corrected for diffraction and attenuation along with the measured hydrophone pressure [7], [14], [27], [38]. Also note that a given device will demonstrate more impressive transmit efficiency metrics



(a)



(b)

Fig. 10. Laser-Doppler vibrometer measurements of a single-membrane IIP CMUT biased at 80 V. (a) Deflection measurement of a central point on the membrane in response to 10-V pseudorandom signals. (b) Vibrometer scan of the central portion of the membrane in response to 10-V sinusoidal excitation at the resonance frequency (2.0844 MHz).

if driven with longer pulse trains containing more energy. However, such long pulse trains are generally impractical for imaging due to their long spatial pulselength. Finally, electron microscopy is very useful for diagnosing devices that perform poorly in the above tests.

VIII. Discussion

Many papers only give superficial details about their fabrication processes. In this manuscript, we aim to provide a lot of details, best practices, and pitfalls to avoid while fabricating wafer-bonded CMUTs. We hope that this extensive detail can be valuable to the ultrasound community and to new researchers interested in CMUTs. Although this manuscript focuses primarily on single-membrane EP CMUTs, the strategies we mention are often applicable to many other designs.

We focus on EP devices, because they have recently been shown to offer performance benefits while also substantially improving device reliability [7]. The combined achievement

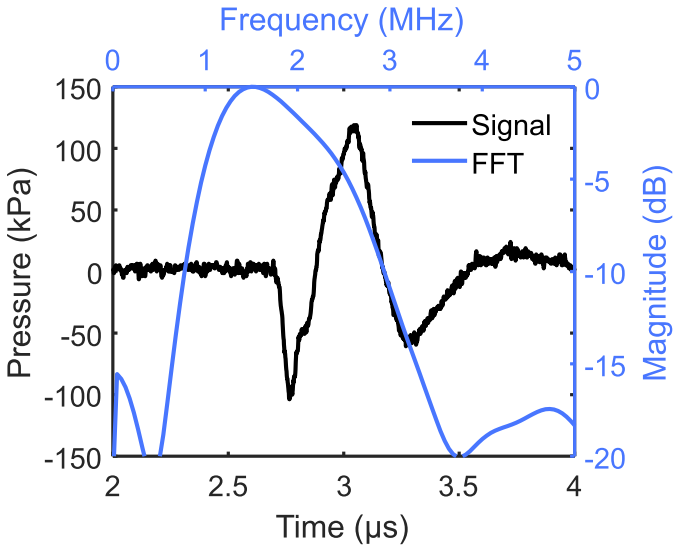


Fig. 11. Impulse-response measurement of a single unbiased EP CMUT in response to a 50-μJ pulse. The pressure measurement was recorded at the location of the hydrophone (no correction for attenuation or diffraction). The 6-dB fractional bandwidth of this device is 114.5% with a center frequency of 1.50 MHz.

of high yield, high reliability, and improved performance in CMUTs has great potential to disrupt the ultrasound industry and compete with piezoelectric devices, which have, thus, far been the gold standard for most ultrasound applications. Despite the very promising initial results, there are several areas of our device design and fabrication process that could be further optimized.

One key difference between the wafer-bonded process presented in this work and more traditional wafer-bonded processes presented elsewhere [12], [19] is the method for defining cavity height. Traditionally, the height of the CMUT cavity is defined by a thermal oxidation step, which has a very predictable growth rate, giving very precise control over the cavity height. In our process, the height of the cavity is determined by reactive ion etching of silicon. This approach has several key advantages, including contiguous oxide coverage throughout the cavity from a single oxidation step, no cusps which negatively impact bonding yield, no precharging of the oxide during dry etching, and reduced wafer fragility from TMAH etching (due to additional protection from the unetched thermal oxide) [7]. However, a drawback of this approach is that silicon RIE rates are less consistent than thermal oxidation, and thus, our tolerances in cavity height and post height were coarser than traditional approaches. We believe this drawback could be mitigated with further development of silicon RIE recipes.

Using our current silicon RIE recipe, we observed $\pm 8\%$ uniformity across a wafer for mask steps 1 and 2. This primarily impacts the height of the CMUT cavity and the height of the posts (which are defined by timed etches). Although these variations do not have a substantial impact on resonant frequency (which is primarily determined by the width of the cavity and thickness of the membrane), they do impact the collapse voltage of the devices. As other

authors have reported uniformities of ±1% or better in timed high aspect ratio DRIE etches, it is likely that this could be considerably improved with more attention toward the silicon RIE recipe [39]. It would also be desirable to perform these process steps with a slower etch rate to reduce the potential for deviations between the intended and etched dimensions.

The most successful generation of devices used a highly arsenic-doped bottom electrode and boron-doped top electrode. Notably, the handle of the bottom SOI was also highly arsenic-doped. During capacitance measurements, we noticed that individual elements from this generation had up to 50 pF more capacitance than previous generations despite having the same dimensions. This is likely related to two different factors. One important consideration is that the highly doped handle likely acted as an additional floating electrode, forming parasitic capacitance with the bottom electrode through the BOX layer. We, therefore, recommend using SOI wafers with high handle resistivity (as with our previous generations of devices) to avoid this parasitic effect. It is also possible that the capacitance may be impacted by the different dopants within the top and bottom electrodes, although the electrodes are separated by 360 nm of thermal oxide in all regions.

An important area for improvement in our design is in preventing dielectric breakdown. This was the primary challenge during characterization, particularly for impulse-response tests using a pulser–receiver or for transmit efficiency tests in collapse mode or using large transmit signals. Thermal oxide is often estimated to have a breakdown voltage of 1 V/nm; thus, with 360 nm of contiguous thermal oxide, one would expect our devices to operate above 300 V. In reality, breakdown would sometimes occur in our devices as low as 150 V. One possible explanation for this breakdown is nonideal thermal oxide quality, as other users of our cleanroom have measured the breakdown strength of their thermal oxide as being closer to 0.5–0.7 V/nm [6]. Although, it should be noted that their oxide was grown on highly boron-doped silicon as opposed to arsenic-doped silicon and, thus, may have different properties. It is also worthy of note that most breakdown instances occurred near the bond pads (as evidenced by burn marks in those regions); thus, wire-bond encapsulation or simply designing bond pads with larger oxide rims may also address this issue.

Finally, our devices are relatively small compared with typical array elements ($\lambda/8 - \lambda/6$ width). This could be improved within the single-long-rectangular-membrane paradigm by increasing the width of the membrane (decreases resonant frequency and decreases collapse voltage) and increasing the thickness of the membrane (increases resonant frequency and increases collapse voltage). Based on some initial modeling, it seems plausible that calculated changes in membrane width and thickness could substantially improve the width of the element while keeping the resonance frequency constant and with only minor increases in collapse voltage. However, this approach would also have additional challenges, such as aligning mask step 4 through a thick device layer. Another possible approach to achieving more practical linear array dimensions is to design membranes to actuate in a more piston-like manner [25], [26], [27]. Both of these approaches would benefit from more sophisticated analytical or computational models beyond the simple electrostatic analysis we presented previously [7]. In particular, dynamic models of EP CMUTs, rectangular membranes, and piston-like rectangular membranes would be extremely valuable.

IX. Conclusion

CMUT technology was proposed over 25 years ago. However, performance and reliability issues have hampered widespread adoption. Building on the work of many previous contributors, we recently developed a promising architecture and fabrication process, which achieves good long-term reliability, electromechanical efficiency, and transmit performance, rivaling and even exceeding broadly adopted piezoelectric transducer technology. This article outlines a detailed roadmap for the fabrication process that we found effective for producing these devices. Many of the process steps are known to microelectromechanical system (MEMS) experts, but less commonly described in detail. It is the purpose of this article to provide best practices as well as common pitfalls, which we hope will be of use to the research and industrial communities.

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