News From Japan

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Development of a Highly Durable SiC Power Device for Electric Vehicles

As a part of the UN's Sustainable Development Goals (SDGs) and those agreed to at the 2015 UN Climate Change Conference (COP21) held in Paris, energy consumption needs to be reduced. One of the effective ways in achieving this goal is to reduce electrical energy consumption by replacing fixed speed drive systems with variable speed ones, so that less energy is used when loads are reduced. Modern variable speed motors are fed from electronic inverters, which modulate the widths, amplitudes, or frequencies of pulse voltages that are fed to them. The heart of such a pulse modulation system, consisting of converters and inverters, is power transistors.

There are two types of power transistors that are currently widely used. These are bipolar power transistors and power metal oxide semiconductor field-effect transistors (MOSFETs). The bipolar transistors use relatively slow minority carriers in their switching operations, have relatively low voltage withstand levels and require relatively long times for switching operations. A major advantage of MOSFETs over bipolar transistors is that MOSFETs use majority carriers for their switching operations and are therefore much faster. Although the voltage withstand levels of power MOSFETs in early days were not too high, this level was gradually increased by improvements of their design, such as the adoption of a double diffusion MOS (DMOS) structure, as shown in Figure 1(a).

One of the most important industrial goods that can significantly benefit from the availability of high-speed high-voltage power transistors are electric vehicles (EVs), in which electric motors controlled by power electronics are used instead of combustion engines. Furthermore, the reduction of the electric power consumption in EVs is essential from the above-mentioned viewpoint of global energy saving as the use of EVs is expected to spread explosively in many countries.

Until recently, power electronic devices have mainly been based on silicon (Si) as the principal semiconductor material, regardless of whether in bipolar transistors or MOSFETs. A new generation of power electronic devices has recently emerged based on silicon carbide (SiC) as the principal semiconductor material and is attracting attention of researchers and potential users. They can operate at much higher voltage levels than those using Si and therefore, can offer significant saving of energy consumption in converter-inverter systems.

As mentioned above, the structure of conventional power MOSFET is of DMOS type, in which the on-resistance is not low enough for effectively securing the high power flow. Another issue common in SiC power devices is that their on-resistance may vary greatly, unlike in Si based ones, depending on the positioning of SiC crystal plane. To resolve this issue, a trench SiC MOSFET, shown in Figure 1(b), has been introduced to pass the electric current along the crystal planes of a lower resistance. However, because of the complex structure of the trench MOSFET, electric field concentrated at the trench edge on the base plane is high and strongly contributes to a decreased durability of the device.

To solve this concern, Hitachi has recently developed a new structure, called original fin-formed trench DMOS-FET or, for short, TED-MOS. In this new type of field effect transistor, the reduction in on-resistance is achieved because of the smaller trench pitch. It can also provide a higher durability, since the maximum electric field is reduced in the device and therefore the new DMOS-FET can be applied to various industrial applications that require high-rated voltage levels, up to 3.3 kV [1].

Very recently, Hitachi has further advanced this TED-MOS structure, so that it becomes suitable for converter systems of EVs that require high current density at a relatively low voltage of 1.2 kV. As shown in Figure 1(c) by its schematic illustration and cross-sectional photograph along the line A-A', the new TED-MOS has a field relaxation layer (FRL) on the top of a PN junction formed at the center of the device. It allows to significantly reduce the electric field strength on the PN junction, which is formed as a part of an n-type junction FET (JFET). The newly proposed TED-MOS has also a current spreading layer (CSL) to reduce the resistance in the n-JFET region, by which the path of the flowing electric current connects the n-JFET to the two sides of the fin-like trenches composed of low-resistance SiC crystal [2].

Results of electric field simulations at the cross-sections of a DMOS and those of the conventional and newly proposed TED-MOSs, without and with the field relaxation layer, are shown in Figure 2. Since the channel is formed in the two TED-MOSs at a certain depth from the substrate surface, the insulator thickness above the JFET region can be easily increased. Therefore, the electric field intensity Eox above the JFET can be reduced in the insulating oxide to a negligibly low level. The maximum Eox should appear at the gate oxide on the trench. The lower parts of Figure 2 show that the conventional TED-MOS can suppress the highest value of Eox by 25% from 2.4 MV/cm to 1.8 MV/cm compared to the DMOS. However, the doses of implanted ions in the CSL and JFET are extremely high and the depth of CSL (Wd) is limited, as shallow as 170 nm (Figure 2).

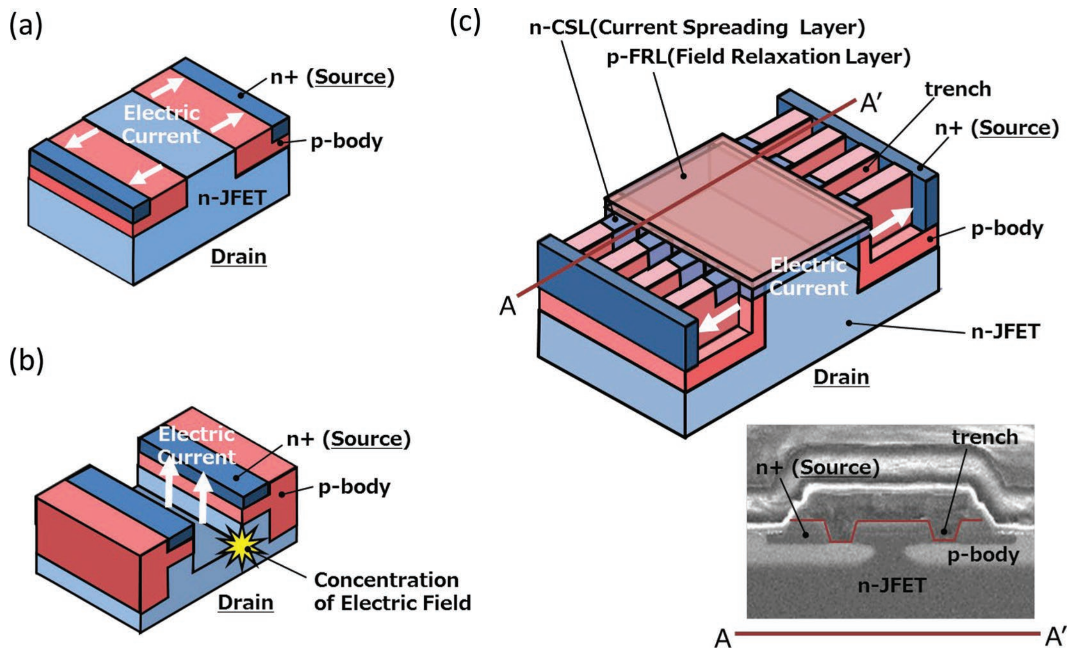

Figure 1. Schematic illustrations of MOS-FETs. (a) Conventional DMOS-FET, (b) Trench MOSFET, (c) TED-MOS.

The proposed TED-MOS with the field relaxation layer (FRL) can reduce Eox even more effectively, reaching, with a deeper Wd, 42% from 2.4 MV/cm to 1.4 MV/cm, as compared to that of DMOS. Figure 3 shows the dependence of Eox on Wd. It is clearly indicated that Eox remains low in the proposed structure in a wide range of Wd. Therefore, a good balance can be achieved between Wd and the trench depth to reduce the channel resistance Rch.

Thanks to this innovation, the newly proposed SiC based TED-MOS successfully realizes, simultaneously, both require-

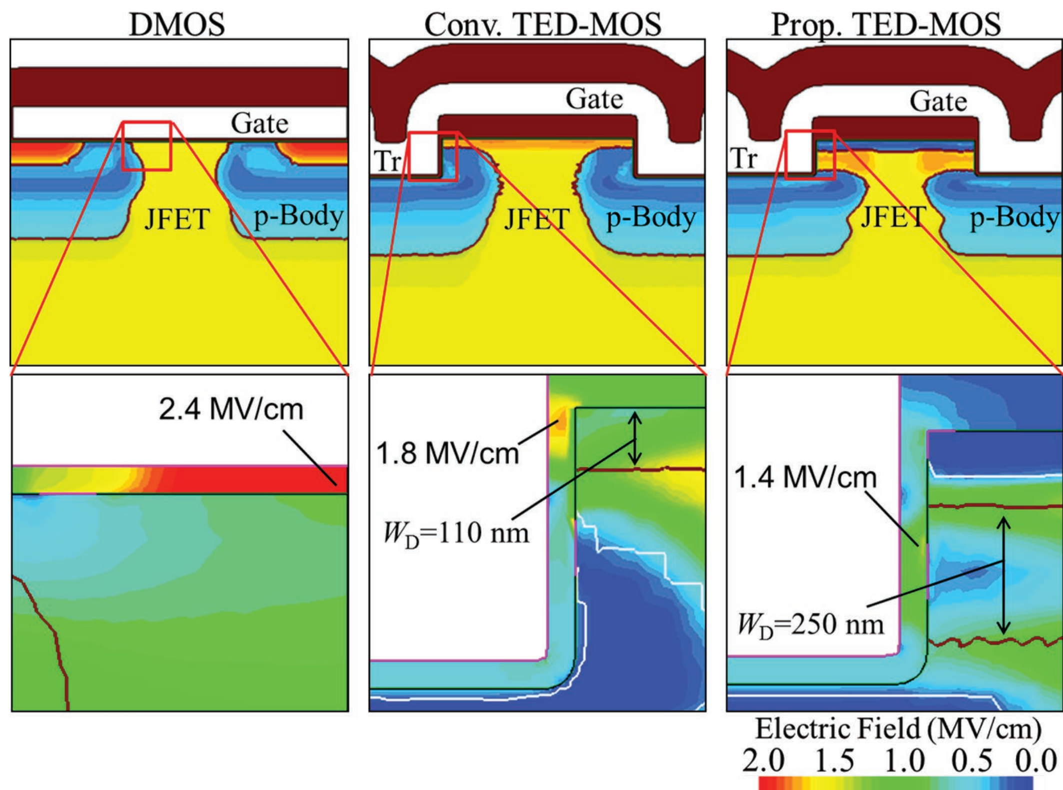

Figure 2. Simulation of E_{ox} in DMOS and the two TED-MOSs, conventional and proposed with FRL.

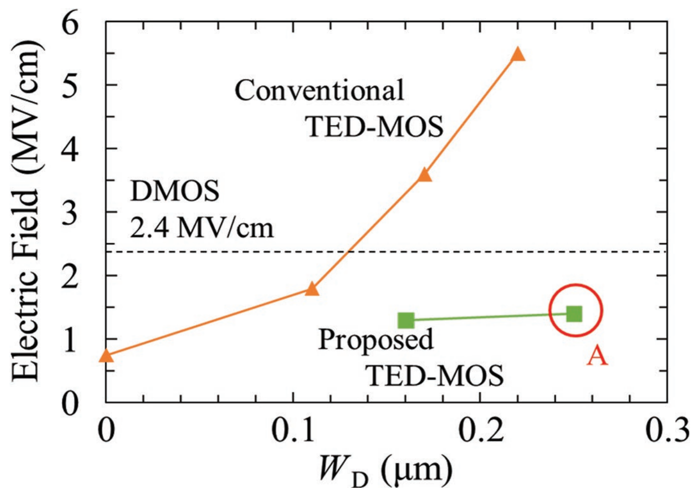

Figure 3. E_{ox} in each structure as a function of W_D. Letter A represents the condition employed for the fabrication.

ments, i.e. lower electric field and lower on-resistance as compared with conventional TED-MOS devices. It is shown in Figure 3 that in the new TED-MOS the highest electric field is reduced by 40% compared to that of the conventional DMOSFET, while maintaining the rated voltage of 1.2 kV. The highest resistance is also reduced by 25%. The letter A in Figure 3 represents the values of Eox and Wd employed in fabrication of the new device. Furthermore, the modified structure allows for further shortening the on/off switching operation times and, as a result, the energy loss of the switching operation becomes also reduced by 50%. Several key device parameters of the proposed TED-MOS with the FRL are summarized in Table I. Hitachi actually claims that the simultaneous realization of low loss and high reliability of this new TED-MOS can better meet the stringent requirements of various converter systems for EVs. Hitachi intends to put the device into practical use very soon and it will also be applied in other types of electric transducers within societal infrastructure systems, not only for EVs, and its use will contribute to the prevention of global warming and to the realization of a low-carbon society.

Table 1. Key parameters of the proposed TED-MOS with FRL

Parameter	Value	Unit	Conditions
V_{th}	3.7 (2.7)	V	T = 25°C (175°C), I_D = 80 mA, V_{DS} = 10 V
$R_{DS(on)}$	83 (V_{gs} = 15 V) 72 (V_{gs} = 18 V) 66 (V_{gs} = 20 V)	mΩ	T = 25°C, I_D = 80 A
V_{BD}	1,620	V	T = 25°C, I_D = 100 μA, V_{GS} = 0 V
C_{rss}	33	pF	f_{ac} = 100 kHz, V_{ac} = 250 mV,
C_{iss}	4,640	pF	V_{DS} = 30 V, V_{GS} = 0 V
C_{oss}	920	pF	

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References

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[2] T. Suto et al., Euro. Conf. SiC Related Mater. (ECSCRM 2018), TU.02a.03, 2018.