

# A 1.42-mm<sup>2</sup> 0.45–0.49 THz Monostatic FMCW Radar Transceiver in 90-nm SiGe BiCMOS

Christoph Mangiavillano , Alexander Kaineder , Klaus Aufinger , *Member, IEEE*,  
and Andreas Stelzer , *Member, IEEE*

**Abstract**—Terahertz frequency-modulated continuous-wave (FMCW) radars operating close to and beyond  $f_{\max}$  often use gain-enhancing lenses to improve the signal-to-noise ratio. A compact single-chip transceiver benefits a lot from the alignment of the lens to the single on-chip antenna in a monostatic system. The typically required coupler for monostatic operation adds an insertion loss. The proposed multiply-by-24 frequency multiplier-based FMCW radar transceiver removes the coupler and integrates both the final 0.48-THz doubler and subharmonic downconverter into a single common collector push–push doubler. The common emitter is the only port at 0.48 THz in this monostatic system, feeding the top-metal on-chip patch antenna using a direct via stack. The 1.42-mm<sup>2</sup> monostatic FMCW radar transceiver, manufactured in a 90-nm SiGe bipolar CMOS (BiCMOS) technology with an  $f_T/f_{\max}$  of 300/480 GHz consumes 85 mA when connected to a 3.3-V supply. At 0.48 THz, the output power is –12 dBm and the single-sideband noise figure is measured as 36.3 dB. FMCW radar measurements with operating bandwidths of up to 55 GHz, corresponding to a theoretical range resolution of 2.73 mm are performed using an on-board frequency source of a credit card sized demonstrator.

**Index Terms**—Frequency-modulated continuous-wave (FMCW) radar, mixer, multiplier, on-chip antenna, SiGe bipolar CMOS (BiCMOS), terahertz (THz).

## I. INTRODUCTION

WHEN moving toward the terahertz (THz) region, radars will benefit from the large achievable bandwidths, leading to range resolutions in the millimeter and submillimeter range. Silicon-integrated technologies such as CMOS and SiGe bipolar CMOS (BiCMOS) are outlined [1] as a low-cost solution for mass-market THz systems that require large integration levels, which is further supported by an approximate tripling in

the number of yearly silicon-based THz publications listed on IEEE Xplore during the past decade [2]. Current research has been able to maximize the  $f_T/f_{\max}$  of CMOS technologies [3] to around 0.3/0.45 THz and SiGe BiCMOS [4] to 0.3/0.5 THz with individual SiGe HBTs achieving  $f_T/f_{\max}$  of 0.505/0.72 THz [5].

Frequency-modulated continuous-wave (FMCW) radar operation at 0.48 THz, close to the  $f_{\max}$  of current silicon-integrated technologies is limited by the achievable output powers and receiver noise figures. The output signal is typically generated using push–push doublers [6], as power amplifiers are not feasible at frequencies of 0.48 THz. Similarly, the receive mixer [7] operates at a subharmonic local oscillator (LO) frequency where larger driving amplitudes are achievable.

THz radar operation has been recently presented using vector network analyzer (VNA) measurements with the relevant frequency extender modules at 0.85–1.1 THz [8] and at 1.1–1.5 THz [9]. Above 0.4 THz, split-block radars have been realized at 0.58 [10] and 0.675 THz [11] using GaAs Schottky-diode multipliers, with system sizes similar to the VNA extender modules.

Compound semiconductors such as indium phosphide HEMTs are able to achieve power amplification at 1 THz [12] with  $f_T/f_{\max}$  of 0.61/1.5 THz and individual transmitter and receiver circuits are demonstrated at 0.85 THz [13] but lack the integration levels and mass-market opportunities of silicon-integrated technologies. Metamorphic high-electron-mobility transistors with  $f_T/f_{\max}$  exceeding 0.5 and 1 THz, respectively, have enabled separate transmitter and receiver chips intended for radar operation at up to 0.44 THz [14] as well as a bistatic FMCW transceiver reaching 0.423 THz [15].

Methods to improve the transmit and receive performance of silicon-integrated single-chip THz FMCW radar transceivers operating close to  $f_{\max}$  have included the use of lenses in monostatic radars at 240 GHz [16], 270 GHz [17], and 0.32 THz [18]. Typically, monostatic designs are formed with a coupler before the antenna to achieve receive and transmit separation, which reduces the signal-to-noise ratio (SNR) by 3–5 dB, resulting from 3 dB due to power division and by an additional insertion loss of up to 2 dB. Furthermore, impedance mismatch at the interfaces of the four coupler ports at THz frequencies due to layout parasitics, device model discrepancies, and antenna mismatch can considerably reduce the transmit–receive isolation, limiting acceptable output powers.

A circularly polarized slot antenna is presented in a 270-GHz FMCW radar [17] to reduce the losses associated with the

Manuscript received 28 March 2022; revised 5 July 2022 and 17 August 2022; accepted 29 August 2022. Date of publication 20 September 2022; date of current version 7 November 2022. This work was supported in part by the European Commission’s ECSEL Joint Undertaking under Grant 737454 - project TARANTO, in part by the Austrian Research Promotion Agency (FFG), and in part by the Joint JKU-LIT-SAL mmWave Lab funded by Silicon Austria Labs (SAL) and Johannes Kepler University (JKU). (*Corresponding author: Christoph Mangiavillano.*)

Christoph Mangiavillano, Alexander Kaineder, and Andreas Stelzer are with the Institute for Communications Engineering and RF-Systems, Johannes Kepler University Linz, 4040 Linz, Austria (e-mail: christoph.mangiavillano@jku.at; alexander.kaineder@jku.at; andreas.stelzer@jku.at).

Klaus Aufinger is with the Infineon Technologies AG, 85579 Neubiberg, Germany (e-mail: Klaus.Aufinger@infineon.com).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TTHZ.2022.3208069>.

Digital Object Identifier 10.1109/TTHZ.2022.3208069

coupler to the insertion losses of the 90°-hybrids and the antenna feeding network. Lately, several solutions have been proposed for monostatic operation without the use of a coupler, similar to the “blow-through mixer” concept employed in the 77-GHz long range radar [19]. In [20] and [21], a diode-connected transistor is located between the 157-GHz oscillator and the on-chip antenna. Similarly, in [22], a common base buffer stage is placed after the 240-GHz oscillator. In the FMCW frequency-comb radar, operating at up to 0.32 THz [18], the square-law mixer input and final doubler output are connected together to the on-chip antenna. Alternatively, a power-combined on-chip antenna is proposed in [23] with separate transmit and receive ports for a 0.31-THz orbital-angular-momentum wave transceiver.

In this work, a monostatic 0.48-THz FMCW radar transceiver is presented, manufactured in a 90-nm SiGe BiCMOS technology with  $f_T/f_{\max}$  of 300/480 GHz. 0.48 THz was chosen as a design frequency by simply doubling the frequency of the previous ISM-band 240-GHz transceiver’s [24] frequency source to remain compatible with the demonstrator platform. Moreover, it is worth mentioning that the atmospheric attenuation demonstrates a local minimum around 0.48 THz [25], relevant for future long-range applications. The proposed 0.48-THz common collector push–push doubler, located at the final stage of the multiply-by-24 frequency multiplier chain also functions as a subharmonic receive mixer, comparable to the combined doubler and subharmonic mixing device demonstrated in a 240-GHz split-block radar using Schottky diodes [26], removing the need for an impedance-sensitive coupler and an additional downconversion mixer circuit. Furthermore, the proposed design only requires a single 0.48-THz connection and is placed directly below the antenna feeding edge. In comparison, four 0.48-THz interfaces are necessary in a coupler-based monostatic system, while at least two 0.48-THz interfaces are used for the previously mentioned state-of-the-art coupler-free solutions.

In Section II, the implemented architecture is discussed, while in Section III, the individual circuits are presented. Section IV illustrates the characterized transceiver transmit and receive performance as well as FMCW radar measurements. Finally, Section V concludes this article.

## II. TRANSCEIVER DESIGN: SYSTEM ARCHITECTURE

The radar SNR is given as

$$\text{SNR} = \frac{P_T G^2 \lambda^2 \sigma}{(4\pi)^3 R^4 k_B T_0 B F_N L} \quad (1)$$

with transmit power  $P_T$ , antenna gain  $G$ , which is identical in the receive and transmit direction for monostatic systems and assumed equal in bistatic systems, wavelength  $\lambda$ , target radar cross section  $\sigma$ , target distance  $R$ , Boltzmann constant  $k_B$ , temperature  $T_0$ , noise bandwidth  $B$ , noise figure  $F_N$ , and loss  $L$ . When doubling the frequency of our previous 240-GHz radar [24] to 0.48-THz operation, from (1) and using the same trihedral corner reflector target and the same  $B$ , the overall SNR would remain constant, as the radar cross section is proportional to  $1/\lambda^2$ . This assumes that all other parameters, including  $P_T$ ,  $G$ , and  $F_N$ , remain unchanged at 0.48 THz. Typical output powers at 0.48 THz

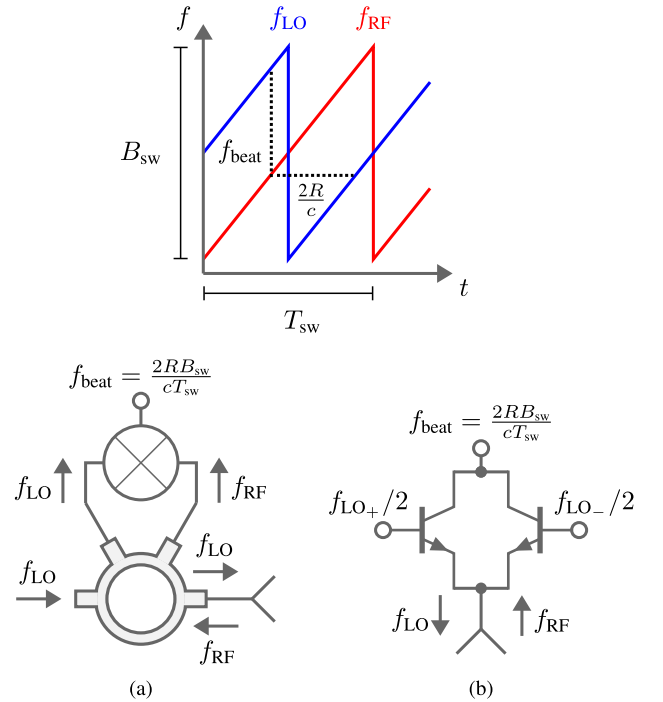


Fig. 1. Comparison of (a) conventional silicon-integrated monostatic FMCW transceiver with fundamental rat-race coupler and (b) proposed coupler-free integrated FMCW transceiver with subharmonic receiver doubler.

only reach 0 dBm [6] with the cost of extensive power combination of four power-combined quadrature push–push doublers or equivalently  $-8.5$  dBm from a single doubler, considering 6 dB due to four-way power combining, another 3 dB from quadrature operation, and 0.5 dB insertion losses, compared to 7.2 dBm at 240 GHz with a single push–push doubler [27]. Moreover, downconversion mixer noise figures are 33 dB [7] at 0.48 THz, typically 10–15 dB higher than counterparts at 240 GHz [28], [29]. On the other hand, a given on-chip antenna, constrained by a fixed size, frequently implemented as a patch antenna [16], [24] using the metal stack for top-side radiation, will see an increase in gain from the frequency increase from 240 GHz to 0.48 THz. For the aforementioned state-of-the-art transmitter and receiver parameters, the SNR is 20 dB lower at 0.48 THz, compared to 240 GHz, assuming identical  $G$  at both frequencies and the same trihedral corner reflector target. This difference increases to 28.5 dB if only a single push–push doubler is considered at 0.48 THz. Monostatic single-chip transceiver architectures benefit from the alignment of external gain-enhancing lenses to the single common antenna, allowing for significant SNR improvements as demonstrated by the  $G^2$  term in (1).  $G$  can be increased by typically 15–20 dB using external lenses as reported at 0.32 THz in a monostatic radar [18] or using separate transmitter and receiver chips [30] and even 35 dB as described in the 240-GHz monostatic radar [16]. The conventional silicon-integrated monostatic FMCW radar architecture, illustrated in Fig. 1(a), involves a coupler to separate the fundamental-frequency transmitter and receiver signals before the common single antenna. This topology will introduce a combined loss of 8 dB, with an expected 3-dB loss due to power

TABLE I  
SILICON-INTEGRATED FMCW RADAR TOPOLOGY COMPARISON AT 0.48 THZ

Topology	$L$ (dB)	0.48-THz interfaces	Additional area (mm <sup>2</sup> )	Additional $P_{dc}$ (mW)
Bistatic 2-chip	–	2	$A_{LO-generation} + A_{Mixer} + A_{Antenna}$	$P_{LO-generation} + P_{Mixer}$
Bistatic 1-chip	–	2	$A_{LO-split} + A_{Mixer} + A_{Antenna}$	$P_{LO-split} + P_{Mixer}$
Monostatic coupler	8	4	$A_{Coupler} + A_{Mixer}$	$P_{Mixer}$
Circularly polarized antenna	2	4	$A_{Hybrid} + A_{Mixer}$	$P_{Mixer}$
Blow-through mixer	1	2	$A_{Mixer}$	$P_{Diode}$
Antenna sharing	–	2	$A_{Mixer}$	–
Power-combined antenna	4	2	$A_{Mixer}$	–
Proposed $\times 2$ /subharmonic mixer	–	1	–	–

division and at least 1 dB of additional loss in both the coupler’s transmitter and receiver paths. The coupler requires some additional area and driving the mixer with sufficient LO-amplitude through the coupler may become difficult at 0.48 THz. In this work, a combined subharmonic receiver and doubler device is proposed, consisting of a common collector push–push doubler, as shown in Fig. 1(b). The operating principle is comparable to the conventional fundamental FMCW radar, with the beat frequency  $f_{beat}$  given as

$$f_{beat} = \frac{2RB_{sw}}{cT_{sw}} \quad (2)$$

dependent on the transmitted LO bandwidth  $B_{sw}$ , ramp duration  $T_{sw}$ , and target distance  $R$ . The proposed design effectively shares both the last frequency doubler and the subharmonic downconverter circuit in a single common collector push–push doubler. Both the doubled subharmonic LO signal and the target-reflected radio frequency (RF) signal are present at the common emitter, with the base–emitter junctions of the two transistors performing the mixing process. The summation of the collector currents generated by the differential subharmonic LO signal suppresses the odd-valued LO-mixing terms as well as the subharmonic LO-signal, detailed in the analysis in Section III-D.

To evaluate the individual transceiver architectures, Table I is presented. The bistatic 2-chip solution, as demonstrated in a 0.32-THz FMCW radar [30], benefits from excellent transmitter–receiver isolation, although roughly twice the area and dc power consumption  $P_{dc}$  is required. In the circularly polarized system at 270 GHz [17], the losses of around 2 dB are estimated from the insertion losses expected of the 90°-hybrids and the antenna feed network. The losses in a monostatic “blow-through mixer” system are reduced to less than 1 dB at 157 GHz [21] with the additional benefit of removing the coupler, although no measurement of the insertion losses has been performed at higher frequencies. Antenna sharing, implemented by connecting transmitter and a zero dc-power square-law mixer to the same antenna port in [18] or as a power-combined antenna in [23], is a further option for removing the coupler in monostatic designs; however, both still require two interfaces to be matched at 0.48 THz and insertion losses are expected from power-combined antennas. The common base topology from [22] would require a technology offering gain close to 0.48 THz. The proposed design, consisting of a push–push doubler with integrated subharmonic downconversion capability

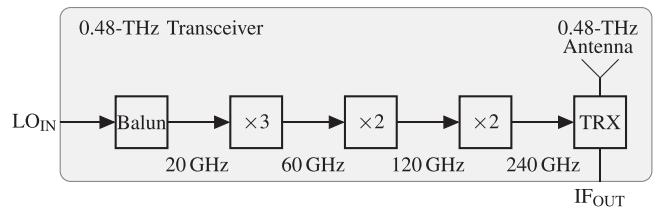


Fig. 2. 0.48-THz transceiver block diagram consisting of a multiply-by-24 frequency multiplier chain, with the last doubler stage at 0.48 THz, labeled TRX, also functioning as a subharmonic receiver.

requires only a single 0.48-THz circuit interface to the antenna and offers the lowest area and power consumption.

### III. TRANSCEIVER DESIGN: CIRCUIT IMPLEMENTATION

Fig. 2 displays the block diagram of the implemented 0.48-THz FMCW transceiver. The transceiver consists of an  $LC$  balun which interfaces the single-ended external 20-GHz LO signal with the differential 60-GHz frequency tripler. A set of two cascaded bootstrapped Gilbert-cell frequency doublers are employed to achieve a 240-GHz signal. The final block, labeled TRX, consists of the 0.48-THz integrated subharmonic receiver doubler, which directly connects to the on-chip antenna. In this section, the implemented circuits will be described, ordered by ascending frequency.

#### A. 20-GHz $LC$ Balun

Fig. 3(a) illustrates the implemented  $LC$  balun schematic. Metal insulator metal (MIM) capacitors  $C_{MIM}$  of around 500 fF are used for dc blocking. The input impedance is 50  $\Omega$ , whilst the balanced output impedance is chosen as 100  $\Omega$ . The inductance  $L = 563$  pH and capacitance  $C = 113$  fF have been calculated using [31]. The simulated S-parameters are presented in Fig. 3(b) for the  $LC$  balun. The simulated phase imbalance is approximately 9° around the intended design frequency of 20 GHz. The spiral inductors with approximately four turns are generated using the Keysight ADS coilsys tool and simulated with the finite element method.

#### B. 60-GHz Frequency Tripler

Fig. 4 demonstrates the schematic diagram of the 20-to-60-GHz frequency tripler. Transistors Q1–Q4 are biased at the maximum  $f_T$  collector current of around 8.4 mA. The biasing

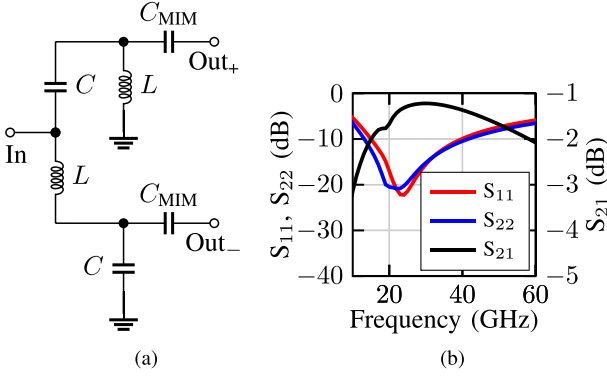


Fig. 3. 20-GHz LC balun (a) schematic diagram and (b) simulated S-parameters with output connected to a differential port.

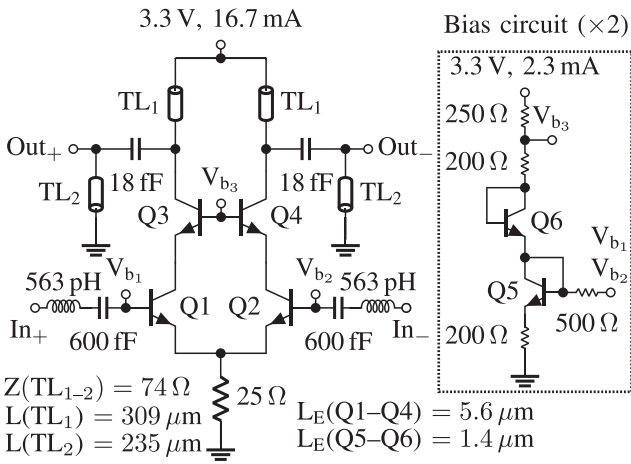


Fig. 4. 20-to-60-GHz frequency tripler schematic.

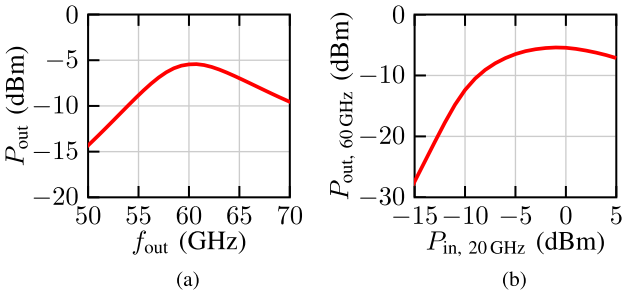


Fig. 5. Frequency tripler simulated: (a) third harmonic output power versus third-harmonic frequency and (b) third-harmonic output power versus 20-GHz input power.

circuit, employed in all preceding designs, has been placed on either sides of the differential frequency tripler circuit, achieving a highly symmetrical layout. Furthermore, this technique allows for the creation of half-circuits, halving the overall layout effort. Fig. 5(a) shows the simulated frequency behavior of the frequency tripler at the third harmonic with a fundamental input power  $P_{\text{in}}$  of 0 dBm. A maximum output power  $P_{\text{out}}$  of around  $-6$  dBm has been simulated at an output frequency  $f_{\text{out}}$  of 60 GHz. In Fig. 5(b), the simulated input–output power characteristic is depicted for a 20-GHz input.

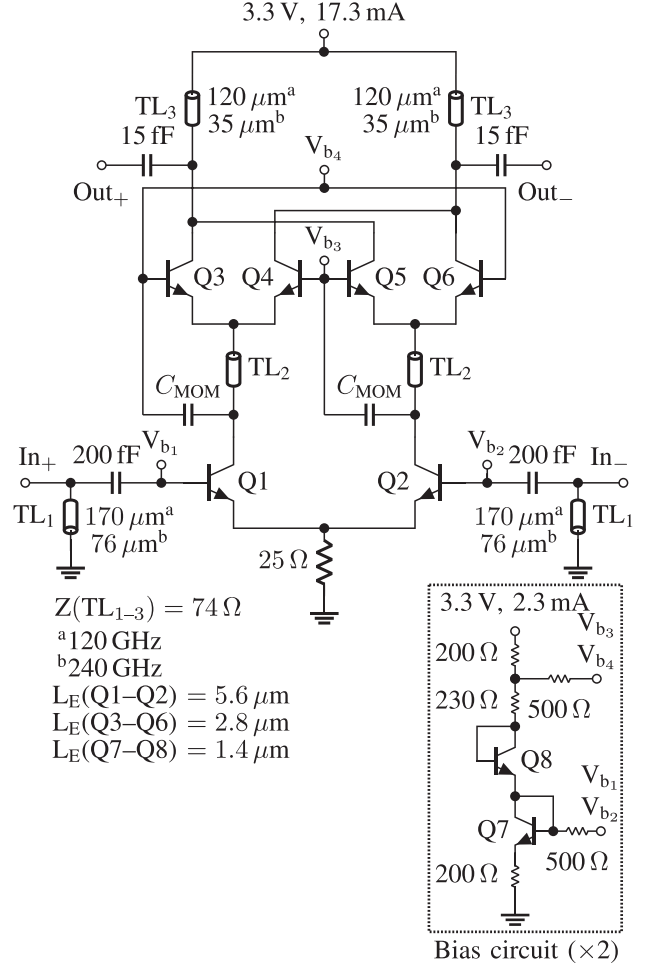


Fig. 6. 120- and 240-GHz frequency doubler schematic.

### C. 120- and 240-GHz Frequency Doublers

Fig. 6 introduces the schematic diagram of the 60-to-120-GHz and 120-to-240-GHz frequency doublers. The topology was first described in [32] as a bootstrapped Gilbert cell frequency doubler. Transmission lines TL<sub>2</sub> are quarter wavelength long, resulting in lengths of 312 and 156  $\mu\text{m}$  at the 120- and 240-GHz frequency doublers, respectively. Transistors Q1–Q6 are biased near the maximum  $f_T$  collector current, at around 8.6 mA. Furthermore, 50-fF interdigitated metal-oxide-metal (MOM) capacitors have been designed to improve the coupling between the collectors of Q1 and Q2 to the bases of Q3, Q6 and Q4, Q5. The use of MOM capacitors located in the bottom four thin-metal layers removes the necessity of traveling up to the MIM capacitor, located between the topmost thick-metal layers, and back down to the transistor, using hard-to-model via stacks.

Fig. 7 depicts both the simulated (a) output power of the second harmonic relative to output frequency and (b) the input–output power characteristic of the 120-GHz frequency doubler. The 120-GHz frequency doubler is able to reach a 5-dBm output power at an input power as low as  $-10$  dBm, which fits very well with the  $-6$  dBm output power of the preceding 60-GHz frequency tripler. Similarly, in Fig. 7, the simulated (c) output

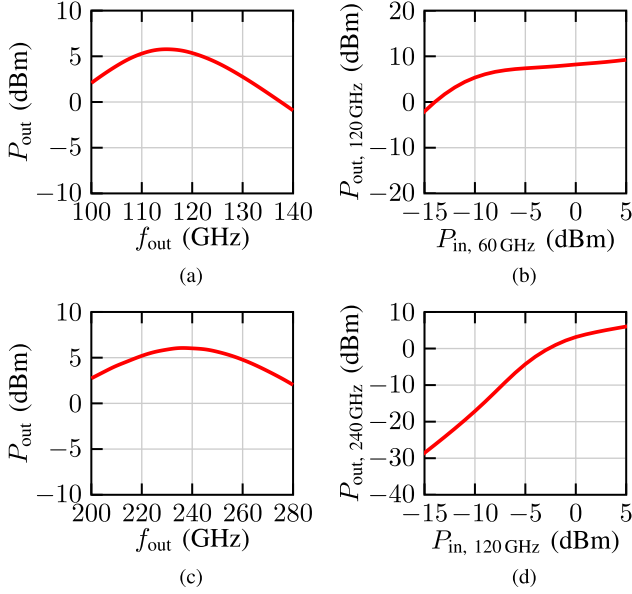


Fig. 7. Simulation of 60-to-120-GHz frequency doubler (a) output power versus input power ( $P_{in} = -10$  dBm) and (b) second-harmonic output power versus input power. Simulation of 120-to-240-GHz frequency doubler (c) output power versus frequency ( $P_{in} = 5$  dBm) and (d) second-harmonic output power versus input power.

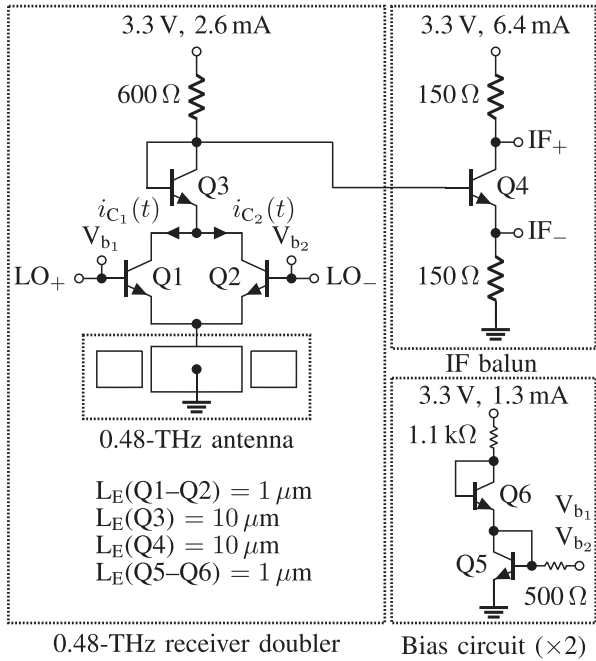


Fig. 8. Integrated 0.48-THz subharmonic receiver doubler schematic.

power of the second harmonic versus output frequency and (d) the input–output power characteristic of the 240-GHz frequency doubler are shown.

#### D. Integrated 0.48-THz Subharmonic Receiver Doubler

The proposed 0.48-THz subharmonic receiver doubler is depicted in Fig. 8. This circuit, consisting of a common collector

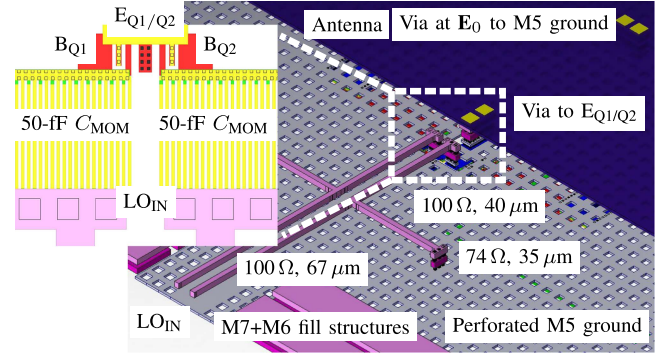


Fig. 9. Integrated 0.48-THz subharmonic receiver doubler layout demonstrating LO input matching network and direct feeding from emitters of Q1 and Q2 located below the antenna.

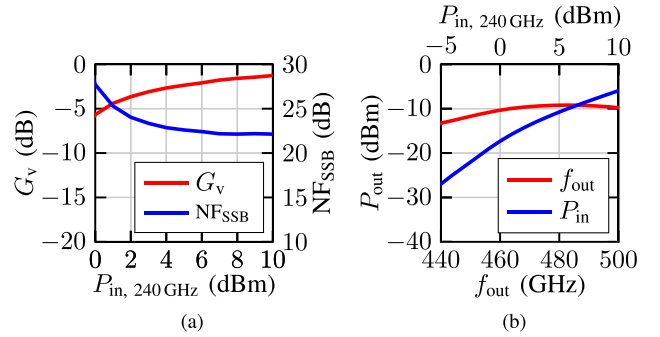


Fig. 10. Simulation of (a) 0.48-THz subharmonic receiver doubler voltage conversion gain and single-sideband noise figure versus subharmonic input power at an IF frequency of 10 MHz and (b) 20-to-480-GHz frequency multiplier output power versus output frequency and 0.48-THz subharmonic receiver doubler output power versus 240-GHz input power.

push–push doubler, as presented in [27] and [33], has been enhanced to also work as a receiver, similar to the stand-alone 44-GHz subharmonic mixer in [34]. The emitters of Q1 and Q2, placed underneath the antenna, form a single direct connection to the 0.48 THz on-chip antenna, reducing the required inter-connection at 0.48 THz to a via stack, as illustrated in Fig. 9. The collector current can be represented as

$$i_C(t) = I_{se} \frac{v_{be}(t)}{V_T} \quad (3)$$

where  $I_S$  is the saturation current,  $V_T \approx 26$  mV at room temperature, and  $v_{be}(t)$  is given as

$$v_{be}(t) = V_{be} + V_{RF} \cos(\omega_{RF}t) + V_{LO} \cos(\omega_{LO}t) \quad (4)$$

with dc base–emitter voltage  $V_{be}$ , RF amplitude  $V_{RF}$ , RF angular frequency  $\omega_{RF}$ , LO amplitude  $V_{LO}$ , and LO angular frequency  $\omega_{LO}$ . Thus

$$i_C(t) = I_{se} \frac{V_{be}}{V_T} e^{\frac{V_{LO} \cos(\omega_{LO}t)}{V_T}} \left( 1 + \frac{V_{RF}}{V_T} \cos(\omega_{RF}t) \right) \quad (5)$$

using the approximation  $e^x \approx 1 + x$  for the RF small signal. We now consider that Q1 will be excited by a positive LO signal, while Q2 will be excited by a negative LO signal, when Q1 and

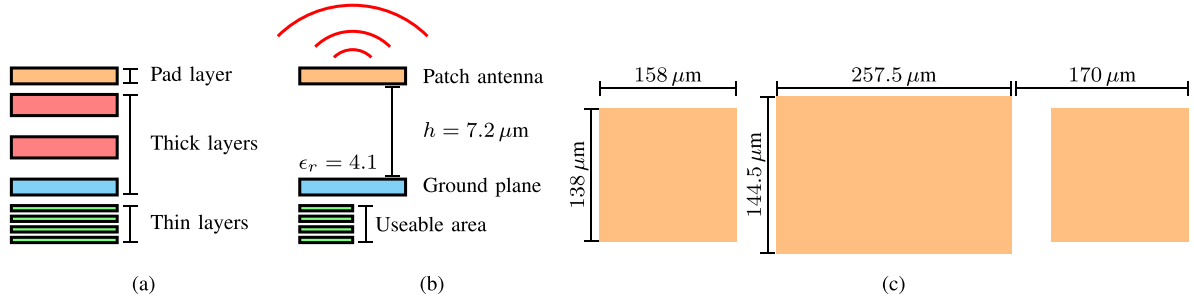


Fig. 11. (a) Technology metal stack, (b) area reuse concept, and (c) patch antenna with parasitic patches (not to scale).

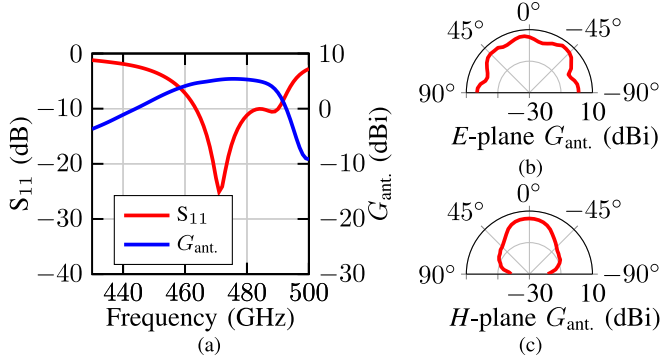


Fig. 12. On-chip antenna simulation of (a)  $S_{11}$  and realized gain versus frequency, (b)  $E$ -plane, and (c)  $H$ -plane of realized gain at 0.48 THz.

$Q_2$  are driven differentially; thus

$$i_{C_1}(t) = I_S e^{\frac{V_{bc}}{V_T}} e^{\frac{V_{LO} \cos(\omega_{LO} t)}{V_T}} \left( 1 + \frac{V_{RF}}{V_T} \cos(\omega_{RF} t) \right) \quad (6)$$

and

$$i_{C_2}(t) = I_S e^{\frac{V_{bc}}{V_T}} e^{\frac{-V_{LO} \cos(\omega_{LO} t)}{V_T}} \left( 1 + \frac{V_{RF}}{V_T} \cos(\omega_{RF} t) \right). \quad (7)$$

From [35, (9.6.34)], it is possible to rewrite the exponential term with the cosine LO-signal as a series of modified Bessel functions of the first kind, with  $z = V_{LO}/V_T$

$$\begin{aligned} i_{C_1}(t) = & I_S e^{\frac{V_{bc}}{V_T}} \left( I_0(z) + 2I_1(z) \cos(\omega_{LO} t) \right. \\ & + 2I_2(z) \cos(2\omega_{LO} t) + 2I_3(z) \cos(3\omega_{LO} t) \\ & \left. + 2I_4(z) \cos(4\omega_{LO} t) \cdots \right) \cdot \left( 1 + \frac{V_{RF}}{V_T} \cos(\omega_{RF} t) \right). \quad (8) \end{aligned}$$

Using [35, (9.6.34, 9.6.38)]  $i_{C_2}(t)$  becomes

$$\begin{aligned} i_{C_2}(t) = & I_S e^{\frac{V_{bc}}{V_T}} \left( I_0(z) - 2I_1(z) \cos(\omega_{LO} t) \right. \\ & + 2I_2(z) \cos(2\omega_{LO} t) - 2I_3(z) \cos(3\omega_{LO} t) \\ & \left. + 2I_4(z) \cos(4\omega_{LO} t) \cdots \right) \cdot \left( 1 + \frac{V_{RF}}{V_T} \cos(\omega_{RF} t) \right). \quad (9) \end{aligned}$$

Once the currents  $i_{C_1}(t)$  and  $i_{C_2}(t)$  are summed, the odd-valued LO-terms in the modified Bessel series cancel out and the even

terms are doubled. Therefore

$$\begin{aligned} i_{C_1}(t) + i_{C_2}(t) = & 2I_S e^{\frac{V_{bc}}{V_T}} \left( I_0(z) + I_0(z) \frac{V_{RF}}{V_T} \cos(\omega_{RF} t) \right. \\ & \left. + 2I_2(z) \cos(2\omega_{LO} t) + I_2(z) \frac{V_{RF}}{V_T} \cos((2\omega_{LO} \pm \omega_{RF})t) \right) \quad (10) \end{aligned}$$

up to the second order, where the cosine product identity has been employed to rewrite the multiplication of the LO and RF cosine functions. In (10), the desired subharmonic mixing product  $2\omega_{LO} \pm \omega_{RF}$  is visible as well as the suppression of the fundamental LO signal. In Fig. 10(a), the simulated voltage conversion gain (CG)  $G_v$  and single-sideband noise figure  $NF_{SSB}$  are illustrated for subharmonic LO input powers between 0 and 10 dBm. The voltage CG and single-sideband noise figure have been simulated with the output power profile of Fig. 7(c). Between 430 and 500 GHz,  $G_v$  varies by less than 0.2 dB, with a peak value of  $-2.2$  dB at around 467 GHz.  $NF_{SSB}$  varies only by 0.7 dB between 430 and 500 GHz, with a minimum of 22.2 dB at around 430 GHz. The simulated input-referred 1-dB compression point of the receiver occurs at an input RF power of  $-5$  dBm at 0.48 THz. The input referred third-order intercept point was simulated to be around 4.5 dBm at 0.48 THz. Fig. 10(b) demonstrates the simulated 20-to-480-GHz multiplier chain output power relative to output frequency as well as the 480-GHz doubler output power versus the 240-GHz input power. A simulated wideband response of at least  $-10$  dBm output power can be achieved in the range of 465–500 GHz. As the output power is lower than the input-referred 1-dB compression point, reflected signals due to antenna mismatch will not affect the receiver. Simulations reveal that the  $S_{11}$  of the RF port is below  $-10$  dB from 390 to 560 GHz, achieved using a current matching scheme at the emitters of  $Q_1$  and  $Q_2$ .

### E. 0.48-THz on-Chip Antenna

In Fig. 11(a), the metal stack is presented. The patch antenna is formed using the top-most pad layer and uses a medium-thick metal 5 ground plane, as illustrated in Fig. 11(b). The ratio of substrate height to resonant wavelength is doubled compared to previous designs at 240 GHz [24], which directly improves the achievable gain and bandwidth. The dimensions of the proposed parasitic patch antenna are represented in Fig. 11(c). CST Studio

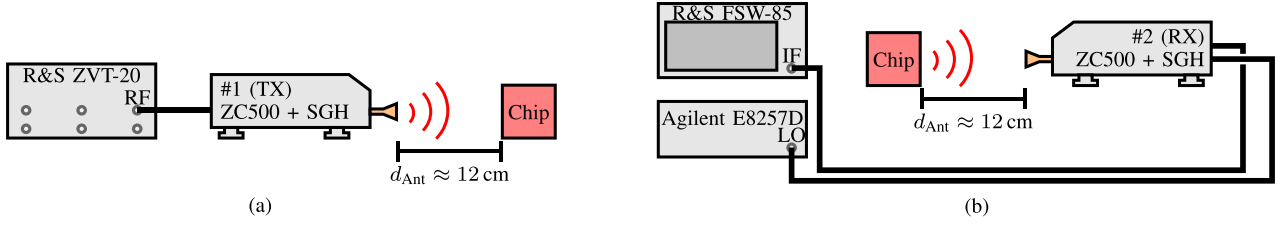


Fig. 13. Illustration of (a) 0.48-THz transceiver-receiver gain measurement and (b) 0.48-THz transceiver EIRP measurement with 26-dBi standard gain horn (SGH) antenna. The wire-bonded transceiver, labeled chip, is connected to a R&S SMBV100A external LO source (not drawn).

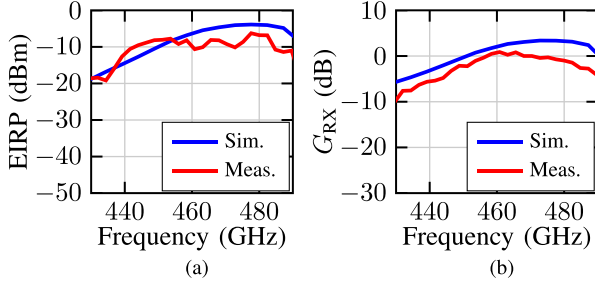


Fig. 14. Measurement and simulation without lens of (a) EIRP and (b) receiver conversion gain of the 0.48-THz transceiver versus frequency.

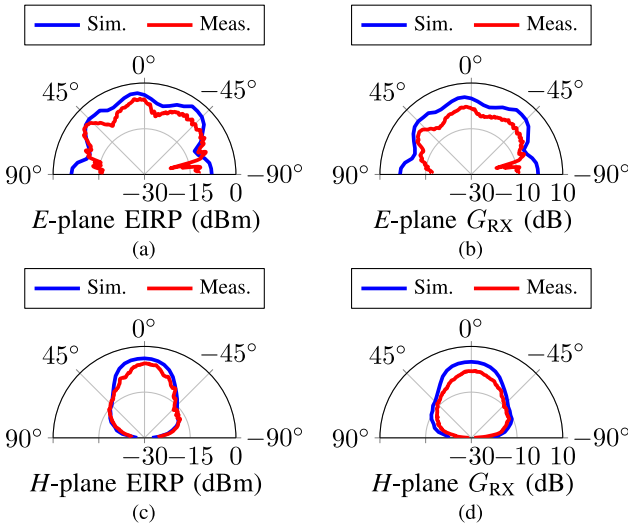


Fig. 15. Measurement and simulation without lens of (a)  $E$ -plane of EIRP, (b)  $E$ -plane of receiver gain, (c)  $H$ -plane of EIRP, and (d)  $H$ -plane of receiver gain at  $f_{RF} = 0.48$  THz and  $f_{IF} = 10$  MHz.

Suite from Dassault Systèmes is used to create a fully parameterizable antenna cell. A particle swarm optimization has been implemented to determine antenna dimensions of the main and parasitic patches, while keeping the separation at a minimum of 12  $\mu\text{m}$ . The layers below metal 5 are free to be used for other purposes, and, thus, the antenna can effectively share its area with other circuitry. Examples may include simple biasing blocks or small digital or analog circuitry which are able to cope with using the bottom four metal layers only. In this design,

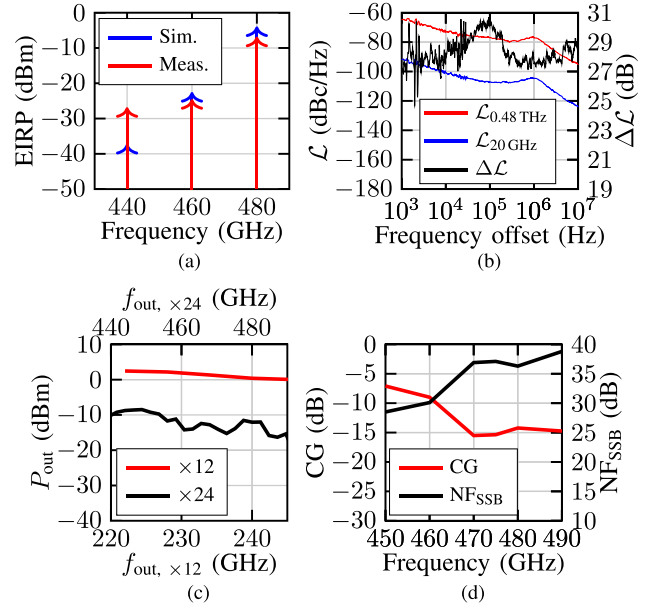


Fig. 16. Measurement of (a) EIRP without lens of multiplied harmonic content with 20-GHz LO input and (b) phase noise measurement of 20-GHz APSIN26G source, 20-GHz APSIN26G source multiplied to 0.48 THz and resulting phase noise translation ( $\Delta\mathcal{L}$ ), (c) multiply-by-12 and multiply-by-24 output power, and (d) receiver gain and noise figure with single-ended IF (50  $\Omega$ ) at  $f_{IF} = 37$  MHz using gain method from [37].

the implemented 0.48-THz subharmonic receiver doubler sits exactly below the wider edge of the antenna, as shown in Fig. 9. Fig. 12(a) depicts the simulated input matching and the realized gain  $G_{ant}$  frequency dependence of the implemented patch antenna. A  $-10$  dB input matching bandwidth has been simulated between 465 and 490 GHz. The 3-dB realized gain bandwidth is approximately from 457 to 489 GHz, with a peak realized gain of 5.4 dBi at 477 GHz. In Fig. 12(b) and (c), the simulated  $E$ -plane and  $H$ -plane of the antenna realized gain is depicted for a frequency of 0.48 THz.

#### IV. MEASUREMENT RESULTS

In the first part, over-the-air measurements of the 0.48-THz transceiver chip, obtained using an optical bench setup, are presented. In the second part, the 0.48-THz transceiver is applied in an FMCW radar measurement.

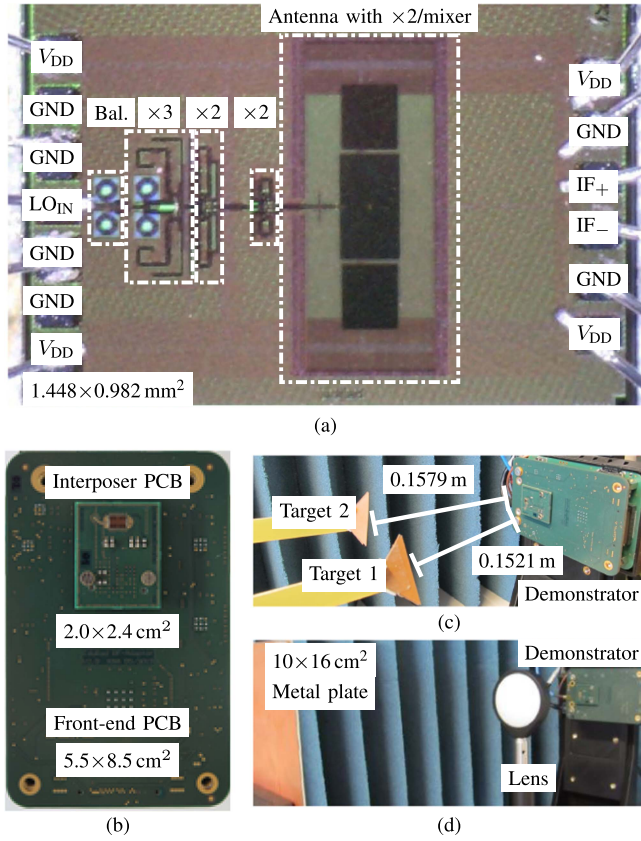


Fig. 17. Photograph of (a) wire-bonded 0.48-THz FMCW transceiver chip, (b) wire-bonded 0.48-THz FMCW transceiver chip mounted on demonstrator front-end PCB using interposer, (c) FMCW radar measurement of two 2.1-cm corner reflector targets at 0.1521 and 0.1579 m, and (d) FMCW radar measurement of 10×16 cm<sup>2</sup> metal plate with Thorlabs LAT100 lens.

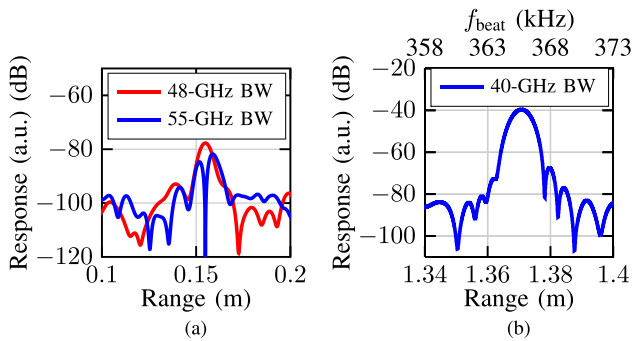


Fig. 18. FMCW radar measurement with (a) minimum four-sample Blackman–Harris–windowed response of two 2.1-cm corner reflectors positioned at 0.1521 and 0.1579 m without lens and with averaging, and (b) Hanning-windowed response of 16×10 cm<sup>2</sup> metal plate at 1.37 m with Thorlabs LAT100 lens and without averaging.

### A. Transceiver Characterization

A diagram of the measurement procedure is shown in Fig. 13. First, one of the R&S ZC500 frequency converters is characterized using an Erickson PM4 for output power over frequency. A R&S ZVT-20 is used to generate the RF signal for the converter. In the second step, the second R&S ZC500 frequency converter is characterized for receiver CG using the aforementioned characterized converter as the RF input. An Agilent E8257D

is utilized as the LO signal for the R&S ZC500 frequency converter in receiver mode with the IF output connected to the R&S FSW-85 signal analyzer. In Fig. 13(a), the measurement setup is demonstrated for receiver gain characterization of the transceiver chip, using the characterized converter as a transmitter. Finally, in Fig. 13(b), it is possible to observe the effective isotropic radiated power (EIRP) characterization setup of the transceiver chip using the characterized converter as a receiver. For *E*-plane and *H*-plane measurements of the EIRP and receiver CG, the transceiver is mounted on a turntable.

The measured and simulated EIRP and receiver gain  $G_{RX}$  are depicted over frequency in Fig. 14(a) and (b), respectively. In Fig. 15(a) and (c), the measured and simulated *E*-plane and *H*-plane of the EIRP are illustrated, while in Fig. 15(b) and (d), the measured and simulated *E*-plane and *H*-plane of the receiver gain are shown. Fig. 16(a) illustrates the harmonic content close to the 480-GHz main carrier. At 440 GHz, the measurement indicates a 10-dB higher harmonic content. In a similar method to Fig. 13(a) and using a R&S ZC330 as the source, the CG at 240 GHz was measured to be 35 dB below the CG at 480 GHz, without lens. Additionally, the radiated fundamental 240-GHz signal was measured using a RPG ZRX330 in a similar setup to Fig. 13(b), revealing an EIRP of −45 dBm without lens, 37 dB below the 480-GHz signal. Thus, considering both transmitter and receiver, an attenuation of 72 dB is achieved for the unwanted 240-GHz signal relative to the desired 0.48-THz signal. In Fig. 16(b), the measured phase noise translation  $\Delta\mathcal{L}$  was investigated using the EIRP setup from Fig. 13(b). First, the 20-GHz signal from a APSIN26G source was directly connected to the R&S FSW-85. In a second measurement, the downconverted IF signal from the receiving R&S ZC500, transmitted by the transceiver-multiplied APSIN26G 20-GHz input signal, was connected to the R&S FSW-85.  $\Delta\mathcal{L}$  is theoretically given as  $20 \log_{10}(N = 24) = 27.6$  dB, compared to the measurement ranging from 24.5 to 30.5 dB between frequency offsets of 1 kHz and 10 MHz, expected from the circumstance of the two-step measurement. The  $NF_{SSB}$  and CG peak in Fig. 16(d) has shifted to around 450 GHz, in line with measurements in Fig. 16(c) that demonstrate that the 20-to-240-GHz frequency multiplier peak output power of 2.45 dBm is centered at 222 GHz and the 20-to-480-GHz frequency multiplier peak output power, calculated from the measured EIRP and simulated realized antenna gain, is −8.5 dBm at 450 GHz. The measured frequency shift and reduced output power of the 20-to-240-GHz frequency multiplier when compared to simulations in Fig. 7(c) can be used to explain the reduction of up to 5 dB in the measured EIRP and receiver gain in Fig. 14(a) and (b). The limited subharmonic output power driving the combined subharmonic receiver doubler will result in a simulated 3-dB lower CG when the 240-GHz input power is reduced from 6 to 0 dBm, as illustrated in Fig. 10(a). With a measured output power of 0.4 dBm at 240 GHz from Fig. 16(c), a simulated output power of only −16 dBm is expected at 0.48 THz, using Fig. 10(b). A power amplifier at 240 GHz [36] could be included in future designs after the 240-GHz doubler. Similarly, the measurement of Fig. 15 indicates typical deviations of 5 dB, although larger discrepancies of more than 10 dB can be observed between simulation and measurement in



TABLE II  
SILICON-INTEGRATED FMCW RADAR DEMONSTRATORS ABOVE 0.3 THZ

Technology	$f_T/f_{\max}/f_{RF}$ (GHz)	Topology	$P_{out}/P_{dc}$ (mW)	Area (mm <sup>2</sup> )	NF <sub>SSB</sub> (dB)	Reference
65-nm CMOS	-/280/220–320	Monostatic, antenna sharing	0.32/840	5	28	[18]
130-nm SiGe	300/350/311–338	Bistatic, 2-chip	0.32/2942	1.97	30.3	[30]
130-nm SiGe	230/-/367–382	Bistatic, 1-chip	0.04/380	4.18	35	[40]
90-nm SiGe	300/480/450–490	Monostatic, integrated doubler receiver	0.07/280	1.42	36.3	This work

the  $E$ -plane measurements, indicating a possible obstruction by bond wires or circuit board components close to  $90^\circ$  and  $-90^\circ$ .

### B. FMCW Radar Measurement

The photograph of the wire-bonded 0.48-THz transceiver is shown in Fig. 17(a). The transceiver is attached to an interposer printed circuit board (PCB) of  $2.0 \times 2.4$  cm<sup>2</sup>, which in turn is connected to the demonstrator front-end PCB with an area of  $5.5 \times 8.5$  cm<sup>2</sup>, as illustrated in Fig. 17(b). More details on the similar radar demonstrator can be found in our 240-GHz FMCW radar [24]. The FMCW radar measurement is depicted in Fig. 17(c). The radar demonstrator is set up on a linear rail and targets such as a metal plate can be moved. The first FMCW radar measurement in Fig. 18(a) investigates the range resolution using a similar setup to [18]. Averaging is performed to improve the SNR in this measurement, performed without a gain-enhancing lens. Two 2.1-cm trihedral corner reflectors are separated in range by 5.8 mm. Increasing the bandwidth (BW) from 48 to 55 GHz allows the two targets to be distinguished. A 48-GHz bandwidth should in theory result in a range resolution of 3.1 mm. The minimum four-sample Blackman–Harris window used in this measurement is able to suppress the sidelobe leakage of a box-car window at the cost of a 2.25 times wider  $-6$  dB mainlobe full-width [38]. Fig. 18(b) illustrates the measurement of a  $16 \times 10$  cm<sup>2</sup> metal plate target at 1.37 m, as depicted in Fig. 17(d), with a plano-convex LAT100 lens from Thorlabs, comparable to the setup found in [16] at 240 GHz. An external Keysight M8195A arbitrary waveform generator is used to generate a linear ramp from 18.75 to 20.42 GHz, resulting in a 40-GHz bandwidth with a ramp duration of 1 ms. In this measurement, no averaging is performed and the large metal plate, illuminated by the focused beam, acts like an electrical mirror, simplifying the SNR equation from (1) to a transmitted signal traveling  $2R$ , governed by the Friis transmission equation

$$\text{SNR} = \frac{P_T G^2 \lambda^2}{(4\pi)^2 (2R)^2 k_B T_0 B F_N}. \quad (11)$$

At 0.48 THz, a noise figure of 36.3 dB, a combined  $G$  of 22.2 dBi of the on-chip antenna and lens,  $P_T$  of  $-12$  dBm,  $T_0$  of 300 K,  $B$  of 1 kHz, related to the ramp duration of 1 ms when using a fast Fourier transform-based matched-filter approach, reveals an SNR of around 40 dB, agreeing with the measurement in Fig. 18(b). The range resolution of the measurement in Fig. 18(b) can be determined from the Rayleigh range resolution, as the distance from the peak to the first null [39]. The distance from the peak to the first null is around 8 mm in Fig. 18(b), and considering a widening factor of 2 by the Hanning window used for improved sidelobe suppression compared to the box-car

window [38], the estimated range resolution is very close to the theoretical range resolution of 3.75 mm.

In Table II, current state-of-the-art silicon-integrated FMCW radars have been summarized for operation frequencies above 0.3 THz. To the authors' best knowledge, the proposed 0.48-THz monostatic transceiver is the first demonstration of a silicon-integrated FMCW radar at frequencies above 0.4 THz, whilst also offering the lowest chip area and power consumption when compared to silicon-integrated FMCW radar transceivers above 0.3 THz.

### V. CONCLUSION

A 1.42-mm<sup>2</sup> FMCW radar transceiver operating at 0.48 THz was implemented in a 90-nm SiGe BiCMOS technology with  $f_T/f_{\max}$  of 300/480 GHz. A common collector push–push doubler generates the 0.48-THz signal at the common emitter port as well as performing subharmonic downconversion of the received signal at the same port. A monostatic system is formed, which removes the typically required lossy and impedance variation-sensitive coupler before the antenna. The proposed topology, placed below the feeding edge of the on-chip antenna, only requires a single 0.48-THz connection, with the separation minimized to the height of the via stack between the bottom-metal emitters of the 0.48-THz subharmonic receiver doubler and the top-metal antenna patch. The transceiver achieves a current consumption of 85 mA when connected to a 3.3-V supply. FMCW radar measurements are performed and reveal detection of targets such as corner reflectors and metal plates using the on-board frequency source of the credit card sized demonstrator or an external arbitrary waveform generator, respectively, at a bandwidth of up to 55 GHz. This work is an optimal candidate for a future terahertz frequency-comb radar [18] with submillimeter range resolution. The recent demonstration [41] of a power amplifier with more than 6 dBm of output power at 0.3 THz in a SiGe BiCMOS technology with  $f_T/f_{\max}$  of 470/650 GHz will further increase the operating frequency of THz silicon-integrated FMCW transceivers using the proposed topology.

### REFERENCES

- [1] P. Hillger, J. Grzyb, R. Jain, and U. R. Pfeiffer, "Terahertz imaging and sensing applications with silicon-based technologies," *IEEE Trans. THz. Sci. Technol.*, vol. 9, no. 1, pp. 1–19, Jan. 2019, doi: [10.1109/TTHZ.2018.2884852](https://doi.org/10.1109/TTHZ.2018.2884852).
- [2] X. Yi et al., "Emerging terahertz integrated systems in silicon," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 68, no. 9, pp. 3537–3550, Sep. 2021, doi: [10.1109/TCSI.2021.3087604](https://doi.org/10.1109/TCSI.2021.3087604).
- [3] H.-J. Lee et al., "Intel 22 nm low-power FinFET (22FFL) process technology for 5G and beyond," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2020, pp. 1–7, doi: [10.1109/CICC48029.2020.9075914](https://doi.org/10.1109/CICC48029.2020.9075914).

- [4] M. H. Eissa et al., “216–256 GHz fully differential frequency multiplier-by-8 chain with 0 dBm output power,” in *Proc. Eur. Microw. Conf.*, 2017, pp. 216–219, doi: [10.23919/EuMC.2017.8230838](https://doi.org/10.23919/EuMC.2017.8230838).
- [5] T. Zimmer et al., “SiGe HBTs and BiCMOS technology for present and future millimeter-wave systems,” *IEEE J. Microw.*, vol. 1, no. 1, pp. 288–298, Jan. 2021, doi: [10.1109/JMW.2020.3031831](https://doi.org/10.1109/JMW.2020.3031831).
- [6] A. Güner, T. Mausolf, J. Wessel, D. Kissinger, and K. Schmalz, “A 440–540 GHz Transmitter in 130 nm SiGe BiCMOS,” *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 779–782, Jun. 2021, doi: [10.1109/LMWC.2021.3060820](https://doi.org/10.1109/LMWC.2021.3060820).
- [7] A. Güner, T. Mausolf, J. Wessel, D. Kissinger, and K. Schmalz, “A 440–540-GHz Subharmonic Mixer in 130-nm SiGe BiCMOS,” *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 12, pp. 1161–1164, Dec. 2020, doi: [10.1109/LMWC.2020.3030315](https://doi.org/10.1109/LMWC.2020.3030315).
- [8] A. Batra et al., “Short-range SAR imaging from GHz to THz waves,” *IEEE J. Microw.*, vol. 1, no. 2, pp. 574–585, Apr. 2021, doi: [10.1109/JMW.2021.3063343](https://doi.org/10.1109/JMW.2021.3063343).
- [9] A. Batra, M. Wiemeler, D. Göhringer, and T. Kaiser, “Sub-mm resolution 3D SAR imaging at 1.5 THz,” in *Proc. Int. Workshop Mobile THz Syst.*, 2021, pp. 1–5, doi: [10.1109/IWMTS51331.2021.9486780](https://doi.org/10.1109/IWMTS51331.2021.9486780).
- [10] K. B. Cooper et al., “A high-resolution imaging radar at 580 GHz,” *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 1, pp. 64–66, Jan. 2008, doi: [10.1109/LMWC.2007.912049](https://doi.org/10.1109/LMWC.2007.912049).
- [11] K. B. Cooper et al., “THz imaging radar for standoff personnel screening,” *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 169–182, Sep. 2011, doi: [10.1109/TTHZ.2011.2159556](https://doi.org/10.1109/TTHZ.2011.2159556).
- [12] X. Mei et al., “First demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process,” *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015, doi: [10.1109/LED.2015.2407193](https://doi.org/10.1109/LED.2015.2407193).
- [13] K. M. K. H. Leong et al., “850 GHz receiver and transmitter front-ends using InP HEMT,” *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 4, pp. 466–475, Jul. 2017, doi: [10.1109/TTHZ.2017.2710632](https://doi.org/10.1109/TTHZ.2017.2710632).
- [14] B. Gashi et al., “Broadband 400-GHz InGaAs mHEMT transmitter and receiver S-MMICs,” *IEEE Trans. THz Sci. Technol.*, vol. 11, no. 6, pp. 660–675, Nov. 2021, doi: [10.1109/TTHZ.2021.3099064](https://doi.org/10.1109/TTHZ.2021.3099064).
- [15] B. Baumann, B. Gashi, D. Meier, and C. Zech, “High-resolution 400 GHz submillimeter-wave quasi-optical radar imaging system,” *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 3, pp. 226–229, Mar. 2022, doi: [10.1109/LMWC.2022.3142354](https://doi.org/10.1109/LMWC.2022.3142354).
- [16] S. Thomas, C. Bredendiek, and N. Pohl, “A SiGe-based 240-GHz FMCW radar system for high-resolution measurements,” *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 11, pp. 4599–4609, Nov. 2019, doi: [10.1109/TMTT.2019.2916851](https://doi.org/10.1109/TMTT.2019.2916851).
- [17] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, “A 210–270-GHz circularly polarized FMCW radar with a single-lens-coupled SiGe HBT chip,” *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 6, pp. 771–783, Nov. 2016, doi: [10.1109/TTHZ.2016.2602539](https://doi.org/10.1109/TTHZ.2016.2602539).
- [18] X. Yi et al., “A 220-to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture,” *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, Feb. 2021, doi: [10.1109/JSSC.2020.3020291](https://doi.org/10.1109/JSSC.2020.3020291).
- [19] G. Kühnle, H. Mayer, H. Olbrich, W. Steffens, and H.-C. Swoboda, “Low-cost long-range radar for future driver assistance systems,” *Auto Technol.*, vol. 3, no. 4, pp. 76–80, Jul. 2003, doi: [10.1007/BF03246785](https://doi.org/10.1007/BF03246785).
- [20] B. Sene, D. Reiter, H. Knapp, and N. Pohl, “Design of a cost-efficient monostatic radar sensor with antenna on chip and lens in package,” *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 1, pp. 502–512, Jan. 2022, doi: [10.1109/TMTT.2021.3098862](https://doi.org/10.1109/TMTT.2021.3098862).
- [21] B. Sene, D. Reiter, H. Knapp, and N. Pohl, “From gunplexer to MMIC: An implementation on a single chip,” *IEEE Microw. Mag.*, vol. 23, no. 1, pp. 48–53, Jan. 2022, doi: [10.1109/MMM.2021.3117320](https://doi.org/10.1109/MMM.2021.3117320).
- [22] S. M. Hossein Naghavi et al., “22.4 A 250 GHz autodyne FMCW radar in 55 nm BiCMOS with micrometer range resolution,” in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2021, pp. 320–322, doi: [10.1109/ISSCC42613.2021.9365759](https://doi.org/10.1109/ISSCC42613.2021.9365759).
- [23] M. I. W. Khan et al., “A 0.31-THz orbital-angular-momentum (OAM) wave transceiver in CMOS with Bits-to-OAM mode mapping,” *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1344–1357, May 2022, doi: [10.1109/JSSC.2022.3141366](https://doi.org/10.1109/JSSC.2022.3141366).
- [24] A. Kaineder, C. Mangiavillano, F. Ahmed, M. Furqan, and A. Stelzer, “240-GHz system on chip FMCW radar for short range applications,” in *Proc. IEEE MTT-S Int. Conf. Microw. Intell. Mobility*, 2020, pp. 1–4, doi: [10.1109/ICMIM48759.2020.9299090](https://doi.org/10.1109/ICMIM48759.2020.9299090).
- [25] Attenuation by atmospheric gases and related effects, International Telecommunication Union Recommendation P.676-12, Aug. 2019.
- [26] T. Bryllert, V. Drakinskiy, K. B. Cooper, and J. Stake, “Integrated 200–240-GHz FMCW radar transceiver module,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3808–3815, Oct. 2013, doi: [10.1109/TMTT.2013.2279359](https://doi.org/10.1109/TMTT.2013.2279359).
- [27] S. Shopov et al., “A 234–261-GHz 55-nm SiGe BiCMOS signal source with 5.4–7.2 dBm output power, 1.3% DC-to-RF efficiency, and 1-GHz divided-down output,” *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2054–2065, Sep. 2016, doi: [10.1109/JSSC.2016.2560198](https://doi.org/10.1109/JSSC.2016.2560198).
- [28] F. Ahmed, M. Furqan, K. Aufinger, and A. Stelzer, “A SiGe-based wide-band 220–310-GHz subharmonic receiver front-end for high resolution radar applications,” in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2017, pp. 983–986, doi: [10.1109/MWSYM.2017.8058754](https://doi.org/10.1109/MWSYM.2017.8058754).
- [29] U. Alakus et al., “A 210–284-GHz I-Q receiver with on-chip VCO and divider chain,” *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 1, pp. 50–53, Jan. 2020, doi: [10.1109/LMWC.2019.2954036](https://doi.org/10.1109/LMWC.2019.2954036).
- [30] K. Statnikov, E. Öjefors, J. Grzyb, P. Chevalier, and U. R. Pfeiffer, “A 0.32 THz FMCW radar system based on low-cost lens-integrated SiGe HBT front-ends,” in *Proc. Eur. Solid-State Circuits Conf.*, 2013, pp. 81–84, doi: [10.1109/ESSCIRC.2013.6649077](https://doi.org/10.1109/ESSCIRC.2013.6649077).
- [31] W. Bakalski, W. Simburger, H. Knapp, H.-D. Wohlmuth, and A. Scholtz, “Lumped and distributed lattice-type LC-baluns,” in *IEEE MTT-S Int. Microw. Symp. Dig. (Cat. No.02CH37278)*, 2002, vol. 1, pp. 209–212, doi: [10.1109/MWSYM.2002.1011595](https://doi.org/10.1109/MWSYM.2002.1011595).
- [32] S. Yuan and H. Schumacher, “90–140 GHz frequency octupler in Si/SiGe BiCMOS using a novel bootstrapped doubler topology,” in *Proc. Eur. Microw. Integr. Circuit Conf.*, 2014, pp. 158–161, doi: [10.1109/EuMIC.2014.6997816](https://doi.org/10.1109/EuMIC.2014.6997816).
- [33] S. P. Voinescu et al., “A study of SiGe HBT signal sources in the 220–330-GHz range,” *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, Sep. 2013, doi: [10.1109/JSSC.2013.2265494](https://doi.org/10.1109/JSSC.2013.2265494).
- [34] T. K. Johansen and V. Krozer, “A 38 to 44 GHz sub-harmonic balanced hbt mixer with integrated miniature spiral type marchand balun,” *Prog. Electromagn. Res.*, vol. 135, pp. 317–330, 2013, doi: [10.2528/PIER12110207](https://doi.org/10.2528/PIER12110207).
- [35] M. Abramovitz and I. A. Stegun, “Handbook of mathematical functions with formulas, graphs, and mathematical tables,” 10th ed. Washington, DC: United States Department of Commerce, National Bureau of Standards, Dec. 1972, p. 376.
- [36] M. H. Eissa, A. Malignaggi, and D. Kissinger, “A 13.5-dBm 200–255-GHz 4-way power amplifier and frequency source in 130-nm BiCMOS,” *IEEE Solid-State Circuits Lett.*, vol. 2, no. 11, pp. 268–271, Nov. 2019, doi: [10.1109/LSSC.2019.2951689](https://doi.org/10.1109/LSSC.2019.2951689).
- [37] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, “Subharmonic 220- and 320-GHz SiGe HBT receiver front-ends,” *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1397–1404, May 2012, doi: [10.1109/TMTT.2012.2190092](https://doi.org/10.1109/TMTT.2012.2190092).
- [38] F. Harris, “On the use of windows for harmonic analysis with the discrete fourier transform,” *Proc. IEEE*, vol. 66, no. 1, pp. 51–83, Jan. 1978, doi: [10.1109/PROC.1978.10837](https://doi.org/10.1109/PROC.1978.10837).
- [39] M. A. Richards, J. A. Scheer, and W. A. Holm, Eds., *Principles of Modern Radar: Basic Principles*, [ser. radar, sonar & navigation], Inst. Eng. Technol., 2010, pp. 782–783, doi: [10.1049/SBRA021E](https://doi.org/10.1049/SBRA021E).
- [40] J.-D. Park, S. Kang, and A. M. Niknejad, “A 0.38 THz fully integrated transceiver utilizing a quadrature push-push harmonic circuitry in SiGe BiCMOS,” *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2344–2354, Oct. 2012, doi: [10.1109/JSSC.2012.2211156](https://doi.org/10.1109/JSSC.2012.2211156).
- [41] T. Bücher et al., “A broadband 300 GHz power amplifier in a 130 nm SiGe BiCMOS technology for communication applications,” *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2024–2034, Jul. 2022, doi: [10.1109/JSSC.2022.3162079](https://doi.org/10.1109/JSSC.2022.3162079).



**Christoph Mangiavillano** received the M.Eng. degree in electronics and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2017. He is currently working toward the Ph.D. degree in electronics and information technology with Johannes Kepler University (JKU) Linz, Linz, Austria.

Since 2017, he has been with the Institute for Communications Engineering and RF-Systems, Johannes Kepler University Linz. His research is focused on millimeter wave and terahertz circuit design.



**Alexander Kaineder** received the Diploma Engineer and Dr. Techn. (Ph.D.) degrees in mechatronics from Johannes Kepler University (JKU) Linz, Linz, Austria, in 1999 and 2013, respectively.

From 2000 to 2001, he was with Ericsson Ahead Communications Systems, Vienna, Austria, as a Firmware Developer for DSL systems. From 2001 to 2005, he was with ABATEC Electronic AG, Regau, Austria, as a Project Manager for research and development of LPM (local position measurement technology). From 2005 to 2009, he was with DICE

- Danube Integrated Circuit Engineering, Linz, Austria, where he was responsible for the application engineering of 77-GHz RF frontends for automotive radar systems. During his doctoral thesis from 2009 to 2013 at the Christian Doppler Laboratory for Integrated Radarsensors, Johannes Kepler University Linz, he was working on system-in-package (SiP) solutions. Since joining the Institute for Communications Engineering and RF-Systems, Johannes Kepler University Linz, in 2016, he has been involved in the development of RF sensor systems in various fields of application. His main research interests include high frequency and microwave measurement, design, modeling and simulation of passive structures, design of bipolar analog RF integrated circuits, and design and characterization of multichannel radar applications.



**Klaus Aufinger** (Member, IEEE) received the diploma and the Ph.D. degrees in physics from the University of Innsbruck, Innsbruck, Austria, in 1990 and 2001, respectively.

From 1990 to 1991, he was a Teaching Assistant with the Institute of Theoretical Physics, University of Innsbruck. In 1991, he joined the Corporate Research and Development, Siemens AG, Munich, Germany, where he investigated noise in submicron bipolar transistors. He is currently with Infineon Technologies, Neubiberg, Germany, the former semiconductor

group of Siemens, Munich, working in the field of device physics, technology development and modeling of advanced SiGe technologies for high-speed digital and analog circuits. He has coauthored more than 200 publications in scientific journals and conferences. He also gives lectures on analog bipolar technology at the Technical University of Munich, Munich, Germany.

Dr. Aufinger serves as a Reviewer for several journals and the EUMW, and was a member of the technical program committee of the IEDM.



**Andreas Stelzer** (Member, IEEE) received the Diploma Engineer degree in electrical engineering from the Technical University of Vienna, Vienna, Austria, in 1994, and the Dr. Techn. degree (Ph.D.) in mechatronics (with honors sub auspiciis praesidentis rei publicae) from the Johannes Kepler University (JKU) Linz, Linz, Austria, in 2000.

In 2003, he became an Associate Professor with the Institute for Communications Engineering and RF Systems, Johannes Kepler University Linz. Since 2008, he has been a key Researcher for the Austrian

Center of Competence in Mechatronics (ACCM), Linz, Austria, where he is responsible for numerous industrial projects. In 2007, he was granted a Christian Doppler Research Laboratory for Integrated Radar Sensors, and since 2011, he has been a Full Professor with the Johannes Kepler University Linz, heading the Department for RF-Systems. He is cofounder of company Inras, where industrial radar sensors are developed. Since 2020, he has also been the Head of the joint Linz Institute of Technology (LIT) and Silicon-Austria-Labs (SAL) Millimeter-Wave Lab working on combined sensing and communication applications for future 6G. He has authored or coauthored in more than 430 journals, conference, and workshop contributions. His research is focused on microwave sensor systems for industrial and automotive applications, integrated radar sensor concepts, SiGe-based circuit design, microwave packaging in eWLB, RF and microwave subsystems, surface acoustic wave (SAW) sensor systems and applications, as well as digital signal processing for sensor signal evaluation.

Dr. Stelzer is a member of the Austrian ÖVE. He has served as an Associate Editor for the *IEEE Microwave and Wireless Components Letters*. He was the Chair of MTT-27 Wireless-Enabled Automotive and Vehicular Applications. He was the recipient of several awards including the 2008 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Outstanding Young Engineer Award, the 2011 IEEE Microwave Prize, and the Best Paper Award of the International Journal of Microwave and Wireless Technologies (IJMWT) 2016. Furthermore, he was the corecipient of the 2012 European Conference on Antennas and Propagation (EuCAP) Best Measurement Paper Prize, the 2012 Asia Pacific Conference on Antennas and Propagation (APCAP) Best Paper Award, the 2011 German Microwave Conference (GeMiC) Best Paper Award, as well as the IEEEfCOM Innovation Award and the European Microwave Association (EuMA) Radar Prize of the European Radar Conference (EuRAD) 2003. He is a member of the IEEE MTT, IM, and CAS Societies and he served as IEEE Distinguished Microwave Lecturer for the period 2014–2016 and was the Chair of IEEE International Conference on Microwaves for Intelligent Mobility (ICMIM) 2020.