Broadband 400-GHz InGaAs mHEMT Transmitter and Receiver S-MMICs

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***Abstract*—The modeling, design, and experimental evaluation of both a 400-GHz transmitter and receiver submillimeter-wave monolithic integrated circuit (S-MMIC) is presented in this article. These S-MMICs are intended for a radar-based system in the aforementioned operating frequency. The transmitter occupies a total chip area of $750 \times 2750\,\mu\mathrm{m}^2$. It consists of a multiplier-by-four, generating the fourth-harmonic of the WR-10 input signal, which drives the integrated WR-2.2 power amplifier. The latter has an output-gate width of 128 μm. The receiver S-MMIC, $750 \times 2750\,\mu\mathrm{m}^2$, consists of a multiplier-by-two, providing the second harmonic of the WR-10 input signal for the local-oscillator port of the subsequent integrated subharmonic mixer. The radio-frequency port of the latter, connects via a Lange coupler to a WR-2.2 low-noise amplifier (LNA). All the components included, are processed on a 35-nm InAlAs/InGaAs metamorphic high-electron-mobility transistor integrated-circuit technology, utilizing two-finger transistors and thin-film microstrip lines (TFMSLs). The modeling approach of the amplifier cores and the respective design decisions taken are listed and elaborated-on in this work. Accompanying measurements and simulations of the transmitter and receiver are presented. The individual components of the aforementioned S-MMICs, are characterized and the results are included in this article. The state-of-the-art, for S-MMIC based circuits operating in the WR-2.2 band, is set by the LNA, on one side, spanning an operational 3-dB bandwidth (BW) of 310 to 475 GHz, with a peak gain of 23 dB and, on the other side, by the final transmitter design, which covers an operating range of 335 to 425 GHz with a peak-output power of 9.0 dBm and accompanying transducer gain of 11 dB. The included transmitter- and receiver-designs represent a first-time implementation in the mentioned technological process, utilizing solely TFMSLs, boasting the integration level, operating in the WR-2.2 frequency band, and setting the state of the art—to the authors' best knowledge—for all S-MMIC based solutions in the respective frequency band, in terms of output power and gain over the operating 3-dB BW.**

***Index Terms*—InGaAs, power amplifier (PA), low-noise amplifier (LNA), subharmonic mixer, multiplier-by-four, transmitter, receiver, metamorphic HEMT.**

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I. Introduction

TERAHERTZ frequencies offer largely unrestricted and wide-band transmit/receive windows for the implementation of applications such as the inspection of composite materials [1]–[3], radar imaging [4]–[6], and data transfer over reasonable distances [7]–[11]. Such applications profit from the higher-available bandwidth (BW), which increases the achievable resolution in radar-based applications, and boosts data rates for wireless communication systems.

Yet, with the steep increase in free-space absorption, for frequencies beyond 300 GHz, the aforementioned benefits are impaired by the insufficient radio-frequency (RF) power over the desired BW. Starting from the transistor's level, depending on the selected technology, the bottleneck may be the device itself, limited by its maximum frequency gain and device-level power density. Complex and innovative antenna front-end solutions have been shown to alleviate the issue, by providing a large directional gain [12], yet these approaches cannot compensate for the lack of generated RF power per device. Rather, a potential increase in dielectric losses is expected. Thus, the active chain and the passive radiating element, require design optimization in order for the respective application to meet the desired requirements.

In this article, the point of interest is the active chain of such an application, required for realizing 400-GHz transmitter and receiver submillimeter-wave monolithic integrated circuits (S-MMICs) that operate over a large BW, while providing the required gain, noise figure (NF), and output power over the complete range. The included designs are developed for the WR-2.2 waveguide band, from 325 to 500 GHz and intended for radar-based applications. This particular frequency band presents a viable option for short- and medium-range communications, as well as radar applications [13]. The implementation of land mobile and fixed services, in said frequency band, is also recommended by the 2019 World Radiocommunication Conference [14].

This article presents the modeling, design, and experimental evaluation of all the required active and passive components up to, but not involving, the main radiating element, for a functioning WR-2.2 transmit/receive radar system. These include a multiplier-by-four (x4), converting the input signal from the WR-10 to WR-2.2 waveguide band, WR-2.2 power amplifier (PA), WR-2.2 low-noise amplifier (LNA), respective Lange coupler and subharmonic mixer. The chips are processed on Fraunhofer IAF's 35-nm $\mathrm{In_{0.52}Al_{0.48}As/In_{0.80}Ga_{0.20}As}$

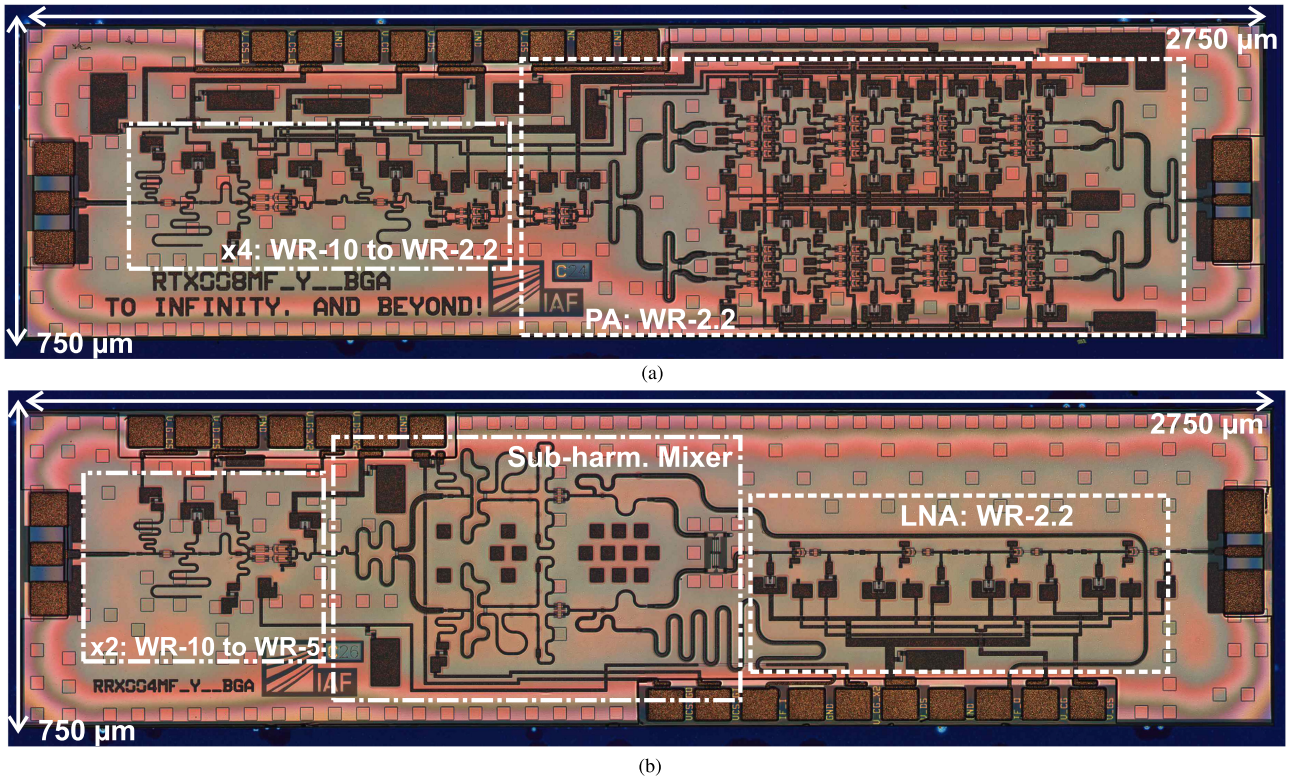


Fig. 1. Microphotograph of the fabricated transmitter (a) and receiver (b) S-MMICs.

metamorphic high-electron-mobility transistor (mHEMT) integrated-circuit (IC) technology. The via molecular-beam epitaxy grown layers boast a channel mobility of 9800 $\mathrm{cm}^2/\mathrm{Vs}$ and carrier density of 6.1E12 cm^{-2}. The front-end-of-line process of the mHEMT devices, which are fabricated on 100-mm GaAs wafers, is described in detail in [15]. The multilayer back-end-of-line (BEOL) process consists of a total of three metal layers separated via benzocyclobutene (BCB), a thin sheet of chemical vapor deposited SiN—utilized in the layout of metal-insulator-metal (MIM) capacitors—and NiCr thin-film resistors. The utilized mHEMT transistors are processed with an increased gate-drain recess, allowing for drain–source voltages of up to 1.5 V, with the OFF-state breakdown voltage above 4 V. The technology boasts a transition and maximum oscillation frequency of $f_{\mathrm{T}} > 500$ GHz and $f_{\max} > 1000$ GHz, respectively, with a peak trasconductance of 2500 mS/mm and drain current density of 1300 mA/mm.

In the following section, a brief overview on the transmitter and receiver architecture is provided. In Section III, the PA design is presented, starting with the core-amplifier unit, and proceeding with an analysis on the design decisions. Section IV, gives insight on the x4 and its individual stages, while Section V elaborates on the subharmonic mixer. Section VI is dedicated to the design of the LNA. The measurement and simulation results of the transmitter and receiver, as well as the corresponding subcircuits are evaluated in detail in Section VII. A state-of-the-art analysis follows in Section VIII, with a brief conclusion in Section IX.

II. Transmitter and Receiver Design

The transmitter and receiver S-MMICs are depicted in Fig. 1(a) and (b), respectively. The transmitter occupies a total chip area of $750 \times 2750\,\mu\mathrm{m}^2$, including the chip frame and RF-pads. It consists of a x4 that up-converts the input WR-10 waveguide-band signal to that of the WR-2.2 waveguide band. This output is amplified by a two-stage cascode buffer-amplifier, which serves as a one-to-four Wilkinson driver—rather two cascaded Wilkinson-divider-stages driver—for the subsequent WR-2.2 PA. The latter consists of a total of four gain stages, with an output-stage total gate-width (TGW) of 128 μm.

The receiver occupies a total chip area of $750 \times 2750\,\mu\mathrm{m}^2$, including the chip frame and RF pads. It consists of a multiplier-by-two (x2), which up-converts the WR-10 local oscillator (LO) signal to a WR-5 output. This is fed into a subharmonic mixer realized via 180°-shifted common-source transistors. The intermediate frequency (IF) ports are equipped with low-pass filters for coupling out the difference between the LO and the incoming RF signal. The RF-port of the mixer is connected via a Lange coupler to an integrated broadband LNA. The former enables an in-phase and quadrature operation on the down-converted signal.

III. Power Amplifier Design

The core unit, upon which the included PA and buffer medium PAs (MPAs) are built around, consists of a cascode with two

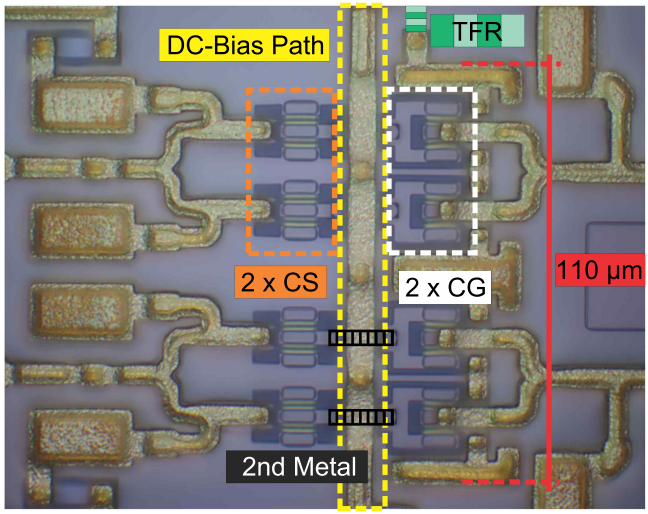


Fig. 2. Microphotograph of the utilized cascode core, here depicted with a TGW of 64 μm.

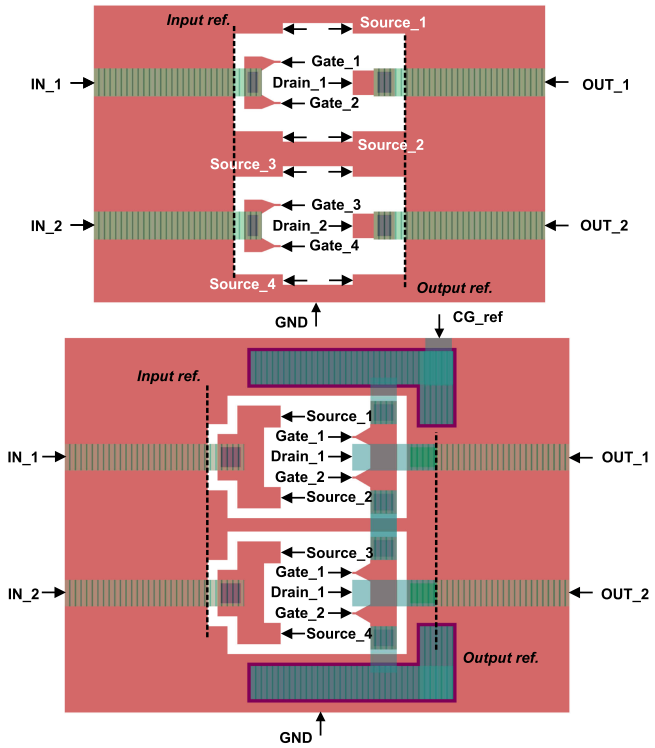


Fig. 3. Depiction of the in-ADS, via Momentum, 2.5-D EM simulated CS and CG extrinsic shells.

parallel common-source (CS), respectively, common-gate (CG), InAlAs/InGaAs two-finger mHEMTs, with either an 8 μm, WR-2.2 case, or 20 μm, WR-5 case, finger-width. A microphotograph of the 400-GHz cascode cell with four parallel two-finger devices, can be seen in Fig. 2.

The cascode device configuration is chosen for the amplifier stages in the reported circuits, due to its superior performance in terms of achievable gain over a wide operating BW with a significant isolation between the input and output ports. To avoid soft compression and improve the output-power performance, the value of the capacitance at the gate of the CG transistor is reduced to a finite size, implementing a design approach similar to [16]–[18] and enabling an improved output power over a large BW.

Each cascode core consists of solely two-finger mHEMTs, which amass to a TGW of 32 μm at the core's output, for the WR-2.2 case. The WR-5 buffer MPA on the other hand has a TGW of 80 μm per core. Two-finger devices are utilized, mainly due to their symmetric-extrinsic shell, consisting of a coplanar-waveguide (CPW) feeding structure with no bridge connections between multiple gate fingers. These aid in odd-mode suppression and near-identical bias-point operation when parallelizing multiple fingers of large unitary-finger width (UFW). Due to the relatively small UFW of the two-finger transistors implemented in all of the included designs, the latter is neglected. The symmetry and simplicity of the two-finger extrinsic shell, reduces the complexity of the respective 2.5- or 3-D electromagnetic (EM) models utilized.

The intrinsic properties of the utilized two-finger mHEMTs are implemented via a polynomial-based model, set-up in Keysight's Advanced Design System (ADS) schematic environment, with the corresponding data extracted from on-wafer measurements [19]. Initially, this model contains a preliminary extrinsic-shell approximation via analytically fit ADS components, validated only up to 300 GHz. Since the focus of this work is in the design of broadband 400-GHz transmitter and receiver S-MMICs, the former is replaced with a 2.5-D EM model, seen in Fig. 3. This model is simulated in ADS's Momentum solver, such that the precision in predicting the transistor's behavior beyond the previously mentioned limit is increased. A more in-depth look on this modeling approach is provided in [20], yet there the models are adjusted for the WR-3.4 band, whereas here they are optimized for the WR-2.2 frequency band. To ensure that the new transistor model, with the added 2.5-D EM simulated extrinsic shell, one-to-one reproduces the experimentally validated results of the original, the respective extrinsic-shell layout is iteratively updated, focusing on the definition of the exact reference points of the various ports and ground node on said model. The extrinsic shell is simulated for frequencies well beyond the 300-GHz limit, such that the combined model can be utilized for designing PAs well beyond the 400-GHz mark. A 2.5-D EM solver is utilized, as the available port definition and excitation methodology present in Momentum, and the benefits of a fully integrated cosimulation between the transistor-finger model and the extrinsic shell, to the authors' knowledge, outweigh the benefits of using an external 3-D EM simulation tool. The latter becomes significant when dealing with meandered matching structures and subsequent cross-coupling effects that occur over the various metalization layers, and is as such utilized in this work as well.

A. WR-2.2 Six-Stage PA, 128-μm TGW

Making use of the BEOL seen in Fig. 4, the PA, depicted in Fig. 5, consists of a total of four gain and two Wilkinson-driver stages. Each stage is composed of the presented cascode

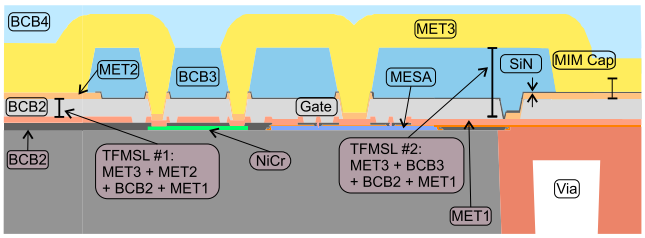


Fig. 4. Layer stack of the utilized 35-nm InGaAs mHEMT technology, courtesy of Fraunhofer IAF.

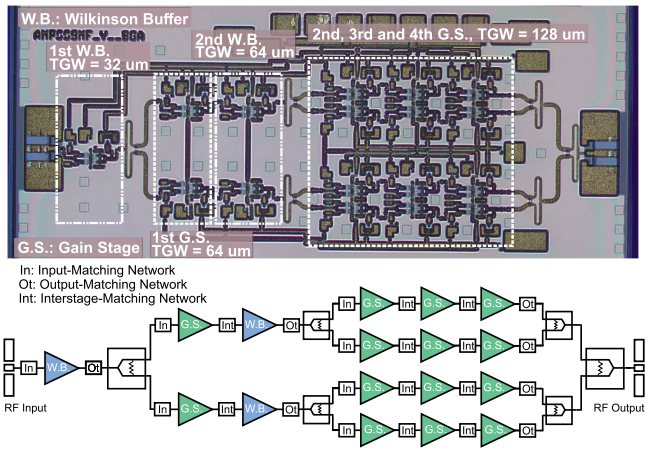


Fig. 5. Microphotograph of the fabricated PA, with a TGW of 128 μm at the output stage, and its respective schematic representation.

design, Section III, with a varying output TGW per stage. The latter is realized via the parallelization of said cores, utilizing Wilkinson combiners. The UFW is set to 8 μm across all the stages. A four-stage MPA based on a slightly bulkier design of the utilized cascode core, with a TGW of 32 μm, is presented in [21]. It can be considered as the first iteration of the implemented design-approach taken in this work.

The here discussed cascode-core designs are displayed in Fig. 2, with a relatively compact layouting of the parallelized CG transistors, where a 64-μm TGW core occupies a physical width of 110 μm. The matching networks of the individual stages are realized via miniaturized thin-film-microstrip line (TFMSL) technology. Contrary to coplanar matching structures, TFMSLs allow for far more design freedom, in terms of routing and compactness. Furthermore, the designer gains a greater degree of leeway when considering wafer-substrate thickness, since the first metal layer of the BEOL functions as the ground reference, rather then the wafer backside metallization.

A schematic representation of a two-stage 32-μm variant of the implemented amplifier topology can be seen in Fig. 6. The input, output, and interstage matching presented, is based on TFMSLs and MIM capacitors. These, form *L*–*C* networks—of up to the third order—that transform the input and output impedance to either a reference value—in the case of the first and last stage of the amplifier, with the reference being the input and output termination impedance—, or the complex conjugate of the adjacent stage—to ensure maximum power transfer between the stages. Benefiting from the high f_{T} and f_{max} of the chosen technological process, the main design task is in the compact and

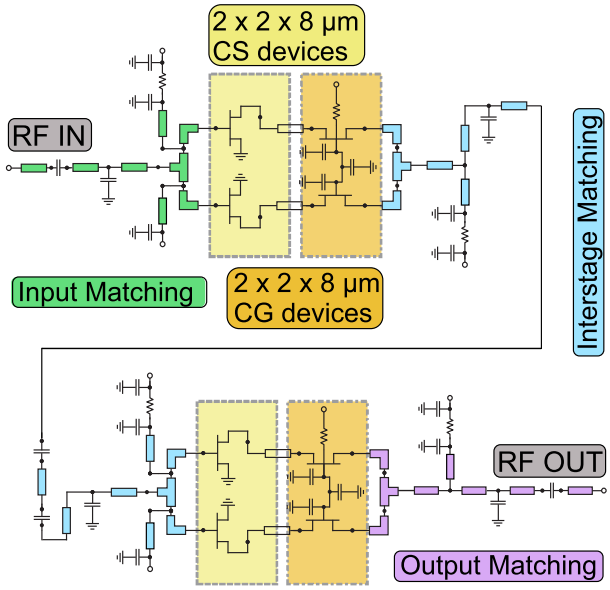


Fig. 6. Schematic representation of two cascode stages with an output TGW of 32 μm.

low-loss meandering of the TFMSL structures. In order to avoid any unwanted coupling effects, these structures are thoroughly simulated.

The matching networks, including the respective biasing stubs, are initially designed utilizing ADS components that implement numerical models to approximate the behavior of such TFMSLs with specific substrate and layer-stack conditions defined. The respective networks are then layouted, having undergone optimization via ADS's harmonic-balance and/or small-signal simulation, and the complete stack is imported as a 3-D CAD file into Computer Simulation Technology's Studio Suite (CST), to undergo full 3-D EM simulation. Through the latter, it is possible to identify unexpected and unwanted cross coupling effects, as a result of compact meandering. In order to reduce losses and the constriction of the operating BW, the matching is performed as early as possible, and is kept as compact as the cross coupling allows.

These 3-D EM models are critical in the design of highly complex and compact structures in the submillimeter wave range. They must reliably model the exact processed physical attributes of the BEOL. Due to a lack of planarization, dependent on which type of TFMSL is utilized—labeled in Fig. 4—and what size and density difference there is with respect to the neighboring structures, the top metal layer can undergo slight deformations, in that the TFMSL cross-section slightly differs from an expected rectangular shape. Considering that the skin-effect is very high, in the operating frequency range, this may slightly alter the impedance transformation targets, resulting in reduced performance. For the realization of the matching networks, the first variant of TFMSLs is applied, with the topmost MET3 metal layer merged with the middle metal layer MET2, while the first metal layer MET1 serves as the ground.

The first variant is selected, such that the required line-width-to-impedance relation, due to the thinner substrate, reduces

the overall TFMSL required width, benefiting the meandering. A secondary benefit, is the presence of BCB between two adjacent TFMSLs, thus reducing potential cross-coupling by encapsulating the structures and thus minimizing any TFMSL shape alterations. The impedance targets resulting in the largest possible operating BW, with a match of 2:1 voltage-standing wave ration (VSWR) or better, with regard to a target impedance are sought. These include 50 Ω, the complex conjugate of the interstage impedances, port impedance of the various Wilkinson combiner/divider structures, and the input/output impedance targets of the first/last stages of the MMIC. The second-metal (MET2) TFMSL extension from the CS to the CG is included in the optimization process. A wide-band and flat response of the amplifier is desired.

As noted in Fig. 5, the PA featured in this article is composed of four gain and two Wilkinson-divider buffer stages. The latter compensate the insertion loss of the Wilkinson dividers—designed utilizing the second variant of the presented TFMSLs, with MET3 (2.7 μm thick) serving as the conductor, while BCB3–BCB2 (3.5 and 1.4 μm, respectively) serve as the dielectric substrate, and MET1 as the ground reference. The thicker dielectric substrate allows for the relaxation of the line-width-to-impedance relationship, making formerly infeasible impedance targets feasible. This is due to the fact, that reaching higher impedance values no longer requires a line width below the processing limit. As such, closer-to-the-ideal impedance transformations are possible in the design of the Wilkinson structures.

However, the higher the metal on the stack, the lesser compact the design becomes, due to the increased overcoupling and the sheer bulkiness of the TFMSLs when compared to their lowered counterparts. The respective termination resistor, which in the ideal case should represent a point resistance, depending on the processing limitations, increases the losses as it introduces a certain electrical length. This affects the isolation of the structures, thus the design intent should focus in configuring the contacting of said thin-film resistor (TFR) such that the correct impedance value is maintained, while the respective electrical length is minimized.

The presented PA is divided in three main sections, with the TGW of each section doubling when moving to the next, ensuring that all stages are driven in saturation, when the device is in large-signal drive. The first stage, with a TGW of 32 μm, mainly compensates for the insertion losses of the first Wilkinson divider, while the second and third stage are gain and buffer stages, respectively. Here the TGW is doubled to 64 μm. The fourth, fifth, and sixth stage are all dedicated to gain and the TGW is doubled to 128 μm, with the intent of achieving a high output power in the WR-2.2 band.

IV. Multiplier-by-Four

The x4, depicted in Fig. 7, consists of two doubler and, respectively, two buffer stages. It upconverts a signal from the WR-10 to the WR-2.2 band, which serves as the input for the WR-2.2 PA, in the integrated transmitter chip.

The first doubler stage consists of a two-finger CS transistor, with a TGW of 30 μm, biased in AB mode. The fundamental

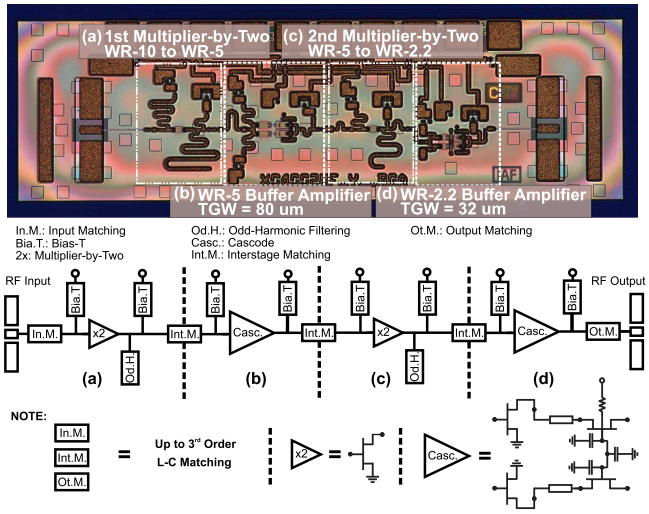


Fig. 7. Microphotograph of the fabricated x4 MMIC, upconverting WR-10 signals to the WR-2.2 band, including its respective schematic representation.

and odd-harmonics are suppressed, via quarter-wavelength stub transformations, whereas the even harmonics pass through to the WR-5 buffer stage, composed of two-finger 20-μm UFW mHEMTs. This stage is composed utilizing the previously mentioned cascode topology, and the transistors are parallelized to reach an output TGW of 80 μm. This buffer stage is optimized to have a wide-band and flat response, such that the second doubler stage is not driven into saturation, but rather receives a linear input drive. A buffer stage designed for peak output power and transducer gain is not desired, rather a constant output power and compression behavior over the complete operating BW is intended.

The second doubler, composed of yet another two-finger CS transistor as seen in the first stage, upconverts the buffered WR.5 signal to the WR.2.2 waveguide band, where it is fed into the WR-2.2 buffer amplifier that represents a 32-μm WR-2.2 cascode stage as elaborated on previously. The buffer amplifier acts as a bandpass filter as well, suppressing the higher harmonics generated by the last doubling stage. Similar to the PA, the x4 is designed with compactness and wide-band performance in mind. TFMSLs, of the first variant only, are utilized in order to tightly meander the respective open-stubs of the matching structures.

V. Subharmonic Mixer

Depicted in Fig. 8, is a subharmonic mixer, the LO port of which is driven by an x2. The doubler and buffer amplifier stages, are identical to that of the x4 introduced in Section IV. The input signal, belonging to the WR-10 band, is upconverted to the WR-5 band, or to half of the incoming RF signal's frequency. The advantages of such a setup lie in the lower LO re-radiation through any radiating element added to the receiver chip, lower LO-buffer current and direct current (DC) offset at either the IF-quadrature (IF-Q) or IF-in-phase (IF-I) component.

The presented subharmonic mixer is a passive mixer. It uses two identical two-finger transistors in the CS topology, without a

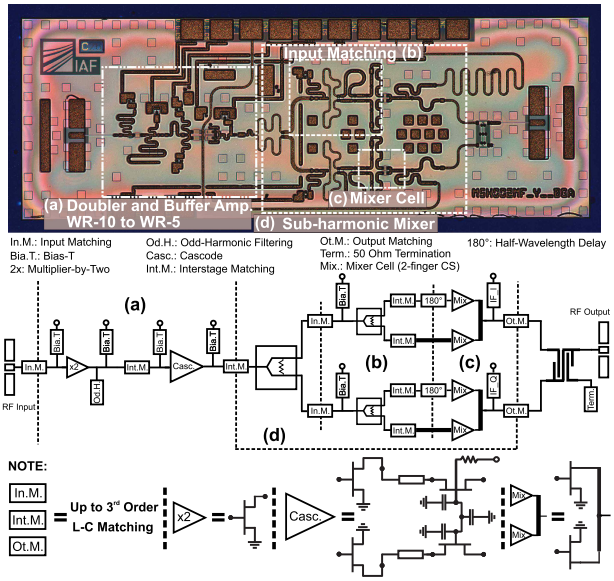


Fig. 8. Microphotograph of the fabricated subharmonic mixer with a WR-2.2 Lange coupler at the RF ports. Included is the respective schematic representation.

drain-source bias, that are fed a balanced LO signal. Since, both the I and Q channels are required, this mixer cell is mirrored and the LO is initially divided via a Wilkinson divider matched for the WR-5 band. Furthermore, the respective input matching network ensures that the conversion gain is constant over the operating bandwidth of WR-2.2. This step is crucial in realizing a flat response over the operating BW, yet it introduces losses in the LO-signal's path. Since these kind of mixers are highly dependent on the drive level when it comes to losses, it is crucial that such matching structures are 3-D EM simulated, such that the generated losses are taken into consideration when attempting to find the optimum drive level. An LO drive above or below said point, leads to a significant increase in losses.

The incoming RF signal is split via a Lange coupler, designed in MET1, utilizing a quasi-MSL environment with respect to the back-side metallization of the wafer, ensured by the corresponding via cage around it. Such a via cage is required, due to the large difference between the GaAs-substrate thickness of 50 μm and the MET1-based MSL width, preventing a proper MSL mode to propagate. This side-effect causes higher losses in the RF path of the mixer, lowering the conversion gain as a consequence. With the Lange coupler resulting in 90°-shifted outputs, an I and Q channel can be distinguished. The respective IF signals are a product of the RF signal and an effective LO—where the fundamental frequency components fall off, due to the balanced mixing—and the second harmonics, those of the WR-2.2 band, undergo constructive interference, resulting in a signal that has twice the subharmonic LO frequency. Through a low pass filter, the difference between the effective LO and the incoming RF from either IF port of the Lange coupler is acquired.

As previously mentioned, the S-MMICs presented in this work are intended for radar-based applications. In particular,

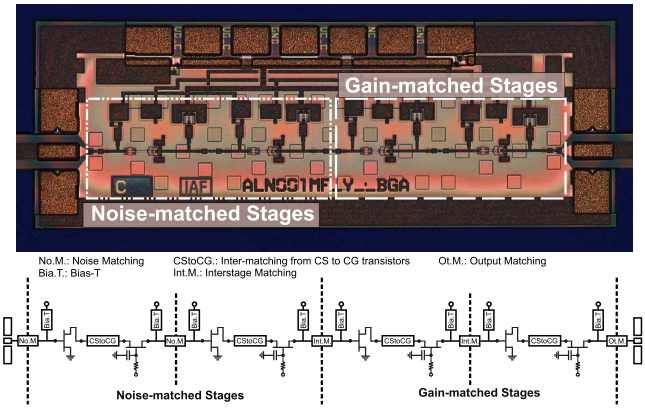


Fig. 9. Microphotograph of the fabricated LNA, including the schematic representation.

frequency-modulated continuous wave based imaging and scanning. While the former benefits from the inherent small wavelength, the latter is primarily dependent on the conversion gain acquired over the operating BW and the dynamic range of the receiver, both yielding in an improvement of the respective vertical resolution of a hypothetical radar scan [3]. Since for such an application, the radar targets are within the kHz-to-a-dozen-MHz range, the IF BW is of minimal concern to this design. Rather, the balanced approach improves the noise level by half, in theory.

VI. LNA Design

The LNA, depicted in Fig. 9, is composed of four cascode stages, the first two matched with respect to noise, whereas the last two are designed with respect to gain-over-BW performance. "Matched with respect to noise," in this context, refers to the design of the first two stages that leads to the smallest possible minimum noise figure (NF). The NF represents the degradation—expressed in dB—of the signal-to-noise ratio by the cascaded active components in a chain. According to Friis' definition of NF and Friis' formula for noise temperature [22], only the first components of the chain significantly impact the NF, if they present sufficient gain. Thus, only the first two stages of the LNA were matched for noise.

Each cascode stage has a TGW of 16 μm at its output. The main noise-affecting components are the first and second stage of the LNA, with later stages' contributions considered negligible. Thus, in order to match for the ideal noise targets, apart from the standard matching through the TFMSLs, of the first variant, the MET2-TFMSL extension between the CS and CG transistor, of the cascode unit, is included in the matching process considering that it significantly impacts the noise contribution of the first two-stages.

VII. Experimental Evaluation Versus Simulation

The measurements presented in this section are acquired via on-wafer probing. All the results, including the simulations, are from S-MMICs with a thinned down $GaAs$ substrate of 50 μm. This holds true throughout this article.

The influence of the probe contacting the chip, as well as the respective RF-pads and RF-pad extensions in the chip are

part of the presented results in this section. This holds true for all the various chips under test, for both scattering parameter (S-parameter) and large-signal measurements.

Regarding the acquisition of the S-parameters, an Agilent N5224A performance network analyzer (PNA) with Virginia Diodes Inc's (VDI) WR-2.2 extensions is utilized. The respective RF-probes are de-embedded, utilizing a through-reflect-line calibration procedure on an impedance-standard substrate.

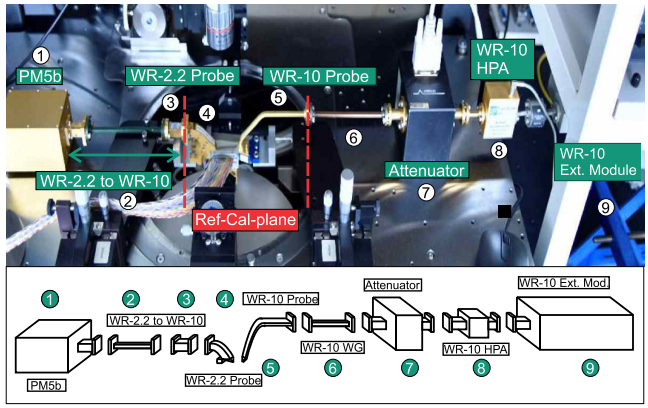
The large-signal measurement set-ups for the various chip configurations are presented in Fig. 10. In Fig. 10(a), the measurement set-up of the transmitter, seen in Fig. 1(a), and the stand-alone x4 chip, seen in Fig. 7, is presented. The input drive is generated via a VDI WR-10 extension module, the output of which is amplified via an in-house high-power amplifier (HPA). The output of said amplifier is adjusted via a Millitech motorized attenuator, and passes through a WR-10 waveguide extension to the respective WR-10 Cascade Infinity probe. The output-chain of the measurement set-up is composed of a WR-2.2 Cascade T-Wave probe, connected to a WR-10-to-WR-2.2 transition, that extends to a VDI Erickson PM5b power meter. The power calibration plane is at the waveguide-hinges of the RF probes, the losses of which are compensated based on the values provided by the respective manufacturer.

The identical input-drive chain is present in the measurement set-up of the receiver, seen in Fig. 1(b), and stand-alone subharmonic mixer chip, seen in Fig. 8, depicted in Fig. 10(b). The output chain drives the LNA present in the receiver, or provides the RF signal for the subharmonic mixer. It consists of a WR-6.5 AFM12 active frequency multiplier-by-twelve from Radiometer Physics in tandem with VDI's passive WR-2.2 multiplier-by-three connected to a WR-2.2 probe. The power amplifier measurement set-up consists of the AFM12, the output of which is buffered via a VDI WR-6.5 AMPR2 HPA, connected to the upper mentioned WR-2.2 multiplier-by-three. The probing is achieved via the WR-2.2 T-Wave probes. The output contains a WR-2.2-to-WR-10 transition to the PM5b.

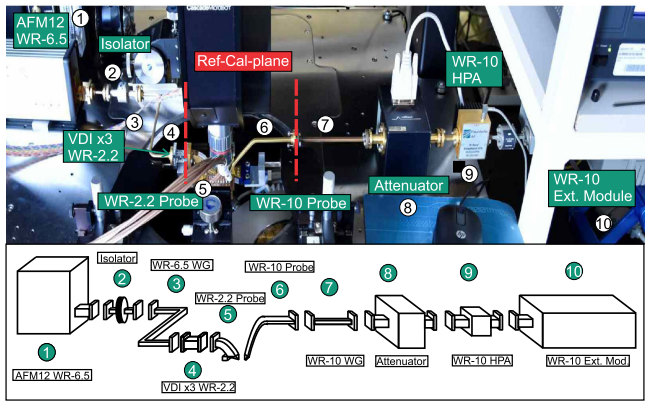
A. WR-2.2 PA, Measurements versus Simulation

The measured and simulated small-signal results of a 32-μm TGW single-stage cascode, Fig. 11, which constitutes the core building block of all the amplifiers in this work, are presented in Fig. 12. The measurement versus the simulation curves, with regard to the gain or S_{21}, are in good agreement to each other with a flat response of about 5 dB from 325 to 425 GHz. To note, is that this particular single-stage cascode is of the initial design presented in [21], thus the upper 3-dB point of the small-signal gain sits at around the 430-GHz mark. The input reflection coefficients are sufficiently well predicted by the modeling and simulation approach taken, with the output reflection coefficients requiring a more in-depth look at the influence of the RF-probes, the contacting on the RF-pads, and the on-chip MSL extensions to the actual matching structures of the active devices.

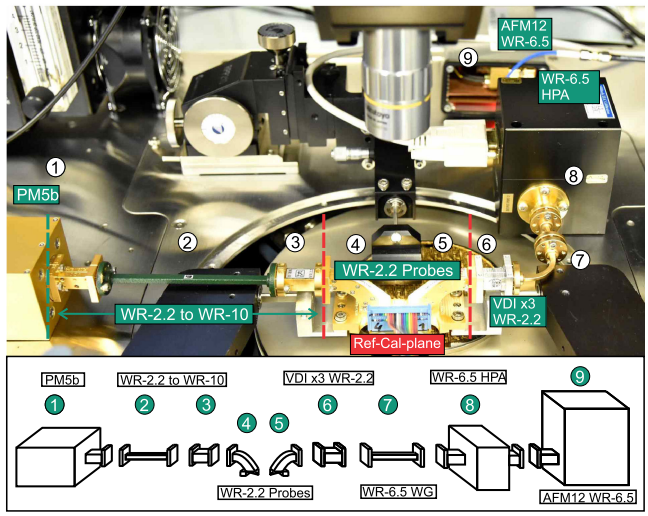
As mentioned in Section III, this approach is subsequently improved upon, taking particular care in embedding the influences of the RF-pads, seen in the measurement, to the simulation domain. Dependent on where the RF-probes contact the on-chip



(a)



(b)



(c)

Fig. 10. Measurement set-up utilized in the large-signal characterization of the transmitter—including the stand-alone multiplier-by-four—(a), the receiver—including the stand-alone mixer—(b) and the PA (c).

RF-pads, the probe tips might not only see the respective RF-pad, the MSL extension and then the active circuit with its matching structures, but rather an added open stub in parallel to all the prior. Depending on the electrical length, this added open stub, shifts the output or input matching of the active devices, leading to potential differences in simulation versus measurement. In a worst case scenario, it may lead to instabilities.

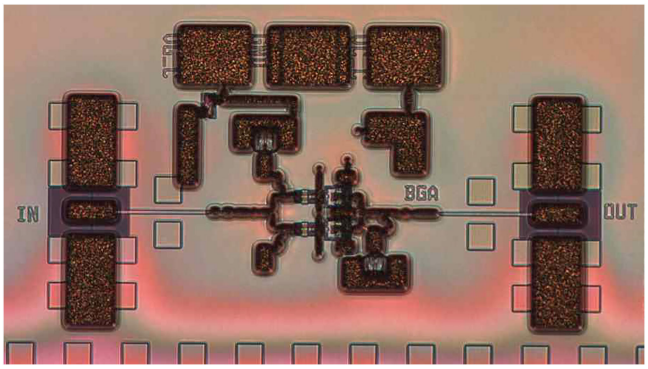


Fig. 11. Microphotograph of a fabricated single-stage cascode, with a TGW of 32 μm.

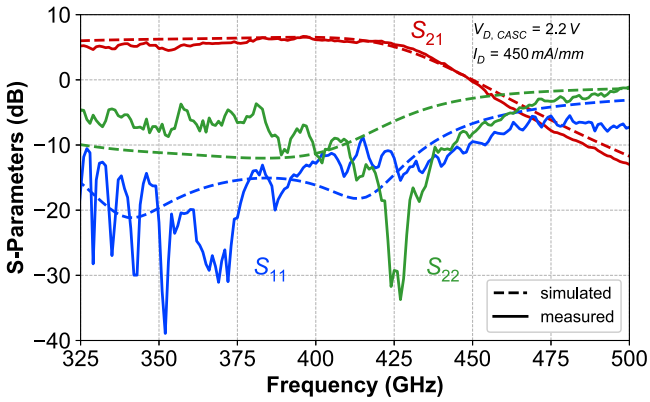


Fig. 12. Measured versus simulated S-parameters of a 32-μm TGW, single-stage cascode, as implemented in this work.

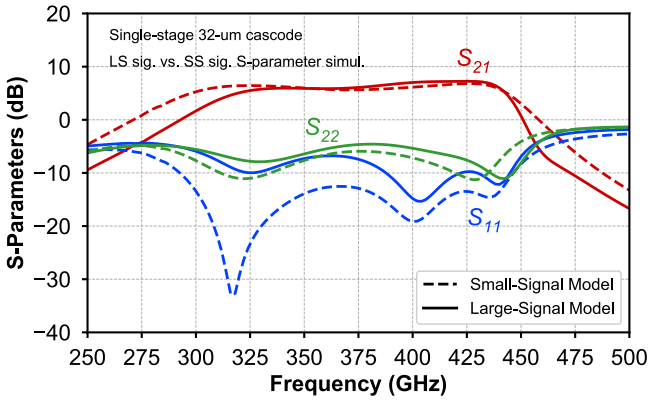


Fig. 13. Single-stage cascode S-parameter simulation utilizing either the SS or the LS transistor models.

Since the SS model successfully predicts the measured S_{21}, the S-parameter simulation utilizing both it and the respective large-signal (LS) model are plotted for an updated single-stage cascode design—that adheres to what is presented in this article—in Fig. 13. Considering the difficulties in large-signal modeling, at the frequency band of interest, the overlap between the two models is sufficient, with the LS model predicting a lower operating BW of the device under test. Since the S-parameter measurements presented in this work nearly

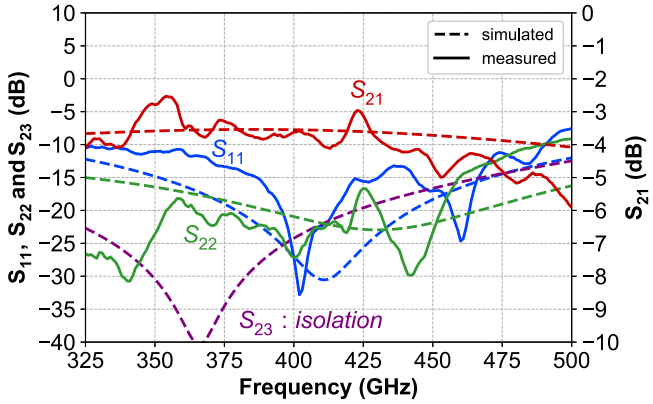


Fig. 14. Measured versus simulated S-parameters of the implemented 2:1 Wilkinson combiner/divider, WR-2.2.

one-to-one fit the via SS-model simulated S_{21}, thus also the respective BW, it can be expected that the large signal measurements are of a higher relative BW then what the LS model predicts. Consistent to the approach taken throughout this work, whether the transistor fingers are modeled based on small- or large-signal data, the extrinsic shell modeling and the complete simulation of the component is as introduced in Section III.

The PA depicted in Fig. 5, makes use of a 4:1 Wilkinson combiner with a total insertion loss of about 1.5 dB, 1 dB of which is due to the larger 2:1 combiner and the remaining 0.5 dB are due to the compacter variant. The S-parameter measurements of the latter are displayed in Fig. 14, where the influence of the on-chip RF-pads and their respective MSL extension is included in the simulation. The ripple present in the measurements is common for the operating BW and is significantly affected by either the off- or on-wafer calibration procedures. As can be seen, there is a good agreement between the simulated and measured S_{21}, thus the former are referred to when stating insertion loss values of approximately 0.5 dB for the frequency range from 350 to 430 GHz. The S_{23} represents the isolation. In this case, the simulated value is ≤ -20 dB for the operating frequency range.

Since the first stage of the 128-μm TGW PA has a gain of around 5 dB, in order to drive the second stage, one has to compensate for the losses over the divider and the 3-dB split itself. Thus, the buffer stage ensures that the driving power seen after the initial division is sufficient for the subsequent gain stage. This approach proceeds through the second splitting stage, after which, the remaining stages are dedicated to purely drive the last output stage into saturation.

Depicted in Fig. 15, the measured versus simulated S-parameter results of the PA reveal a strong overlap, in particular for the gain. This is a good indication that the introduced modeling and simulation approach in this work can predict the actual behavior of complex designs at frequencies well beyond 300 GHz. The measured input and output reflection coefficients are satisfactory, ≤ -10 dB over the operational BW. With four dedicated gain stages, the PA achieves a small-signal gain of around 22 dB, with an upper-3-dB point at 440 GHz. The transducer gain, in large-signal drive, and the output power are

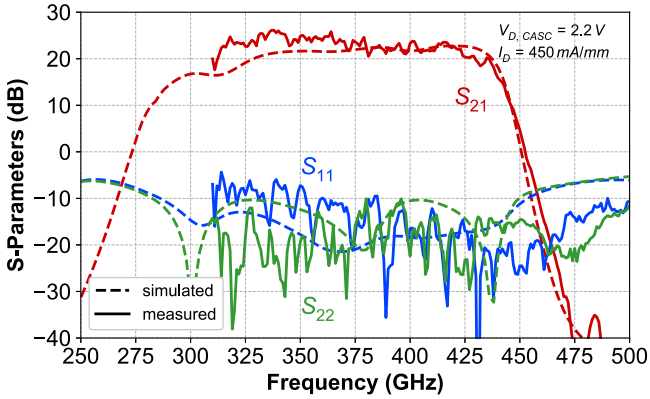


Fig. 15. Measured versus simulated S-parameters of the 128-μm TGW PA, WR-2.2.

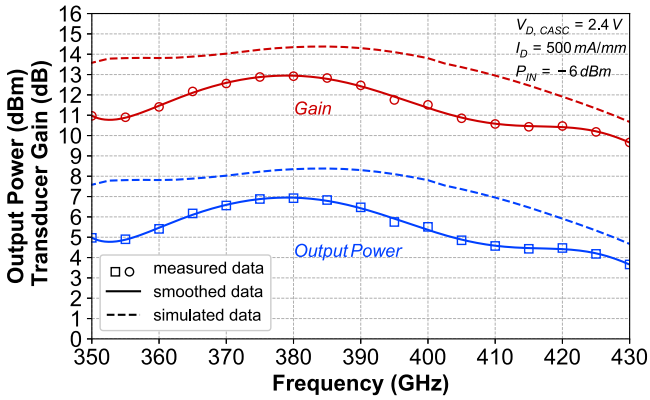


Fig. 16. Measured versus simulated output power over the operating BW of 350 to 430 GHz.

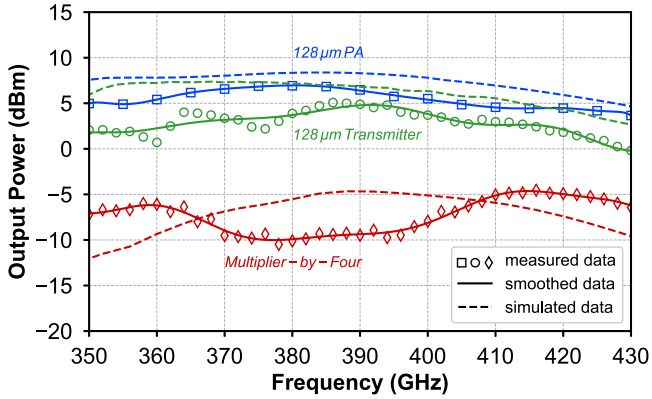


Fig. 17. Measured versus simulated output power over the operating BW of 350 to 430 GHz, at an input drive of −5 dBm, for the transmitter and x4, depicted against the PA's output over the BW as wells as accompanying x4 simulations.

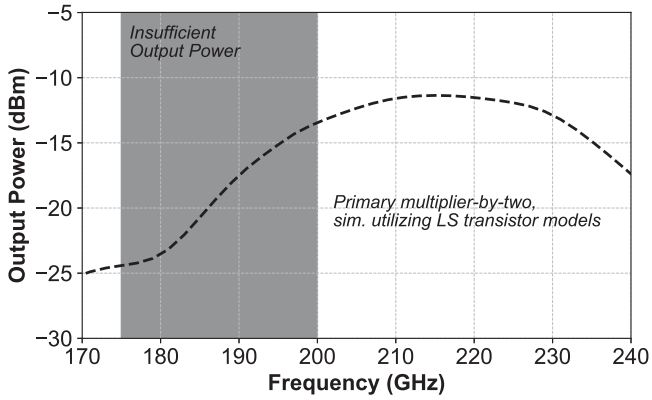


Fig. 18. Resimulated output power of the first doubler and buffer MPA in the x4 chain.

depicted in Fig. 16, measured over a BW from 350 to 430 GHz. The difference between the small-signal gain of about 22 dB and the transducer gain of 13 dB at 380 GHz, taking into consideration the compression level of the PA, is affected in part by the differing bias points between the small-signal and large-signal measurements. For the small-signal measurement, a drain voltage of 2.2 V is applied with a max drain current of 450 mA/mm, over the complete drain gate finger width. Since only the introduced cascode topology is utilized, the drain voltage applied is split between the CS and the CG HEMTs evenly, thus 1.1 V per device, while the absolute drain current is normalized over the total gate finger width connected to the main drain-source bias, here 544 μm.

With regard to the large-signal measurement, the PA is biased at a drain-source voltage of 2.4 V, with a drain current of 500 mA/mm. Looking at the output power over the operational BW of 350 to 430 GHz, a peak performance of 7 dBm is observed at 380 GHz, seen in more detail in Fig. 16. The measured power-added efficiency (PAE) is 0.6%. The input drive lies at −6 dBm. An output power of greater or equal to 4 dBm is observed for a BW of around 80 GHz. Compared to the simulations, a discrepancy of 1 to 3 dB is observed, over the complete BW, for both the output power and transducer gain. This is in part due to the nonideal layouting of the resistor within the Wilkinson combiners/dividers and an increased amount of losses over the matching structures, then expected. In the coming Section VII-E, the improved layouting and compacter matching structures reduce this discrepancy significantly.

B. Multiplier-by-Four and Transmitter, Measurements versus Partial Simulation

Presented in Fig. 17, is the measured output power of the transmitter, x4, and the respective simulations. As a benchmark comparison, the output power of the PA is plotted alongside its simulation as well. Yet again, the discrepancy between the simulated and measured output power of the transmitter, as in the case the amplifier, is around 1 to 3 dB. Being processed within the same run, they both suffer from the same aforementioned deficits.

Furthermore, to understand the output of the transmitter, in more detail, one has to carefully observe the performance of the x4. Depicted in Figs. 17 and 18, is the simulated output power of the desired fourth harmonic of the complete x4 chain and that of the second harmonic through the first doubler with its respective WR-5 buffer MPA. Due to the previously mentioned model short-comings, the LS model predicts a lower BW while the output power of the fourth harmonic is expected to be much higher. This is clearly observable in the measured versus simulated behavior of the x4. With respect to the transmitter's

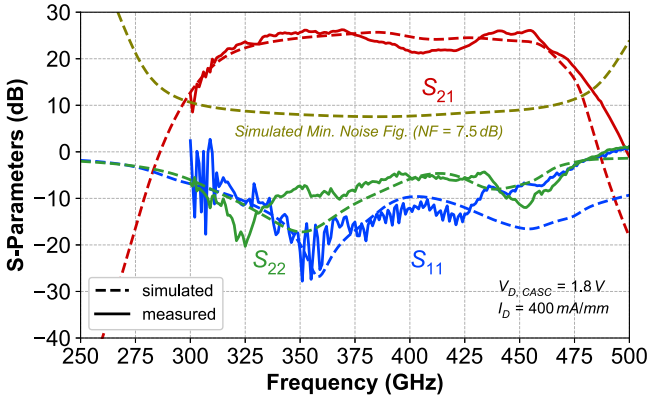


Fig. 19. Measured versus simulated S-parameters of the 16-μm TGW LNA, WR-2.2.

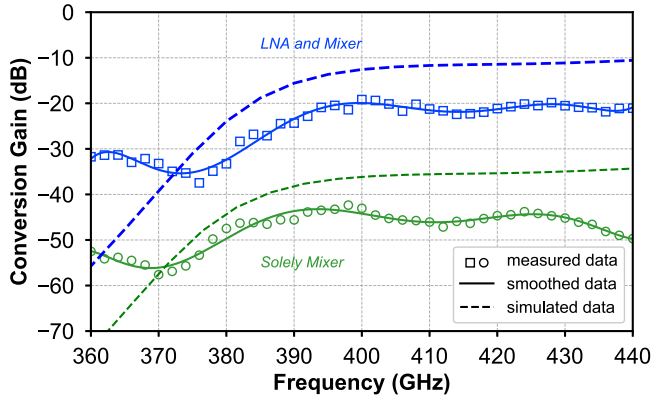


Fig. 20. Measured versus simulated conversion gain of the receiver and stand-alone mixer, versus the RF input frequency sweep.

output power, the dip of the x4's output is compensated by the peaking behavior of the PA around the frequencies of 360 to 400 GHz.

Observing the first doubler and buffer MPA, from the resimulation depicted in Fig. 18, it becomes clear that the second-harmonic output power is insufficient to drive the buffer MPA into saturation. Thus, the output of the subsequent doubler and MPA buffer is not a flat response over the desired operational BW. The wide-band response of the second doubler and WR-2.2 MPA are insufficient to compensate the first two stages, thus in Fig. 17, various dips and a drop of around 2.5 dB are observed in the output of the complete transmitter chain as compared to the results of the 128-μm PA. This is in part, due to the insufficient drive power provided by the x4, as well as due to the respective load targets shifting once the individual components are integrated into a one-chip solution. Nonetheless, the fully-integrated on-chip transmitter maintains its broadband performance and delivers output-power over BW comparable to the state of the art.

C. WR-2.2 LNA, Measurements versus Simulation

As one of the main components of the receiver chain, the LNA presented in Fig 9, with its respective S-parameter measurements versus simulation—including the simulated NF—displayed in Fig. 19, is based on the exact design approach as highlighted in Section III. However, the capacitor at the CG device of the utilized cascode is increased, resulting in a higher small-signal gain. The LNA is designed to cover a large portion of the WR-2.2 band, such that even as a singular component, it can find versatile usage packaged in a split-block module, similar to what is seen in [23]. Referring to Fig. 19, the LNA has a 3-dB BW of 150 GHz, starting from 315 to 475 GHz, with an average small-signal gain of 23 dB and a minimum NF of 7.5 dB. The NF was extracted from simulations only, with CST-simulated matching structures and ADS-based transistor models. The operating conditions were approximated via adjusting the device's channel temperatures. Since measuring the NF on-wafer for the WR-2.2 band is highly nontrivial and currently not feasible, the strong overlap between the simulated S-parameters and the measured ones, should sufficiently indicate that the presented NF is of a reasonable range. The explicit measurement of the NF with a split-block based approach is possible, yet goes beyond the scope of this particular paper.

D. Mixer and Receiver, Measurements versus Simulation

The remaining part of the receiver chip, is composed of a Lange coupler and the subharmonic mixer. The measured conversion gain of the mixer, with either the aforementioned LNA amplifying the received RF signal or a variant without it, and the respective simulation of the conversion gain of the complete chain is depicted in Fig. 20, plotted against the swept-RF signal frequency. The measurements are acquired with an IF frequency of 5 MHz. Regarding the latter, increasing the IF frequency to 1 GHz results in a conversion-gain drop of 3 dB. With the provided LO signal coming from the same doubler and buffer MPA combination as in the first two stages of the x4, the performance over the complete BW is restricted by the driving power of the second harmonic. Due to the splitting of the LO signal via a Wilkinson divider, and the consecutive input matching network for the respective I and Q subharmonic mixer cells, the delivered power is insufficient, thus there is a 10-dB difference between the measured conversion gain and the simulated one, considering the resimulation as depicted in Fig. 18. Subharmonic mixers are sensitive with regard to the LO drive. Since the measured LO drive is non-ideal, the conversion gain is hampered, yet it is to be observed that the performance remains broadband, with the 20 to 25-dB gain from the LNA present in the respective case. The operational BW of the receiver chain is from 390 to 440 GHz.

The I and Q split of the RF signal is achieved through a Lange coupler, which commonly suffers from either over- or under-coupling, resulting in a slight amplitude difference of around 1.5 dB between the low-pass filtered I and Q components. Depicted in Fig. 21, is a Lange-coupler test field, utilized in the respective characterization. The RF-probe reference plane sits at the on-chip RF-pads, thus the aforementioned open-stub effect, as well as the MSL extension to the actual structure have a large influence in the insertion loss and respective reflection coefficients.

As can be viewed in Fig. 22, the measured transmission from the "input" to the "through" port, is around 5 dB. This indicates

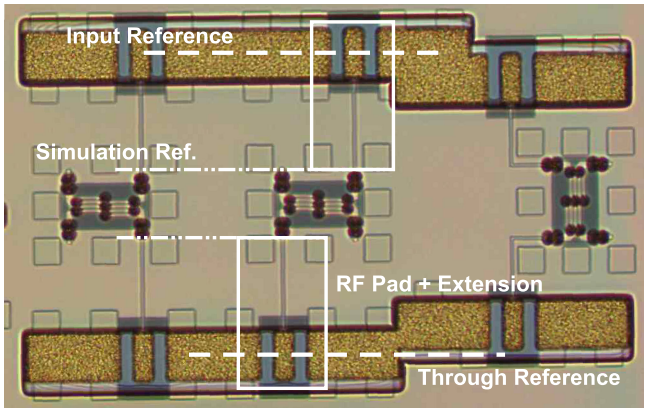


Fig. 21. Microphotograph of the WR-2.2 Lange-coupler test field.

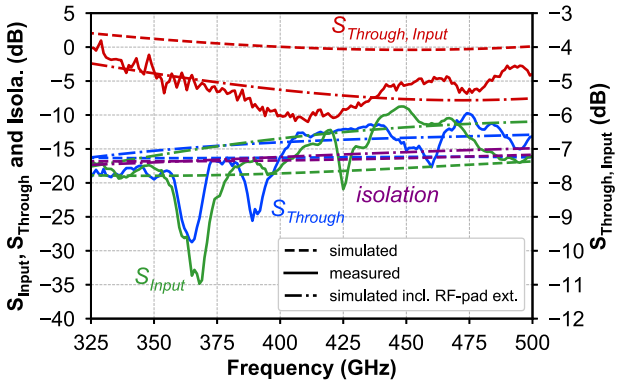


Fig. 22. Measured versus simulated S-parameters of the Lange coupler.

an approximate 2-dB transmission loss, 1.5-dB greater then the original simulation, which referenced itself directly at the ports of the Lange coupler, ignoring the RF pads and MSL extensions. Once the exact structure is resimulated with the latter included in the simulation, the transmission losses become apparent. Thus, follows that for the WR-2.2 frequency band, the losses over an on-chip RF-pad and respective 100-μm MET2 MSL extension total to an average 1.5 dB, or 0.75 dB per side. In this case, the ports are labeled as "input" and "through." What is nontrivial is the resimulation of the respective input/output reflection coefficients. However, from the overlap of the transmission results, it can be deduced that the cut-off seen around 430 GHz is due to the influences of the RF probes and the respective RF pad and MSL extension, considering that in the measurement of the complete receiver, such a breakdown in performance is not observed.

E. Updated Multiplier, Transmitter and Receiver Design

The highlighted deficits of the initial x4 design are improved upon in this subsequent iteration. Furthermore, improvements are made in the large-signal performance of the respective 128-μm PA. Thus, the updated transmitter chain displays significant gains in the achieved BW and output power. The latter is depicted in Fig. 23.

Concerning the updated x4, the two-finger transistor of the initial dobuler stage is interchanged from a device with a TGW of 30 μm to one with a TGW of 42 μm. This, results in a larger second harmonic drive for the subsequent WR-5 buffer MPA. The latter is upgraded with a second stage cascode, with an updated interstage matching, resulting in an increase in the output power drive over the operating BW, such that the input drive for the second multiplier-by-two is sufficient, for it to deliver a large BW performance.

For the updated WR-2.2 PA, the matching networks are adjusted following acquired insight from resimulation and subsequent iterative design alterations. Namely, the matching networks are adjusted to be more compact and the load transformation targets are skewed closer to what is expected from the measurement. Plainly said, the simulated matching networks were altered until the harmonic balance simulation corresponded to the initial measurements. Thus, the simulated load targets adhered more to what was expected form the device under test. Knowing this particular state, slight changes to the L-C networks enabled the design to perform as anticipated in the initial simulations. This can be viewed in Fig. 24, where the large signal simulation of the complete chain fits the on-wafer measurements, with only a slight discrepancy in the 3-dB BW.

The biasing network and the respective Wilkinson dividers/combiners are designed in a more compact form, particularly the layout of the latter is improved to reduce losses in the added electrical length of the respective thin-film resistors. The latter, results in lesser insertion losses. These changes allow for the complete chip to reduce in size, as well as for the integrated PA to feature the complete stage-to-stage topology as seen in Fig. 5, with the included iterative changes. The respective measurements of the output power and transducer gain of the updated transmitter, in a frequency range from 330 to 440 GHz and input drive of -2 dBm, can be seen in Fig. 24. Measured at a biasing of $V_{\text{D-CASC}} = 2.2$ V and $I_{\text{D}} = 500$ mA/mm, a peak output power of 9 dBm at 350 GHz and a 3-dB BW from 335 to 425 GHz, is observed. A total operating BW of 90 GHz or 23.6% relative BW, is achieved. The measured PAE of the complete transmitter is 0.7%, with a required dc power of 770 mW, or 2.2 V and 350 mA.

In Fig. 25, the output versus input power of the updated transmitter is plotted, under the aforementioned biasing conditions. Apparent become the nonlinear characteristics of the updated x4, driving the integrated PA. The updated x4 delivers sufficient driving power over the complete operating BW, provided that an input power of -6 to -2 dBm is seen at the input of the x4. The simulated output power of the first to the sixth harmonic of the updated x4, including the measurement of the fourth harmonic, is depicted in Fig. 26. The suppression of the third and particularly the fifth harmonic is less ideal below the 340-GHz mark. Thus when comparing the PA performance on its own with that of the transmitter, the performance of the former has a larger simulated and measured response as the input signal does not contain said harmonics. The measurement, in terms of the transmitter output power, slightly shifts the simulated 340-GHz frequency point by 10 GHz, to a value closer to 330 GHz. As previously mentioned, and as can be seen in Fig. 24, the LS model gives a more restricted prediction in both the upper and the lower 3-dB point.

With all the presented designs in this article, the biasing-point for the optimal large signal performance, slightly varies between

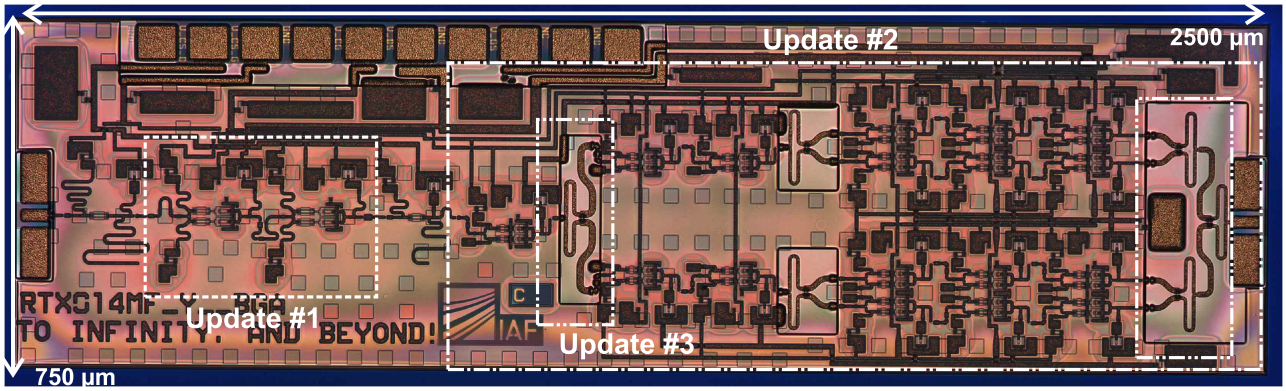


Fig. 23. Microphotograph of the updated and improved transmitter.

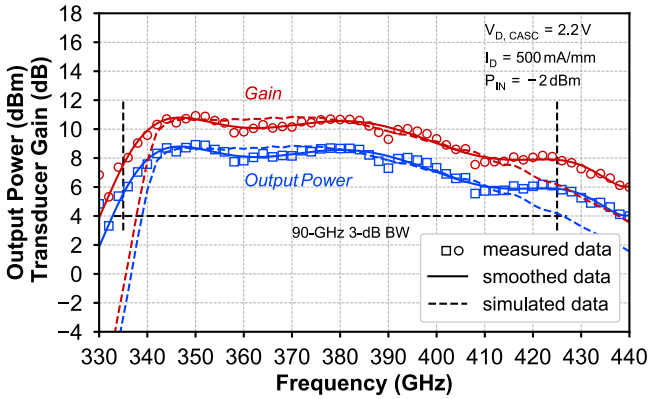


Fig. 24. Measured versus simulated output power and transducer gain of the updated transmitter design.

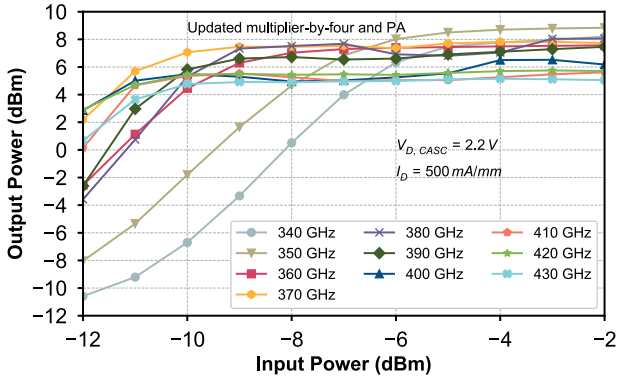


Fig. 25. Measured output power plotted against the input of the transmitter. Apparent becomes the output characteristic of the updated multiplier.

the different runs. The simulations are adjusted to run with the biasing utilized in the corresponding measurements.

The updated receiver is depicted in, Fig. 27, where the one significant design change is the integration of the improved x2. To remain within the same chip area as the updated transmitter, the Wilkinson divider, necessary for splitting the LO signal for the IF-Q and IF-I path, is inverted 90° to compensate for the longitudinal size increase of the updated x2.

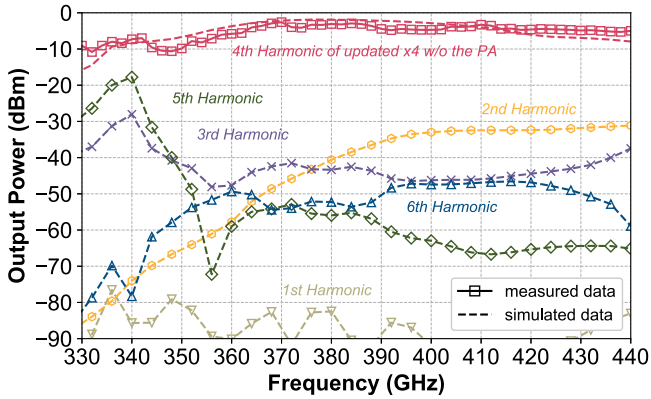


Fig. 26. Output power of the first to the sixth harmonic of the updated multiplier-by-four without the PA.

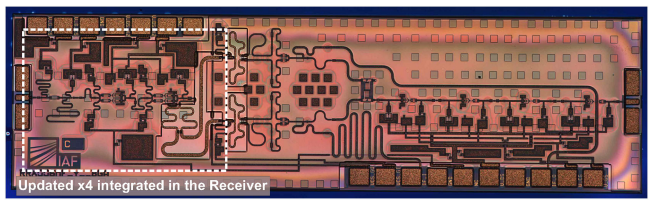


Fig. 27. Microphotograph of the updated receiver. Note: "x2", not "x4".

Compared to the previous results, the measured conversion gain of the updated design, depicted in Fig. 28, displays a maximum conversion gain of −7 dB at 370 GHz, with a 3-dB BW of 340 to 410 GHz and respective 10-dB BW of 335 to 420 GHz. The simulated behavior over the operating BW also fits the measurements quite well. In both cases an LO drive of −2 dBm is utilized, with an RF signal of −35 dBm. The IF frequency is at 5 MHz. The required dc power is 150 mW, or 1.8 V and 83 mA. This represents an improvement of greater than 10 dB, as well as an absolute BW increase of 20 GHz. For the operating frequencies, the realized conversion gain of −7 to −10 dB within a relative BW of 18.6%, represents a performance comparable to the state-of-the-art, setting it with regard to the BW. Comparing it to the simulation results depicted in Fig. 20, it can be concluded that the changes made to the x2 resulted in

TABLE I
WR-2.8, WR-2.2 AMPLIFIER AND TRANSMITTER[‡] S-MMICS[♣] AND MODULES[♠]

Technology	S_{21} *3-dB BW* (GHz)	S_{21} *max* (dB)	*Large-Signal Range* (GHz)*	P_{out} *in saturation* (dBm)	*Transducer gain* (dB)	*Power-added efficiency* (%)	*TGW* (μm)	*Ref.*
SOI CMOS	-	-	374–407	-10	-20	-	-	[24]$^{‡}_{\Upsilon}$
SOI CMOS	-	-	395–435	-7	-22	-	-	[25]$^{‡}_{\Upsilon}$
SiGe BiCMOS	-	-	340–385	-12–0	-	-	-	[26]$^{‡}_{\Upsilon}$
SiGe BiCMOS	-	-	317	4.8	-	-	-	[27]$^{‡}_{\Upsilon}$
InP HBT	360–390	22	385	-8.8	9.2	0.05[†]	4[⊐]	[28][♣]
InP HBT	325–340	16.6	325–340	8.6–12.6	3–7	1.09	160[⊐]	[29][♣]
InP HEMT	330–345	14.6	338	10	3	0.7–2[†]	160	[30][♠]
InP HEMT	460–485	14.7	-	-	-	-	14	[31][♠]
InP HEMT	300–390	19	385–423	6–8.4	3	0.3–0.4[†]	120	[32], [33]$^{♠}_{§}$
InP HEMT	469.5–482.5	20	460–490	-3 – -1	-	-	80	[34]$^{♣}_{§}$
InGaAs mHEMT	426–458	14	424–464	-8	-	-	10	[35]$^{♣}_{§}$
InGaAs mHEMT	433–465	16.1	-	-	-	-	10	[23][♣]
InGaAs mHEMT	280–310	19	280–310	6.7–8.3	12.5–14	0.8–1.3[†]	160	[16][♣]
InGaAs mHEMT	280–320	19	280–320	6.8–8.6	11.5–13.5	2.1	128	[18][♣]
InGaAs mHEMT	280–322	26	284–320	9.6–13.7	11.5–13.8	0.8–2.4	512	[20][♣]
InGaAs mHEMT	280–430	20	355–395	1.5–3.3	16–18	1.0–1.5	32	[21][♣]
InGaAs mHEMT	315–440	22	350–430	4–7	10–13	0.3–0.6	128	PA-1[♣]
InGaAs mHEMT	-	-	360–420	2–5	7-10	0.2–0.3	128	TRX-1$^{♣}_{‡}$
InGaAs mHEMT	-	-	335–425	6–9	8–11	0.5–1.0	128	TRX-2$^{♣}_{‡}$
InGaAs mHEMT	315–475	23[Ψ]	-	-	-	-	16	LNA-1[♣]

§: Last buffer amplifier considered in a multiplier chain.
*: Frequency range over which large-signal measurements are acquired.
[†]: Calculated from in-text provided and from graphs' read-out values.
LNA: Low-Noise Amplifier, PA: Power Amplifier, TRX: Transmitter (Multiplier-by-Four + PA).
[Ψ]: Respective minimum noise figure of 7.5-dB, acquired via SIMULATION only.
[ϒ]: Transmitter with an integrated antenna solution. The performance of the active chain is regarded only.
[⊐]: Total emitter length with regard to the HBT.

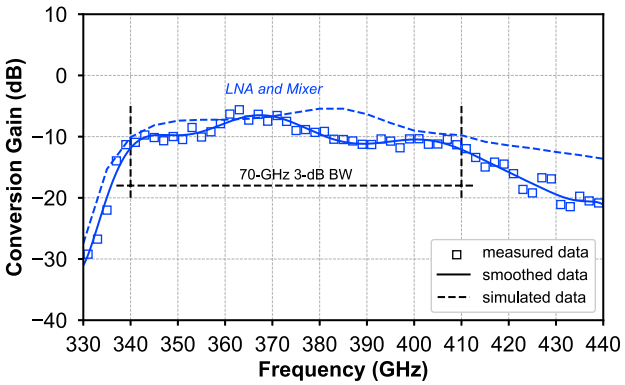


Fig. 28. Conversion gain of the updated receiver.

a sufficient drive for the subharmonic mixer, thus reducing the overall losses.

VIII. STATE OF THE ART

A comparison of the most recently published results within the WR-2.8 and WR-2.2 waveguide bands, with regard to amplifier- and transmitter-performance figures, is portrayed in Table I. The state-of-the-art of four semiconductor technologies is compared. In the case of the CMOS and SiGe solutions, which all include an integrated antenna, solely the performance of the respective active chain is considered. Since such a comparison might present a technical conundrum, the included examples serve an intent of information-completion only. The listed devices are either amplifiers or complete transmitter chains, in either S-MMIC form with accompanying on-wafer measurements, or module form—meaning they are assembled and packaged, with respective measurements performed beyond an on-wafer environment. Starting with the amplifiers, the 128-μm PA presented in this work, boasts a state-of-the-art performance when considering output power over the operating large-signal BW in WR-2.2, with a span of 4 to 7 dBm over a range from 350 to 430 GHz. The initial transmitter design, labeled in Table I as "TRX-1," due to the lacking LO drive from the initial doubler stage, presents a constricted output power and operating BW, with 2 to 5 dBm over a range from 360 to 420 GHz. The updated transmitter chip, labeled as "TRX-2," sets the state-of-the-art in terms of output power over the operating BW of 6 to 9 dBm for a frequency span from 335 to 425 GHz, which represents a relative BW of 23.6%. The peak-output power of 9 dBm is recorded at

TABLE II
SUBMILLIMETER-WAVE MIXERS AND RECEIVERS

Technology	*Type of Mixer*	*3-dB BW* (GHz)	*Conv. Gain* (dB)	NF_{SSB} (dB)	*Ref.*
SOI CMOS	Fund-harm. (1^{st})	240–300 *10-dB BW* (240–320)	-30	23	[36]
SOI CMOS	Single-balanced (1^{st})	335 *Single meas. pt*	-10.2	23.2	[37]
SOI CMOS	Sub-harm. (3^{rd})	278–304	-16.5 *mixer Conv. Gain*	-	[38]
SiGe BiCMOS	Fund-harm. (1^{st})	324–348† *10-dB BW* (305–375)	12.6$^{*}_{\dagger}$	22.7	[26]
SiGe BiCMOS	Sub-harm. (2^{nd})	465–495† *10-dB BW* (450–500)	-12.5 – -7.5	33	[39]
InP HEMT	Fund-harm. (1^{st})	290–300† *10-dB BW* (270–305)	3	15.04	[40]
InGaAs mHEMT	Sub-harm. (2^{nd})	215–255 *10-dB BW* (212–268)	10	7.0	[3]
InGaAs mHEMT	Sub-harm. (2^{nd})	390–440 *10-dB BW* (380–440)	-20	8.5§ *LNA–NF* (7.5§)	RRX-1
InGaAs mHEMT	Sub-harm. (2^{nd})	340–410 *10-dB BW* (335–420)	-7	8.5§ *LNA–NF* (7.5§)	RRX-2

§: Acquired through SIMULATION only.
*: Without the provided lens and antenna gain of 15.4-dB.
†: Extracted from in-graph provided information.
RRX-1 and -2: Presented receiver, LNA and subharmonic mixer included.

350 GHz, for a device parrallelized to reach 128 μm of finger width at the output. The presented LNA, boasts the largest gain over 3-dB BW, with 20 to 23 dB over a range from 315 to 475 GHz, a relative BW of 40%. The simulated minimum NF lies at 7.5 dB. The presented transmit and receive chips are designed to be integrated with respective on-chip antennas and mounted on carrier boards, rather then be placed in waveguide split-block modules. A measurement of the NF was at this time not possible.

Table II, shows a comprehensive list of current state-of-the-art receivers and mixers in the sub-mmW regime, namely around the 300-GHz-and-above mark. Due to the previously noted lack of sufficient LO drive over the desired frequency BW, caused by the initial x2 design under-performing, the conversion gain suffers and fails to reach the simulated results. However, the operating BW of 50 GHz with a low single side band NF (NF_{SSB}) of 8.5 dB—acquired through simulation only—indicate the benefits of broadband and low-noise receiver designs in the chosen 35-nm InGaAs mHEMT technology, when compared to the much higher noise figures of SiGe and the BW-over-conversion-gain limitations of CMOS. The updated receiver design benefits from the sufficient LO drive, resulting in a conversion gain of -7 to -10 dB over a BW from 340 to 410 GHz, thus setting the state of the art with a relative BW of 18.6% for S-MMIC based solutions of the presented integration level. For this particular implementation, the conversion gain can always be improved upon, by increasing the number of gain stages of the integrated LNA.

IX. CONCLUSION

This article describes the design and implementation of 400-GHz transmitter and receiver S-MMICs, implemented utilizing Fraunhofer IAF's 35-nm InGaAs mHEMT technology. The individual components of the respective transmitter and receiver are presented as well, with a multiplier-by-four and PA for the former, and a subharmonic mixer and LNA for the latter. The designs are all realized utilizing TFMSLs on a three-metal layer stack.

Each individual component of the transmit or receive chain is designed with compactness in mind, aiming at achieving the largest operational BW in the respective operating frequency band of WR-2.2. The measured output power of the transmitter chain varies from 6 to 9 dBm over an operating BW from 335 to 425 GHz. To the best knowledge of the authors, this represents the state-of-the-art in terms of output power and 3-dB BW in the WR-2.2 frequency band. The integrated PA contains four gain and two buffer stages, there to compensate for the insertion losses of the Wilkinson combiners/dividers. The output TGW is 128 μm and the recorded peak output power is 8 mW. The final chip size sits at $750 \times 2500\,\mu\mathrm{m}^2$, including biasing and RF pads, as well as the redundant remains of the chip frame. The receiver chain, with a final chip size of $750 \times 2500\,\mu\mathrm{m}^2$, boasts an LNA with a maximum gain of 23 dB and 3-dB BW from 315 to 475 GHz, or a relative BW of 40%. To the best knowledge of the authors, this is the largest gain-over-BW combination observed in the WR-2.2 frequency band. The subharmonic mixer is heavily dependent on the LO drive. The initial design of the multiplier-by-two provides insufficient driving power. Thus, the conversion gain suffers and the operating BW is restricted due the LO signal subsequently being frequency limited. This is improved upon in a subsequent iteration of the multiplier-by-four, included in the paper, which makes use of the multiplier-by-two found in the receiver chip. The updated design results in a state-of-the-art 3-dB BW from 340 to 410 GHz, or relative BW of 18.6%. The single-side-band noise figure of 8.5 dB—acquired solely via simulation with reasonable real-world operating conditions taken into consideration—represents values competitive with the current state of the art.

To sum up, this work includes the modeling, design, simulation, and characterization of broadband 400-GHz 35-nm mHEMT transmit and receive S-MMICs, realized for the first time, utilizing solely TFMSLs, in a high-integration level, in the mentioned technology and at the WR-2.2 frequency band, setting the general state-of-the-art with many of its components, such as the updated transmitter and receiver, as well as the stand-alone PA and LNA.

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