A CMOS Fully Integrated 860-GHz Terahertz Sensor

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***Abstract*—This paper proposes a CMOS fully integrated 860-GHz terahertz (THz) sensor. The sensor integrates a single-NMOS THz detector, a low-noise chopper instrumentation amplifier and a high-resolution $\Delta\Sigma$-ADC. The detector consists of a novel on-chip grounded patch antenna and a source-feeding NMOS field-effect transistor (FET) of the minimum size. A microstrip transmission line is designed to improve the power transfer efficiency between the antenna and the NMOS transistor. A notch filter is proposed to improve detector performance. To enable the theoretical analysis of the operation of the THz detector and the formulation of design guidelines, we propose a THz-FET device model in which a source-coupled FET for THz detection is modeled as a dc voltage source with a resistor. The model indicates that an FET with the minimum physical dimensions for a given CMOS process can produce the maximum output signal. The sensor is implemented in a 180-nm standard CMOS process. The detector achieves a voltage responsivity of 3.3 kV/W and an NEP of 106 pW/Hz$^{1/2}$ at 860 GHz. The sensor noise and the readout circuit noise are 10.81 and 2.03 μVrms, respectively. The sensor obtains clear raster-scanning transmission images under continuous THz illumination.**

***Index Terms*—ADC, CMOS, continuous wave, notch filter, readout circuit, submillimeter wave, terahertz (THz) detector, THz device model, THz imaging, THz sensor.**

I. Introduction

TERAHERTZ (THz) waves refer to electromagnetic radiation that lies in the frequency interval from 0.3 to 3 THz, between the ranges corresponding to millimeter waves and far-infrared light. THz waves can penetrate materials such as plastic, wood, or paper sheets, and consequently, THz imaging techniques are widely applied in security checks [1]–[3] and nondestructive quality control [4]. Compared with X-ray imaging, THz imaging is safe for biological tissues because of the low photon energy of THz radiation. Compared with millimeter-wave imaging, THz imaging can achieve a higher resolution because of the relatively short wavelength of THz radiation. Since THz waves can interact with various chemical and biological materials, THz absorption can be used in many applications, such as cancer detection, explosives detection [5], biological analysis [6], and material analysis [7]. Although their possible applications appear promising, THz circuit blocks have proven difficult to build. One of the obstacles is the lack of low-cost and extensively integrated detectors to enable the construction of low-cost, small-volume video-rate imaging systems.

Several THz detectors based on high-electron-mobility transistor technologies have been demonstrated [8]–[13]. Although they exhibit high sensitivity, it is difficult to integrate such a detector and signal processing circuits on a single chip. By virtue of its advantages of low cost, high yield, and easy integration, CMOS technology is emerging as an alternative to other technologies. In recent years, considerable progress has been achieved with regard to CMOS THz detectors [14]–[25]. Detectors based on Schottky diodes [14]–[16] and field-effect transistors (FETs) [17]–[25] have been implemented using CMOS technology. In CMOS FET-based detectors, transistors are directly combined with antennas. The performance of such a detector depends on the efficiency of the signal coupling between the antenna and the transistors; therefore, a codesign procedure is important to achieve an optimal detector. The physics of FET-based detectors can be explained in terms of plasma wave theory [10], [26]–[27] or distributed self-mixing theory [17], which indicate that an FET can detect THz radiation beyond its cut-off frequency. However, none of these theories provide design guidelines regarding how to maximize the output response by optimizing the physical dimensions of the FET.

In a CMOS FET-based detector, the gate-source bias supply lines will influence the transistors' impedance and result in impedance mismatching between the antenna and the transistors. The influence can be diminished by adopting a two-NMOS configuration [17]–[20], [23]–[24]. However, only half of the power received by the antenna is transferred to each transistor in the two-NMOS configuration. Moreover, most detectors require an additional bias through the antenna to provide a dc path for the transistors [17]–[19], [21]–[23]. Meanwhile, most CMOS THz imaging systems typically employ mechanical raster scanning and lock-in measurement technique for the acquisition of two-dimensional (2-D) images [14]–[19], [21], [24]. Therefore, such systems are bulky and complicated. In 2012, a 1k-pixel THz video camera chip was presented [23], which can capture THz video frames without requiring the lock-in measurement technique. However, it used a two-NMOS configuration and did not include an on-chip ADC. In the future, a fully integrated THz image sensor could be a good approach in realizing video-rate THz cameras that are small in size and low in weight and power.

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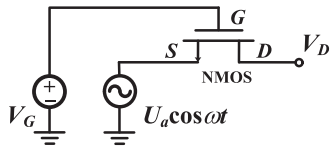

Fig. 1. Source-coupled NMOS transistor for THz detection.

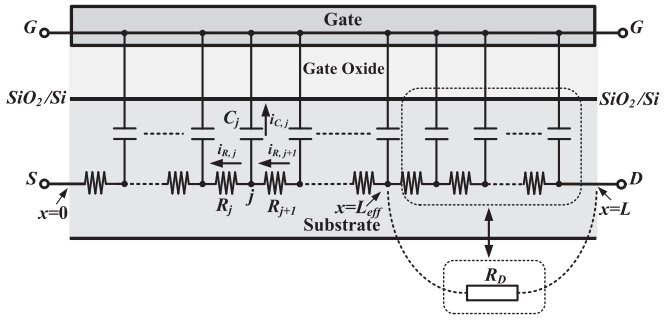

Fig. 2. Distributed resistor–capacitor network model. The NMOS channel between the point $x = L_{\rm eff}$ and the drain can be regarded as a resistor R_D.

This paper proposes a CMOS fully integrated THz sensor. Early measurements using the sensor were previously presented in [28]. The sensor integrates a single-NMOS THz detector, a low-noise chopper instrumentation amplifier, and a high-resolution $\Delta\Sigma$-ADC. The detector consists of a novel on-chip grounded patch antenna and a single source-feeding NMOS transistor of the minimum size. A microstrip transmission line is designed to achieve impedance matching between the antenna and the transistor. A notch filter is proposed to improve detector performance by eliminating the influence of the gate bias supply line. We propose a THz-FET device model in which the source-coupled drain-open FET is modeled as a dc voltage source with a resistor. The model can be used to theoretically analyze the operation of the THz detector and to formulate design guidelines for the detector. The analytical results indicate that an FET with the minimum physical dimensions for a given CMOS process can produce the maximum output signal. The sensor is implemented in a 180-nm standard CMOS process. The measurement results demonstrate that the notch filter can effectively improve the detector performance. The detector achieves a voltage responsivity of 3.3 kV/W and an NEP of 106 pW/Hz$^{1/2}$ at 860 GHz at room temperature. Clear raster-scanning transmission images are obtained under continuous THz illumination. This paper is organized as follows. Section II presents a theoretical analysis of the THz transistor. Section III describes the architecture and circuit design of the THz sensor. Section IV presents the measurement results and analysis. Section V concludes this paper.

II. Theoretical Analysis

In this section, we theoretically analyze the operation of the FET in the proposed THz detector and formulate design guidelines based on a single-NMOS configuration, as shown in Fig. 1. A THz signal $U_a\cos\omega t$ is coupled to the source of the NMOS transistor. The gate is biased to a constant potential V_G and the drain is open. The transistor is modeled as a distributed resistor–capacitor network [17], as shown in Fig. 2. The channel is divided into segments. Each segment *j* consists of a segment capacitance C_j and a variable resistor R_j, which is controlled by the local gate-to-channel voltage *V(j)*. The segment capacitance C_j represents the corresponding fraction of the total gate-to-channel capacitance that attenuates the THz signal. Since the THz frequency is much higher than the cut-off frequency of the transistor, the THz signal will be significantly attenuated. We assume that the amplitude of the THz signal is equal to zero at the position $x = L_{\rm eff}$. Under the assumption that the direction of the current is from the drain to the source, Kirchhoff's junction rule at node *j* yields

$$i_{R,j+1}(t) = i_{R,j}(t) + i_{C,j}(t). \tag{1}$$

Equation (1) indicates that the channel current *I* is a function of both *t* and *x*. For strong inversion, $I(x,\,t)$ can be approximated as [29]

$$I(x,t) = WC_{\rm ox}[V_G - V(x,t) - V_{\rm TH}]\mu_n[\partial V(x,t)/\partial x] \tag{2}$$

where $WC_{\rm ox}$ represents the total capacitance per unit length, V_G is the gate bias, $V_{\rm TH}$ is the threshold voltage, $V(x,\,t)$ is the channel potential at *x*, and μ_n is the mobility of the carrier electrons. The boundary conditions are $V(0,\,t_1) = U_a\cos\omega t_1$ and $V(L_{\rm eff},\,t_1) = 0$ at $t = t_1$. Upon multiplying both sides of (2) by *dx* and integrating, we obtain

$$\begin{aligned}\int_{x=0}^{L_{\rm eff}} I(x,t_1)dx &= \int_{V=U_a\cos\omega t_1}^{0} WC_{\rm ox}\mu_n(V_G - V - V_{\rm TH})dV \\ &= -WC_{\rm ox}\mu_n(V_G - V_{\rm TH})U_a\cos\omega t_1 \\ &\quad + WC_{\rm ox}\mu_n U_a^2(\cos 2\omega t_1 + 1)/4.\end{aligned} \tag{3}$$

There is a dc current term, $WC_{\rm ox}\mu_n U_a^2/4$. Therefore, $I(x,\,t_1)$ must include a dc part, I_1

$$I(x,t_1) = I_1 + I_2(x,t_1) \tag{4}$$

where $I_1 = WC_{\rm ox}\,\mu_n U_a^2/(4L_{\rm eff})$ and its direction is from $L_{\rm eff}$ to the source. I_1 will decrease the voltage at $L_{\rm eff}$. We assume that the voltage decreases to $V(L_{\rm eff},\,t_2) = -U_{L\rm eff}$ at $t = t_2$. Thus, we obtain

$$\begin{aligned}\int_{x=0}^{L_{\rm eff}} I(x,t_2)dx &= -WC_{\rm ox}\mu_n(V_G - V_{\rm TH})U_a\cos\omega t_2 \\ &\quad + WC_{\rm ox}\mu_n U_a^2(\cos 2\omega t_2 + 1)/4 \\ &\quad - WC_{\rm ox}\mu_n[(V_G - V_{\rm TH})U_{L\rm eff} + U_{L\rm eff}^2/2]\end{aligned} \tag{5}$$

which also includes a dc current term

$$\begin{aligned}I_1' &= WC_{\rm ox}\mu_n U_a^2/(4L_{\rm eff}) \\ &\quad - WC_{\rm ox}\mu_n[(V_G - V_{\rm TH})U_{L\rm eff} + U_{L\rm eff}^2/2]/L_{\rm eff} \\ I_1' &= I_1 - I_2\end{aligned} \tag{6}$$

where $I_2 = WC_{\rm ox}\mu_n[(V_G - V_{\rm TH})U_{\rm Leff} + U_{\rm Leff}^2/2]/L_{\rm eff}$. I_1 and I_2 depend on U_a and $U_{\rm Leff}$, respectively. We assume that when $t \geq \tau$, $I_1 = I_2$, which means that the system reaches a

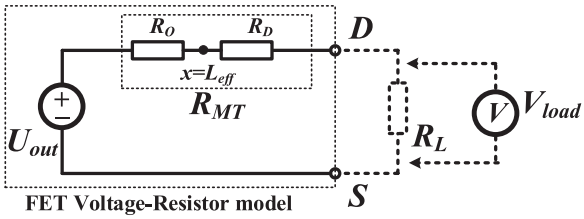

Fig. 3. The FET for THz detection can be modeled as a voltage source $U_{\rm out}$ with a resistor $R_{\rm MT}$ (THz-FET device model). $R_{\rm L}$ is a load connected to the drain.

steady state. We obtain

$$U_{\rm out} = (V_G - V_{\rm TH}) - \sqrt{(V_G - V_{\rm TH})^2 + U_a^2/2} \quad (7)$$

where $U_{\rm out}$ is the steady induced voltage at $L_{\rm eff}$. For $(V_G - V_{\rm TH}) >> U_a$ [27]

$$U_{\rm out} = -{U_a}^2/[4(V_G - V_{\rm TH})]. \quad (8)$$

The NMOS channel between $L_{\rm eff}$ and the drain can be regarded as a resistor R_D, as shown in Fig. 2

$$R_D = (L - L_{\rm eff})/[WC_{\rm ox}\mu_n(V_G - V_{\rm TH})] \quad (9)$$

which is the resistance of an NMOS transistor with a length of L–$L_{\rm eff}$ and a width of W operating in the deep triode region. Based on the above analysis, the configuration shown in Fig. 1 can be modeled as a voltage source $U_{\rm out}$ with a resistor $R_{\rm MT}$ in accordance with Thevenin's theorem, as shown in Fig. 3. $R_{\rm MT}$ is

$$R_{MT} = R_O + R_D = L/[WC_{\rm ox}\mu_n(V_G - V_{\rm TH})] \quad (10)$$

where

$$R_O = U_{\rm out}/I_1 = L_{\rm eff}/[WC_{\rm ox}\mu_n(V_G - V_{\rm TH})]. \quad (11)$$

Because the drain is open, its voltage is

$$V_D = U_{\rm out} = -{U_a}^2/[4(V_G - V_{\rm TH})]. \quad (12)$$

This result is the same as the result obtained based on the plasma wave theory [10], [27].

Next, we will discuss how to optimize the dimensions of the transistor to maximize its output signal. $U_{\rm out}$ can be rewritten as

$$U_{\rm out} = -\frac{P_{\rm acc}}{2(V_G - V_{\rm TH})} \cdot \frac{{\rm Re}(Z_m)^2 + {\rm Im}(Z_m)^2}{{\rm Re}(Z_m)} \quad (13)$$

where $P_{\rm acc}$ is the THz power that the transistor accepts and $Z_{\rm m}$ is the source input impedance of the transistor at the corresponding frequency. Equation (13) indicates that a higher value of $|Z_m|^2/{\rm Re}(Z_m)$ results in a higher $|U_{\rm out}|$.

We used the *Synopsys* TCAD simulator to qualitatively analyze the relationship between Z_m and the transistor dimensions. The *Synopsys* TCAD can perform ac analysis simulation for an NMOS device to deduce its Z_m [30]. Fig. 4 shows a simulated 2-D NMOS transistor. All process steps, such as etching, deposition, ion implantation, thermal annealing, and oxidation, were considered. Using this transistor, we extracted Z_m at 860 GHz. Fig. 5 shows $|Z_m|^2/{\rm Re}(Z_m)$ as a function of V_G for different

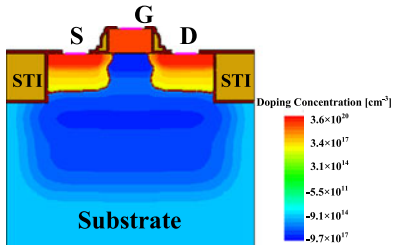

Fig. 4. Simulation result of a 2-D NMOS transistor. The different colors represent the ion doping concentrations. The shallow trench isolation (STI) process was considered in the simulation. The letters S, G, and D denote the source, gate, and drain, respectively.

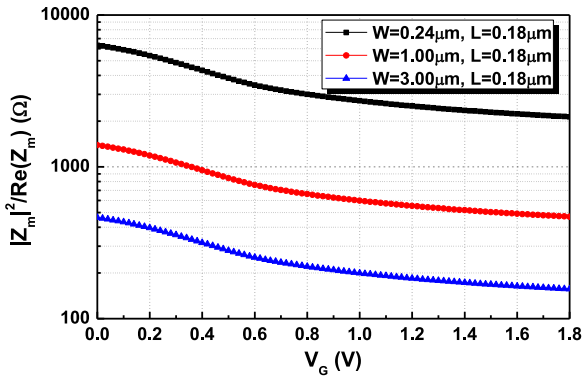

Fig. 5. $|Z_{\rm m}|^2/{\rm Re}(Z_{\rm m})$ as a function of the gate bias V_G for different channel widths W. The channel length L is fixed at 0.18 μm.

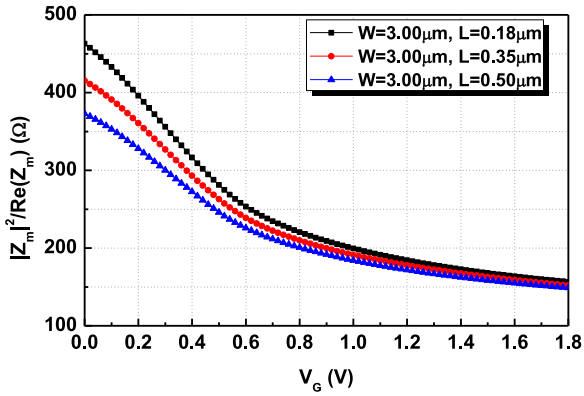

Fig. 6. $|Z_m|^2/{\rm Re}(Z_m)$ as a function of the gate bias V_G for different channel lengths L. The channel width W is fixed at 3 μm.

channel widths W. The result indicates that $|Z_m|^2/{\rm Re}(Z_m)$ increases as W decreases. This is because a smaller W reduces C_j and increases R_j in the model shown in Fig. 2. Fig. 6 shows $|Z_m|^2/{\rm Re}(Z_m)$ as a function of V_G for different channel lengths L. This figure indicates that $|Z_m|^2/{\rm Re}(Z_m)$ decreases slightly as L increases. One possible explanation is as follows. Although the THz signal is significantly attenuated by the transistor, it is difficult for it to be completely attenuated. Therefore, a longer L result in more active C_j and R_j segments, which results in a slight increase in ${\rm Re}(Z_m)$ and a decrease of $|{\rm Im}(Z_m)|$. The decrease in ${\rm Im}(Z_m)^2/{\rm Re}(Z_m)$ is greater than the increase in ${\rm Re}(Z_m)$ (according to the simulation results), resulting in a

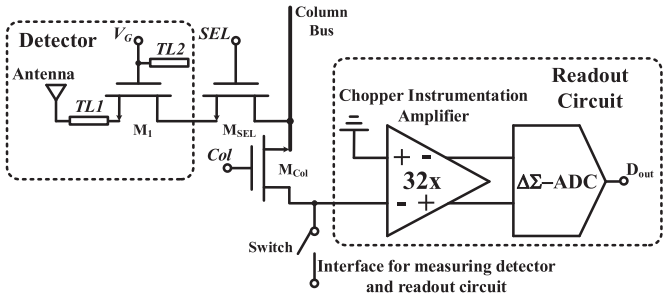

Fig. 7. Architecture of the proposed THz sensor.

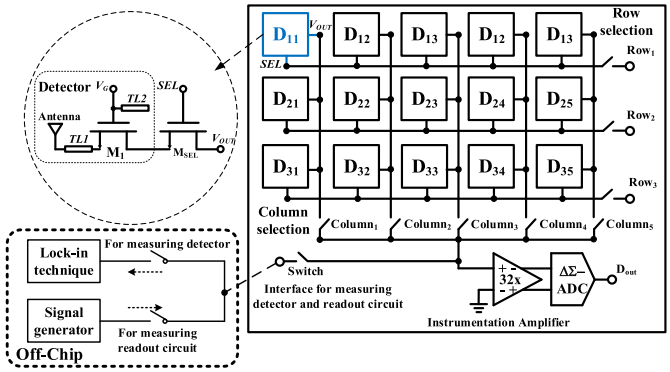

Fig. 8. Block diagram of the 3 × 5 sensor array with detectors of various sizes.

slight decrease in $|Z_m|^2/\mathrm{Re}(Z_m)$. Note that when L reaches a length at which the THz signal is completely attenuated, Z_m will become independent of L because the number of active C_j and R_j segments will no longer increase. In summary, to increase $|U_{\mathrm{out}}|$, a transistor with smaller W and L values should be chosen.

When the drain is connected to a load R_L, as shown in Fig. 3, the voltage on R_L is

$$V_{\mathrm{Load}} = U_{\mathrm{out}} \frac{1}{R_{MT}/R_L + 1}. \tag{14}$$

It is obvious that to maximize V_{Load}, we should reduce R_{MT}. According to (10), the transistor with the shortest L is the optimum choice. Note that if R_L is a capacitor or if its value is much higher than R_{MT}, then there is no need to consider R_{MT}.

The above analyses indicate that the source-coupled, nonbiased FET can be modeled as a dc voltage source with a resistor and that an FET with the minimum possible physical dimensions can produce the maximum output signal. The proposed model describes the dependence of the FET's output signal on its physical dimensions.

III. Sensor Architecture and Circuit Design

The architecture of the proposed THz sensor is shown in Fig. 7. The sensor integrates a single-NMOS THz detector, a low-noise chopper instrumentation amplifier and a high-resolution ΔΣ-ADC. The detector consists of a novel on-chip grounded patch antenna and a source-feeding NMOS transistor of the minimum size. THz radiation waves are received by the antenna and then coupled to the transistor. A microstrip transmission line, TL1, is designed to improve the power transfer efficiency between the antenna and the transistor. TL2 is a notch filter used to eliminate the influence of the gate bias supply line on the antenna–transistor impedance matching. Since the radiation power of the THz source considered in this study is low, the detector output is a small dc voltage signal with a low signal-to-noise ratio. Therefore, the signal is amplified by the chopper instrumentation amplifier. The amplifier utilizes the chopping circuit technique [31] to reduce its own offset and *1/f* noise. Finally, the ΔΣ-ADC digitizes the amplified signal.

The proposed THz sensor has the following advantages. First, it comprises a single-NMOS THz detector, a low-noise chopper instrumentation amplifier and a high-resolution ΔΣ-ADC integrated on a single chip. Therefore, it has great potential for future development into a single, fully functional THz image sensor. Second, compared with the two-NMOS detector configuration reported in [17]–[20], [23]–[24], the single-NMOS configuration offers an improved voltage responsivity. In the two-NMOS configuration, only half of the power received by the antenna is transferred to each transistor. As a result, its output is 50% less than that of the single-NMOS detector. Third, the detector includes a novel grounded patch antenna and a notch filter. The proposed grounded patch antenna does not require an additional bias line connected to the antenna to provide a dc path for the NMOS transistor. The notch filter improves the detector performance by eliminating the influence of the gate connections. Finally, a transistor of the minimum size is used as the rectifying element in the detector. The proposed THz-FET device model presented in Section II proves that a transistor of the minimum physical dimensions will produce the maximum output signal.

A. Detector Design

The proposed source-driven detector consists of an integrated on-chip grounded patch antenna and an NMOS transistor with a nonbiased channel (shown in Fig. 7). The detector's performance depends on the efficiency of the signal coupling between the antenna and the transistor. By carefully designing the TL1 geometry, the optimum impedance matching can be achieved. In this single-NMOS configuration, the influence of the gate bias supply line must be considered. The notch filter, TL2, is proposed to eliminate this influence. To achieve the optimal structure of the detector at 860 GHz, we designed a 3 × 5 array of different detectors, as shown in Fig. 8. These 3 × 5 detectors share a common readout circuit. One single detector is selected to be read out at a time. The switch at the common output is a reserved interface that is used to measure the performances of the detectors and the readout circuit.

1) NMOS Transistor: The analysis presented in Section II demonstrates that a transistor with the minimum physical dimensions can produce the maximum output signal. Therefore, we designed all NMOS transistors used in the 3 × 5 detectors to have the minimum size of 0.18 μm in length and 0.24 μm in width. The simulated source input impedance of such a transistor is shown in Fig. 9. To achieve a good match at all gate biases,

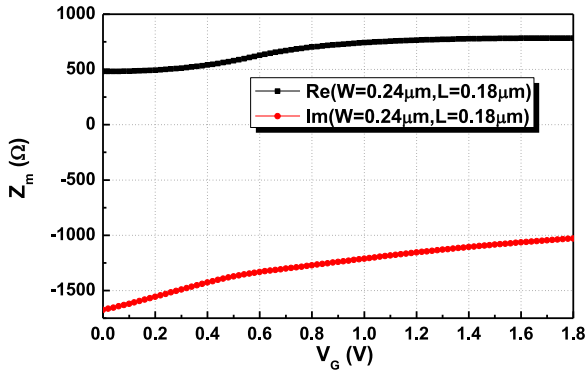

Fig. 9. Source input impedances of the NMOS transistors as a function of the gate bias V_G.

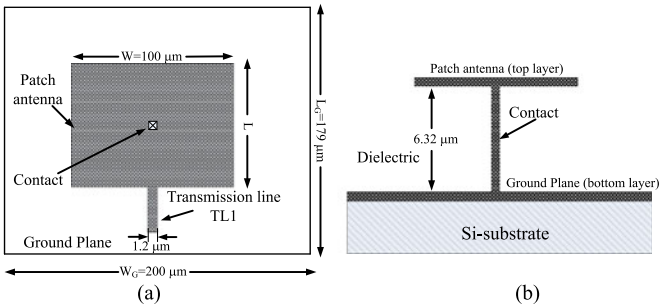

Fig. 10. (a) Top and (b) cross-sectional views of the grounded patch antenna.

the middle value of $Z_m = (632 - j1336)\,\Omega$ was chosen for the design of TL1.

2) Grounded Patch Antenna: The detector integrates a grounded half-wavelength patch antenna, as shown in Fig. 10. The patch and the ground plane are formed by the top metal layer (2.06 μm) and the bottom metal layer (0.48 μm), respectively, in the CMOS process. The thickness of the dielectric insulator between them is 6.32 μm. Since the transistor requires a dc path, a contact connecting the patch and the ground plane at the center of the antenna is designed to provide a dc ground for the source. The grounded antenna can be regarded as the ac voltage source in Fig. 1. The center of the antenna is zero-field intensity (H-plane); therefore, the contact has little effect on the electromagnetic performance of the antenna. The simulation results for antennas with and without a contact will be presented in Section III-A.3. Compared with [19], in which an additional bias line connected to the antenna is needed to provide the NMOS gate-source bias, the proposed structure does not require such an additional bias line, thus mitigating the system-level complexity for future array implementations.

3) Transmission Line TL1: To improve the power transfer efficiency between the antenna and the transistor, we designed the microstrip transmission line denoted by TL1 in Fig. 7. TL1 is implemented in the top metal layer, using the bottom metal layer as the ground plane. We designed detectors of several different antenna lengths and TL1 lengths among the 3 × 5 detectors, as listed in Table I. The widths of the antennas and TL1s in all detectors are 100 and 1.2 μm, respectively. Compared with a previously published design for a short-stub transmission line

TABLE I
CHARACTERISTICS OF THE DETECTORS IN THE 3 × 5 ARRAY

Detector	Ant./μm	[1]TL1/ μm	TL2/ μm	Out/mV	R_v / kV/W
D_{11}	67	20 + 7.3	29	3.56	3.3
D_{12}	67	23 + 7.3	29	2.41	2.1
D_{13}	67	27 + 7.3	29	1.59	1.4
D_{14}	67	30 + 7.3	29	1.53	1.3
D_{15}	62	22 + 7.3	29	2.95	2.6
D_{21}	62	25 + 7.3	20	1.22	1.0
D_{22}	67	25 + 7.3	29	1.64	1.4
D_{23}	62	25 + 7.3	29	1.84	1.5
D_{24}	62	28 + 7.3	29	1.22	1.0
D_{25}	62	25 + 7.3	25	1.47	1.2
D_{31}	62	25 + 7.3	35	2.38	2.0
D_{32}	55	25 + 7.3	29	1.29	1.1
D_{33}	65	25 + 7.3	29	1.56	1.2
D_{34}	70	25 + 7.3	29	1.91	1.5
D_{35}	75	25 + 7.3	29	1.71	1.3

TL1 is the microstrip transmission line between the antenna and the NMOS transistor. Here, the additional 7.3 μm represents the depth of the metal in stacked vias between the top metal layer and the NMOS source.

[32], [33], this proposed TL1 design can enable the transition from the low antenna impedance to a high impedance more easily.

The matching coefficient M_c, defined as the ratio of the power accepted by the NMOS transistor to the incident power from the antenna, can be expressed as follows:

$$\begin{aligned} M_C &= \frac{P_{\rm acc}}{P_{\rm inc}} \\ &= \frac{\mathrm{Re}(Z_m)}{|Z_m + Z_{\rm ANT}|^2} \Big/ \frac{1}{4\mathrm{Re}(Z_{\rm ANT})} \\ &= 4\,\mathrm{Re}(Z_m)\mathrm{Re}(Z_{\rm ANT})/|Z_m + Z_{\rm ANT}|^2 \end{aligned} \tag{15}$$

where Z_m is the source input impedance of the transistor and $Z_{\rm ANT}$ is the combined impedance of the antenna and TL1. Therefore,

$$P_{\rm acc} = P_{\rm inc} M_C = \eta J_{\rm in} A_{\rm eff} M_C \tag{16}$$

where $J_{\rm in}$ is the power density incident to the antenna, $A_{\rm eff}$ is the effective area of the antenna, and η is the radiation efficiency of the antenna. $A_{\rm eff}$ can be calculated as follows [34]:

$$A_{\rm eff} = D\lambda^2/4\pi \tag{17}$$

where D is the directivity of the antenna and λ is the electromagnetic wave length in free space.

The 3-D electromagnetic solver package HFSS was used to simulate the combined performance of the antenna and TL1. D, Z_m, and η were obtained from the simulation results. Thus, we could calculate the output voltage of the detector using (13) and (15)–(17). Fig. 11 shows the calculated output voltage versus the length of TL1. There is a relative change in value between the curves near 35 μm. The optimal lengths of the antenna and TL1 are 62 and 25 μm, respectively. For this optimal case, the simulated impedance and radiation pattern of the antenna (including TL1) are plotted in Figs. 12 and 13, respectively. $Z_{\rm ANT}$ = (966 + j629)Ω at 860 GHz, and the calculated matching coefficient is $M_C = 0.8$. The directivity is 5.36 dBi and the

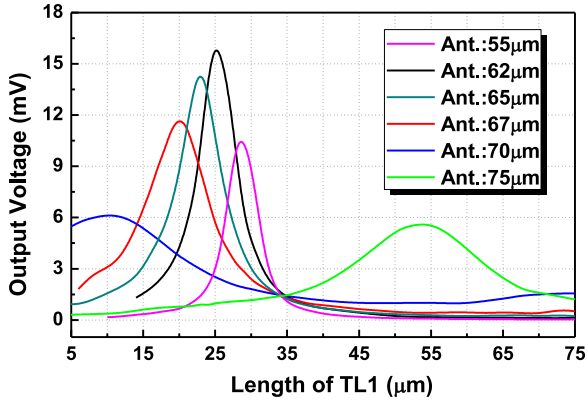

Fig. 11. Simulated output voltage of the detector versus the length of TL1 for different antenna lengths. In all case, the antenna width is 100 μm.

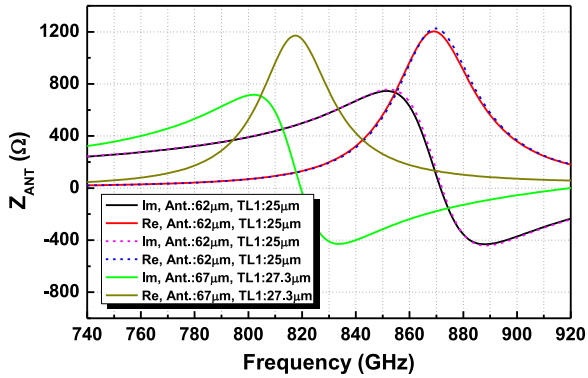

Fig. 12. Simulated impedance of the antenna (including TL1) versus frequency for different antennas. The solid and dashed lines represent antennas with and without a contact, respectively.

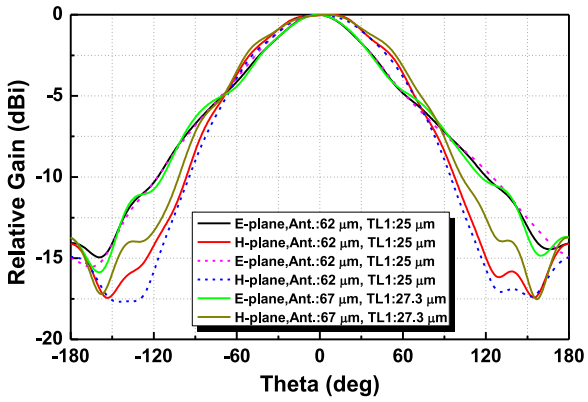

Fig. 13. Simulated E-plane and H-plane cuts of the radiation pattern of the antenna (including TL1) for different antennas. The solid and dashed lines represent antennas with and without a contact, respectively.

gain, including the conductor and dielectric losses, is 3.41 dBi for a radiation efficiency of 64%.

For comparison, the impedance and radiation pattern of an antenna without a contact are also plotted in Figs. 12 and 13, respectively. The comparison results show that the contact minimally affects the performance of the antenna.

The actual length of TL1 should include the depth of the metal in stacked vias between the top metal layer and the NMOS

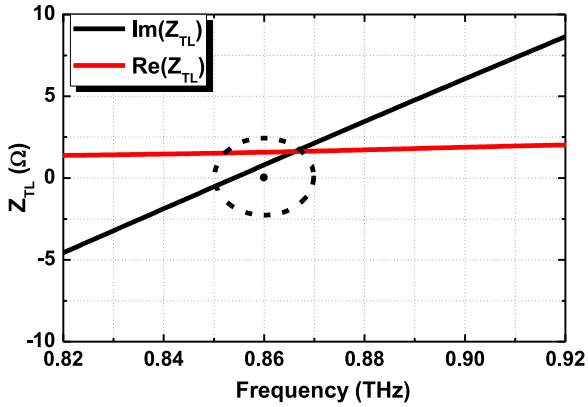

Fig. 14. Simulated impedance of TL2 as a function of frequency. The length and width of TL2 are 29 and 1.2 μm, respectively.

source. In our design, detector D_{11} shows the best-measured output voltage (see Section IV). The lengths of its antenna and TL1 are 67 and (20 + 7.3) μm (the additional 7.3 μm represents the depth of the metal in stacked vias), respectively. The impedance and radiation pattern of the antenna (including TL1) with this design are also plotted in Figs. 12 and 13, respectively. At 860 GHz, the calculated matching coefficient is $M_c = 0.16$, the directivity is 5.32 dBi, and the gain is 3.89 dBi for a radiation efficiency of 72%.

4) Notch Filter TL2: Since the gate of the transistor should be connected to a constant potential, it is typically biased directly by an off-chip voltage supply through the bonding wire, pad, and on-chip metal line. The parasitic capacitance and inductance of these components will influence the transistor's source input impedance, thereby affecting the antenna–transistor impedance matching. Therefore, the gate connections will degrade the detector performance. We designed a notch filter, labeled as TL2 in Fig. 7, to eliminate this influence. TL2 is an open quarter-wavelength microstrip transmission line. One end of TL2 is connected to the transistor gate, and the other is floating. It forms an ac ground at the corresponding THz frequency [35] and has no impact on the dc gate bias. Since TL2 and the gate bias supply line are connected in parallel, the gate always serves as an ac ground for the THz signal. Hence, the effect of the gate connections is eliminated. TL2 is also implemented in the top metal layer, using the bottom metal layer as the ground plane. Its length and width are 29 and 1.2 μm, respectively. Fig. 14 shows its simulated impedance. Both the real and imaginary parts of the impedance are close to 0 Ω at approximately 860 GHz. We designed detectors with several different lengths of TL2 among the 3 $\times$ 5 detectors, which are also listed in Table I.

B. Readout Circuit

The readout circuit consists of a low-noise chopper instrumentation amplifier and a high-resolution $\Delta\Sigma$-ADC. In terms of the readout circuit design, the key challenge is to achieve both low noise and high accuracy. The chopper instrumentation amplifier utilizes a chopping technique to reduce its own offset and *1/f* noise. The ADC used in this THz detection application requires a very high absolute accuracy and very high linearity

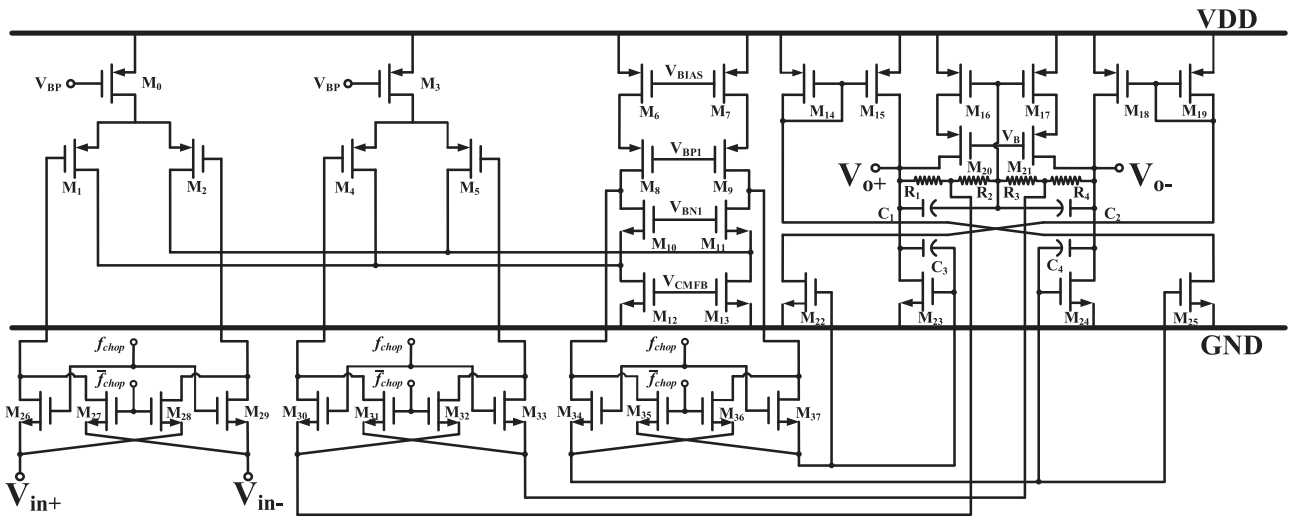

Fig. 15. Circuit diagram for the chopper instrumentation amplifier.

as well as a very low offset and very low noise. Among the available types of CMOS-integrated ADCs, a $\Delta\Sigma$-ADC seems to be the best candidate to satisfy these requirements.

1) Chopper Instrumentation Amplifier: The circuit diagram for the chopper instrumentation amplifier is shown in Fig. 15. It is a two-stage differential amplifier. The first stage has a folded configuration. It includes a PMOS input pair (M1 and M2) that provides a high input impedance. One input of the amplifier is connected to the detector output, and the other is grounded. The chopping circuit technique is applied to reduce the amplifier's offset and *1/f* noise [31]. There are three choppers, each connected to the amplifier's input, feedback loop, and first-stage output. The choppers are driven by a clock $f_{\rm chop}$. The first two choppers modulate the input signal and feedback signal to $f_{\rm chop}$, respectively. Next, the modulated signal is amplified together with the offset and *1/f* noise. The last chopper demodulates the amplified input signal back to dc and simultaneously modulates the offset and *1/f* noise to the odd harmonics of $f_{\rm chop}$, such that they will be filtered out by the subsequent circuit. This results in an amplified signal without offset or *1/f* noise. If $f_{\rm chop}$ were to be too high, the input impedance of the amplifier would be low, which would cause the voltage of the received signal to decrease, according to (14). If $f_{\rm chop}$ were to be too low, the offset and *1/f* noise would not be effectively eliminated. As a tradeoff, $f_{\rm chop}$ is chosen to be 125 kHz. The simulated closed-loop gain of the amplifier is 32.

2) Delta–Sigma ADC: The block diagram of the $\Delta\Sigma$-ADC is shown in Fig. 16. It uses a third-order cascaded integrators with feedforward modulator structure [36]. It operates for a predetermined number of clock periods and then resets itself. The modulator output is captured by an external FPGA, in which a digital decimation filter is implemented. Each integrator incorporates an operational amplifier with a two-stage cascode configuration and 120-dB dc gain. The chopping technique is also utilized in the first stage of the operational amplifier to reduce the offset and *1/f* noise. The sampling capacitor and sampling rate of the $\Delta\Sigma$-ADC are 4 pF and 500 kHz, respectively. The oversampling rate is adjustable, with a default value of 8192.

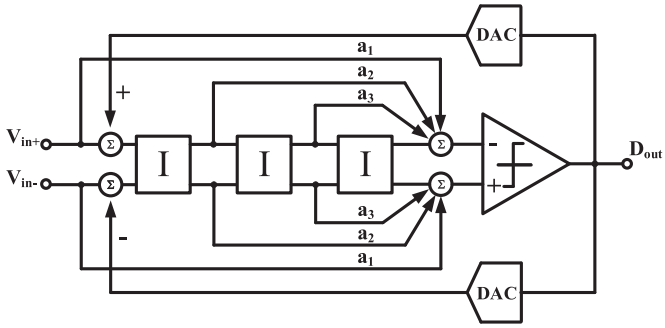

Fig. 16. Block diagram of the $\Delta\Sigma$-ADC.

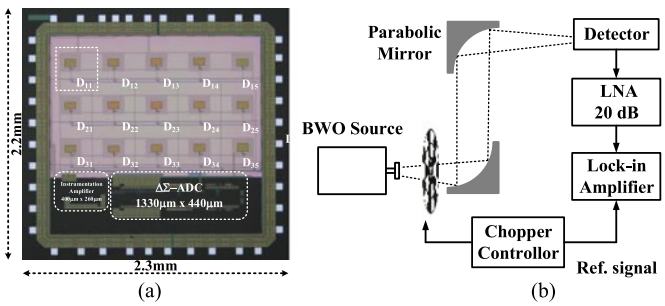

Fig. 17. (a) Die photograph of the 860-GHz CMOS THz sensors and (b) measurement setup used to characterize the detectors.

The $\Delta\Sigma$-ADC outputs a detected digital signal approximately every 16 ms in default mode.

IV. Measurement Results

The sensor was fabricated in a 180-nm CMOS process. Fig. 17(a) shows the die photograph of the 860-GHz CMOS THz sensors. The distance between detectors was designed to be approximately 200 μm to avoid coupling between adjacent antennas. The areas of the chopper instrumentation amplifier and the $\Delta\Sigma$-ADC are 400 μm $\times$ 260 μm and 1330 μm $\times$ 440 μm, respectively.

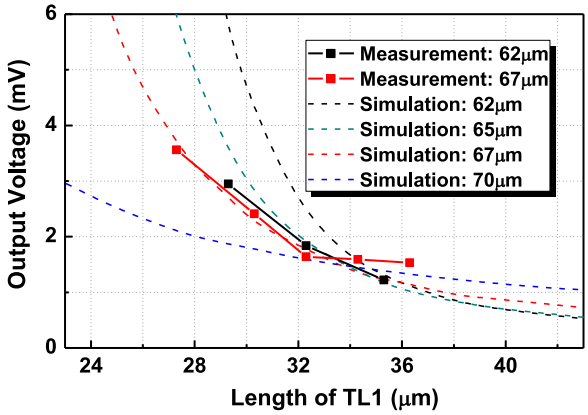

Fig. 18. Measured and simulated detector output voltages versus the length of TL1 for different antenna lengths.

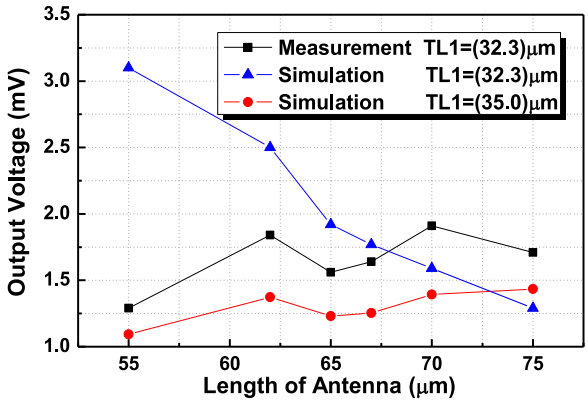

Fig. 19. Measured and simulated detector output voltages versus the antenna length. The black line is the measured result, for which the length of TL1 is $(25 + 7.3)\ \mu\text{m} = 32.3\ \mu\text{m}$. The blue and red lines are the simulated results, for which lengths of TL1 are 32.3 and 35.0 μm, respectively.

The detectors were characterized using the lock-in technique. Fig. 17(b) illustrates the measurement setup. The maximum output voltages of all detectors without external gain are listed in Table I.

The measured and simulated output voltages are plotted versus the length of TL1 in Fig. 18. They show the same general trend. The intersection of the solid red and black lines corresponds to a TL1 length of 33.3 μm, and the intersection of the dashed red and black lines corresponds to a length of 36 μm. These results indicate a difference of approximately 2.7 μm between the simulated and actual lengths of TL1.

The measured and simulated output voltages are plotted versus the antenna length in Fig. 19 for a fixed TL1 length of 32.3 μm. Considering the difference between the simulated and actual lengths of TL1, the curve corresponding to a TL1 length of 35 μm is also plotted in Fig. 19. The red and black curves show the same trend, again indicating the difference of 2.7 μm. Their nonmonotonicity can be attributed to the relative change in value between the curves in Fig. 11 near the TL1 length of 35 μm.

The measured output voltage is plotted versus the length of TL2 in Fig. 20. The output voltage markedly changes as the length of TL2 varies. This result shows that the gate supply line

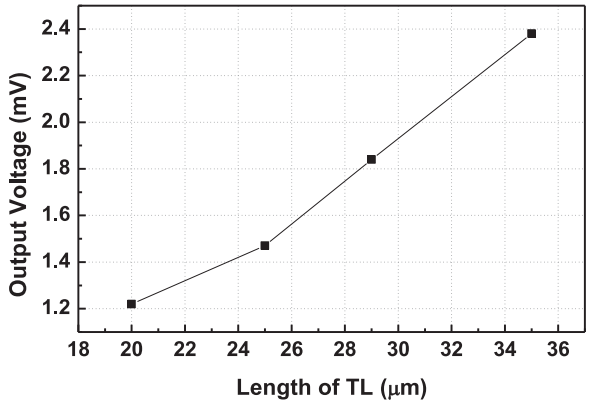

Fig. 20. Detector output voltage versus the length of TL2 for a fixed width of 1.2 μm. The lengths of the antenna and TL1 are 62 and 32.3 μm, respectively.

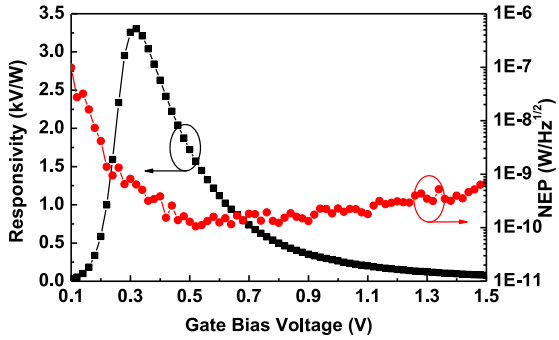

Fig. 21. Measured R_V and NEP values for detector D_{11} as functions of the gate bias voltage.

significantly affects the antenna–transistor impedance matching. It also demonstrates that TL2 can improve the detector performance. With a continued increase in the length of TL2, the output voltage would reach a peak and then drop. However, the optimal length of TL2 may not be a quarter wavelength. The exact physical model describing how the gate connections affect the transistor's source input impedance Z_m is not yet known. The purpose of the design of TL2 is simply to eliminate the influence of the gate supply line. Supposing that the model is known, Z_m can be maximized by optimizing the structure of TL2 to maximize the detector output [according to (13)]. In this case, the optimal length of TL2 may not be a quarter wavelength.

For comparison with other designs, the voltage responsivity R_V and the noise equivalent power were calculated for detector D_{11}, which exhibits the best performance. R_V is defined as the ratio between the detector output voltage and the power incident to the antenna, that is,

$$R_v = U_{\text{out}}/P_{\text{in}} = U_{\text{out}}/(J_{\text{in}} A_{\text{eff}}). \tag{18}$$

Based on (17), the calculated A_{eff} is 0.033 mm^2. The measured value of J_{in} is 32.7 μW/mm^2. Fig. 21 shows the measured R_V of D_{11}. The peak R_V is 3.3 kV/W, corresponding to a V_G of 0.32 V. The NEP is defined as the input power that results in a signal-to-noise ratio of one in a 1-Hz bandwidth [14]. The NEP values under different gate bias conditions at a modulation frequency of 177 Hz are also plotted in Fig. 21. The minimum NEP is 106 pW/Hz$^{1/2}$, corresponding to a V_G of 0.52 V. In fact,

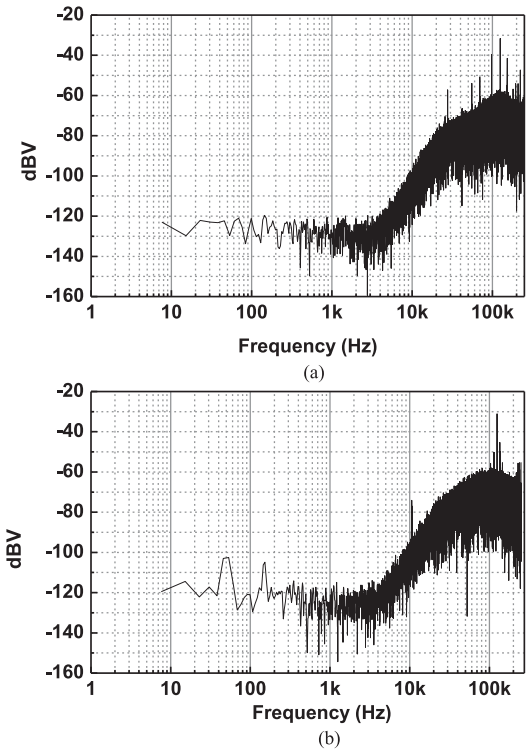

Fig. 22. (a) Measured noise power spectral density of the readout circuit and (b) measured noise power spectral density of the sensor (including the noise of D_{11}, the switches and the readout circuit).

the measured NEP includes the noise of the detector D_{11}, the row selection switch M_{SEL}, the column selection switch, and the test switch (as shown in Fig. 8); therefore, the actual detector NEP should be lower.

Fig. 22(a) shows the measured noise power spectral density of the readout circuit. When the oversampling rate of the $\Delta\Sigma$-ADC is 8192 or 1024, the readout circuit noise is 2.03 or 4.61 μVrms, respectively. Fig. 22(b) shows the measured noise power spectral density of the sensor (including the noise of D_{11}, the switches and the readout circuit). The gate bias of D_{11} was chosen to be 0.32 V for these measurements. When the oversampling rate of the $\Delta\Sigma$-ADC is 8192 or 1024, the sensor noise is 10.81 or 15.02 μVrms, respectively. Since the maximum output of D_{11} is 3.56 mV and the gain of the amplifier is 32, the sensor is able to form images with an SNR of 80 dB when the $\Delta\Sigma$-ADC oversampling rate is 8192. Here, the SNR is defined as the ratio between the $\Delta\Sigma$-ADC outputs when the sensor is illuminated by the source without an object in the beam line and when the beam is blocked. In fact, the true SNR is lower because some noise will be induced by the radiation fluctuation of the backward-wave oscillator THz source.

In most recently published works [14]–[19], [21], [24], THz imaging has been achieved by means of the lock-in technique, which requires source modulation. By contrast, this paper demonstrates the acquisition of raster-scanning images under continuous-wave illumination. Fig. 23 shows a block diagram of the THz imaging system. Fig. 24(a) and (b) shows raster-scanning images of tree leaves and pieces of metal in a paper envelope, respectively. The oversampling rate of the $\Delta\Sigma$-ADC

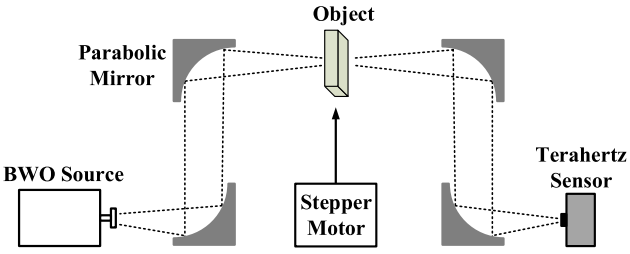

Fig. 23. Block diagram of the THz imaging system.

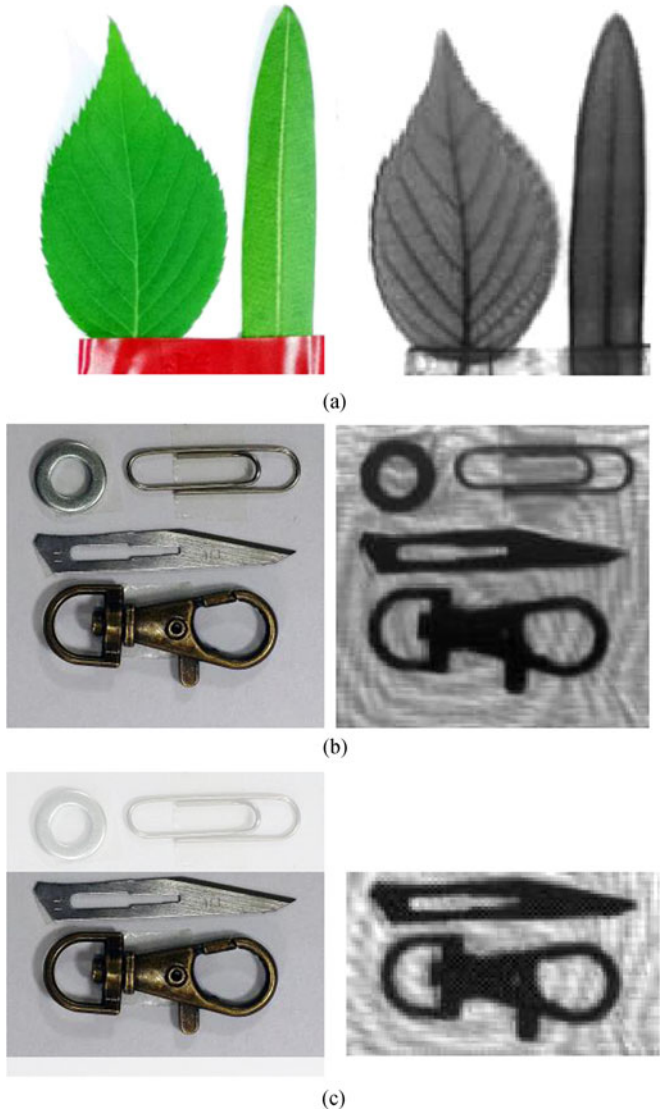

Fig. 24. (a) and (b) Images captured at 860 GHz of (a) various tree leaves and (b) pieces of metal in a paper envelope, with the $\Delta\Sigma$-ADC oversampling rate set to 8192. (c) Partial image of the metal pieces captured with the $\Delta\Sigma$-ADC oversampling rate set to 1024.

was set to 8192. For the imaging of the tree leaves, the scanned area was 5 $\times$ 4 cm^2, divided into 156 $\times$ 125 pixels. The scan required approximately 57 min. Each pixel requires 176 ms of measurement time, of which the stepper motor consumes 160 ms. For the imaging of the pieces of metal, the scanned area was 4 $\times$ 4 cm^2, divided into 125 $\times$ 125 pixels. The scan required

TABLE II
PERFORMANCE COMPARISON OF CMOS TERAHERTZ SENSORS

Technology	Freq. [THz]	Max R_V [V/W]	Min NEP [pW/Hz$^{1/2}$]	Image acquisition mode	Ref.
180 nm CMOS	0.86	3.3 k	106	Integrated ADC	This work
65 nm CMOS	0.86	[1,2]140 k	[1,2]100	External ADC	[23]
65 nm CMOS	1.027	800	66	Lock-in technique	[19]
65 nm SOI	0.65	1.1 k	50	Lock-in technique	[18]
130 nm CMOS (SBD)	0.86	0.27 k	42	Lock-in technique	[16]
130 nm CMOS	0.3	[3]90 k	–	Lock-in technique	[21]
	1.05	[3]1.8 k	–		
130 nm CMOS	0.27	[4]300 k	18.7	Integrated filter	[22]
150 nm CMOS	4.1	11	1330	–	[25]
250 nm CMOS	0.65	[5]80 k	[5]300	Lock-in technique	[17]

[1]With an integrated amplifier with a 50-dB open-loop gain and a 5-dB VGA gain.
[2]With an integrated Si lens.
[3]With an integrated amplifier with a 31-dB closed-loop gain.
[4]With an integrated amplifier with a 58-dB closed-loop gain.
[5]With an integrated amplifier with a 43-dB open-loop gain.

approximately 46 min. The images clearly reflect the internal structures of the leaves and the shapes of the metal pieces. We also extracted a partial raster-scanning image of the metal pieces with the oversampling rate of the $\Delta\Sigma$-ADC set to 1024, as shown in Fig. 24(c). Again, the shapes of the metal pieces are reasonably clear. The ADC conversion time was 2 ms. The scanned area was 2.36×4 cm^2, divided into 59×100 pixels. The scan required approximately 20 min. Although the ADC speed was four times faster, scanning the entire image still required a long time because of the slow speed of the stepper motor.

A performance comparison between this work and other published THz sensors is shown in Table II. The proposed THz sensor demonstrates the best R_V, excluding the gain of the integrated amplifier.

V. CONCLUSION

This paper reports the proposal and implementation of a fully integrated 860-GHz THz sensor in a 180-nm standard CMOS process. The sensor integrates a single-NMOS THz detector, a low-noise chopper instrumentation amplifier and a high-resolution $\Delta\Sigma$-ADC. It can detect continuous THz waves. The detector consists of a novel on-chip grounded patch antenna and an NMOS transistor. This single-NMOS detector can achieve a higher voltage responsivity than that of a two-NMOS configuration. A microstrip transmission line, TL1, is designed to improve the power transfer efficiency between the antenna and the transistor. A notch filter, TL2, is proposed to eliminate the influence of the gate bias supply line. We propose a THz-FET device model for the theoretical analysis of the operation of the THz detector. The results of this analysis indicate that an FET with the minimum possible physical dimensions can produce the maximum output signal. The experimentally measured results confirm that TL2 improves the detector performance. The detector exhibits a voltage responsivity of 3.3 kV/W and an NEP of 106 pW/Hz$^{1/2}$ at 860 GHz. With the $\Delta\Sigma$-ADC oversampling rate set to 8192, the sensor noise and the readout circuit noise are 10.81 and 2.03 μVrms, respectively. The sensor can obtain clear raster-scanning transmission images under continuous THz illumination. The results indicate that the proposed THz sensor has great potential for future development into a single, fully functional THz image sensor.

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