A 16-GHz Bandwidth Cryogenic IF Amplifier With 4-K Noise Temperature for Sub-mm Radio-Astronomy Receivers

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***Abstract*—The major mm and sub-mm radio-astronomy observatories are prioritizing instantaneous bandwidth widening for their current or planned upgrades this decade. We present an ultra-wideband and ultra-low-noise cryogenic hybrid amplifier with 4 K ($NF = 0.06$ dB) average noise temperature in the 2–18 GHz band when cooled to 6 K. It is based on a 100 nm gate pseudomorphic indium–phosphide HEMT with outstanding characteristics. This demonstration amplifier meets the noise and IF bandwidth demands of atacama large millimiter/submillimeter array (ALMA) next-generation receivers, doubling the present maximum IF instantaneous bandwidth with state-of-the-art noise performance, with a gain flatness of $\pm$0.8 dB, and output return loss better than 15 dB over 85% of the band. It can be used in the 1–19 GHz range with negligible degradation, and a tentative test has been performed with a 602–720 GHz ALMA band-9 double sideband SIS mixer, showing a flat-average and low-ripple IF noise level in an 18-GHz wideband down to near dc. A balanced configuration is feasible to improve the input matching.**

***Index Terms*—Broadband amplifiers, cryogenics, indium–phosphide pseudomorphic high-electron mobility transistors (InP PHEMTs), low-noise amplifiers (LNAs), noise measurement, radio astronomy, submillimeter wave, superconductor–insulator–superconductor (SIS) devices, ultra-wideband technology.**

I. Introduction

MILLIMETER- and submillimeter-wave radio astronomy explores the spectrum between the infrared and the microwaves. In this frequency range, it is still possible to use sensitive heterodyne receivers, which preserve the phase information of the signal, allowing to build interferometers that are capable of obtaining extreme angular resolution with very high sensitivity. These instruments provide a unique view of the universe and have been fundamental for the development of our present astronomical knowledge. Some of the scientific cases addressed by this technique, just to name a few, are planet and star formation from dust and gas clouds, the first stars and galaxies emerging from the "dark ages" of the young expanding universe, the complex chemistry of the interstellar medium, the production of large organic molecules, which may lead to the origin of life, and the obtainment of the first direct images of black holes.

The major observatories of this kind in the world are in continuous evolution to improve their scientific production and a common prime concern is to achieve ever broader instantaneous bandwidths to enable gains in speed and sensitivity. For example, atacama large millimiter/submillimeter array (ALMA) Scientific Advisory Committee has marked this topic with the highest priority in the Horizon 2030 development path [1], and other major radio telescope interferometers, e.g., SMA [2], NOEMA [3], [4], and ngEHT [5], are in the way of implementing similar upgrades.

The first component of a typical radio-astronomy heterodyne front end for bands higher than 100 GHz is a superconductor mixer (superconductor–insulator–superconductor (SIS) or hot electron bolometer) followed by an IF cryogenic low-noise amplifier (CLNA). The sensitivity obtained depends critically on the noise performance of both. Some results suggest that SIS mixers could reach the goal of a wider bandwidth with a careful design [6]. Our work addresses the demonstration of a CLNA to fulfill the future needs of a wider instantaneous IF bandwidth of large sub-mm radio telescopes, taking the guidelines given for ALMA in terms of noise and bandwidth. The present generation of ALMA receivers has up to 8 GHz instantaneous IF bandwidth (typically 4–12 GHz). The goal is to double that figure to reach at least 16 GHz per sideband for each polarization. In the case of a sideband separating (2SB) mixer and two polarizations, this accounts for a total of 64 GHz per band to be processed by the backend. Although some ultra-wideband CLNA with excellent performance have been demonstrated and even produced commercially [7], [8], [9], [10], [11], [12], there are very few amplifiers with the required 16 GHz bandwidth in the SIS IF range.

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Indium–phosphide (InP) or mGaAs HEMTs are still the workhorses for CLNAs, although other emerging technologies have also demonstrated interesting characteristics, such as SiGe heterojunction bipolar transistors [13], which may be advantageous for applications starting at very low frequencies (hundreds of MHz), or traveling-wave kinetic inductance parametric amplifiers [14], which promise quantum-limited noise levels with negligible power dissipation.

The optimum frequency range to obtain 16 GHz instantaneous bandwidth may depend on several details of the system, including the type of mixers. From the point of view of the stand-alone amplifier, it is better to keep the maximum frequency as low as possible since the noise temperature of the HEMT devices is roughly proportional to the frequency. However, this leads to very large fractional bandwidths (FBWs), which may limit the performance of other components needed in the system (for example, quadrature hybrids for 2SB mixers or balanced amplifiers). The choice of 2–18 GHz for this demonstration imposes an FBW of 9:1 or 160% (almost a decade). Good performance decade-wide cryogenic quadrature hybrids in stripline technology for similar frequency ranges have also been demonstrated [15].

Another problem that appears in high FBW HEMT CLNAs is the difficulty in controlling the input reflection at the low-frequency end of the band. This may lead to noise and gain ripples in the system. A mixer–CLNA integration [16], [17] would reduce these ripples, but the matching problem still persists. One possibility to address this is using a wideband ferrite isolator at the input. This approach was taken in earlier generations of ALMA receivers. However, it is particularly challenging to obtain good performance cryogenic isolators for a band as wide as our target, as they tend to add significant losses (degrading the noise) and are very bulky [18]. Other interesting possibility feasible even in widebands is using balanced amplifiers [15], [19], although this adds complexity and increases the power dissipation.

The rest of this article is organized as follows. Section II introduces the development of the new generation of transistors. In Section III, the design and fabrication of the amplifier are explained. Section IV describes the measurement procedures, focusing especially on the noise characterization, and discusses the performance of the amplifier presented. Finally, Section V concludes this article.

II. Device Development

The InP pseudomorphic HEMT transistors were produced at FIRST-lab foundry in ETH-Zurich by Diramics AG. Diramics 100 nm process features a GaInAs channel and AlInAs barrier. In particular, the transistor of the first stage of this work is the outcome of a long-term joint effort of Diramics and Yebes Observatory to achieve a significant improvement over what we will call Diramics "standard devices," in the two key features holding back ultralarge FBW CLNA development: stability and noise temperature.

The stability is favored by the not too aggressive 100 nm gate-length technology employed by Diramics. We found no significant advantage in noise in this frequency range by further reducing the gate length. This can be explained by the reduction of the shot noise suppression factor [20], while the increase in cutoff frequency (f_T) and maximum oscillation frequency ($f_{\max}$) of shorter gates provides no benefit at these frequencies and makes the device more prone to very high-frequency oscillations. Layout-related stability enhancement came from the reduction of the source metallization area to reduce its parasitic capacitance to ground, shifting the problematic resonance with the bond wires to higher frequencies, and the use of two-finger layouts and source air bridges. More fingers may theoretically help in reducing the parasitic gate resistance and, therefore, noise, but at cryogenic temperatures, this effect is negligible and comes with the cost of increasing the risk of high-frequency instabilities due to the existence of odd resonant modes in the structure that can be excited by small asymmetries [21]. We have verified that the restoration of the symmetry by drain and gate air bridges kills these oscillations, but it is detrimental to noise and gain in the high end of our IF band due to the added parasitic capacitance. Even though such asymmetry effects are less common in two-finger transistors with gate peripheries below 200 μm, source air bridges are employed, as we have confirmed experimentally that they also contribute to improve the stability with no other drawbacks [22]. All these layout features can be seen in Fig. 1(a).

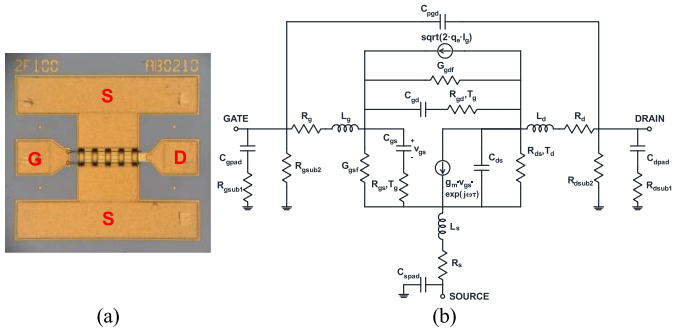


Fig. 1. 2×100 μm gate finger InP HEMT in 100 nm technology used in the first stage of the amplifier. (a) Microphotograph of the $350 \times 350 \times 100$ μm die with the transistor terminals labeled and where the source air bridges can be seen. (b) Small-signal and noise model (parameter values are listed in Table I).

Solely the enlargement of the oscillation-free bias regions in many cases leads to noise temperature improvements, as better bias settings are accessible. Further noise reduction came from the enhancement of the standard epitaxial layer structure (described in [23]) to reduce impact ionization and improve channel control. The latter was achieved through a reduction of the gate-to-channel distance, lowering the Schottky barrier and, thus, providing higher transconductance for lower drain currents. According to the figure-of-merit (FOM) defined in [24] as $\sqrt{I_d/g_m}$, this behavior points to devices with lower minimum noise temperature. The downside of a thinner barrier layer is an increase in the tunneling effect producing more gate leakage current and, therefore, higher gate shot noise, which may become relevant at very low frequencies. The optimum thickness was found around 70% of the standard material, by testing samples from different runs, from 45% to 85% scaling.

What we refer to as "optimized devices" incorporate all the preceding enhancements in layout and epitaxial material.

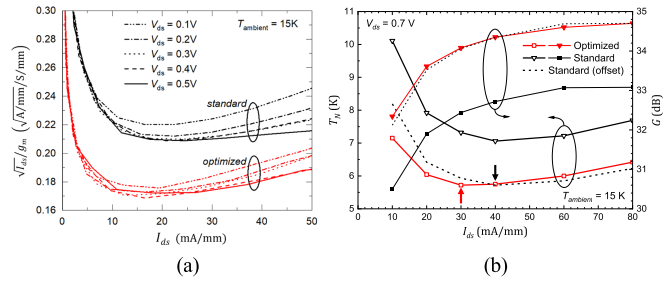


Fig. 2. Comparison of (a) device FOM from cryogenic on-wafer measurements and (b) average noise (thick lines) and gain (thin lines) of a test amplifier with the device in the first stage. Optimized devices in red exhibit better performance and a displacement of the minima to lower drain currents. Dashed lines in (b) are normalized for easy comparison.

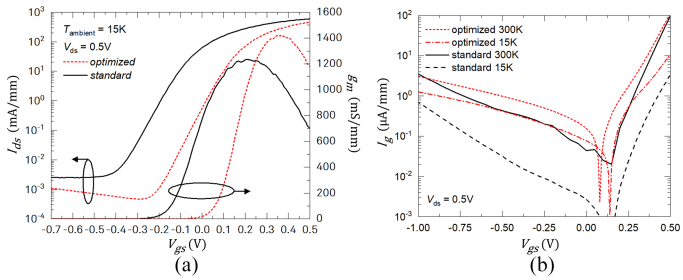


Fig. 3. (a) Drain current and transconductance, and (b) gate current variation with gate voltage of optimized (red) and standard (black) devices. For the optimized devices, the maximum transconductance is higher, with a sharper turn on and for lower drain currents as in (a), but the gate leakage in (b) is worse due to the lower Schottky barrier.

The cryogenic noise improvement was evaluated by comparing the noise temperature of wideband test amplifiers fitted with standard or optimized devices of the same layout in its first stage. Different gate peripheries were chosen according to the frequency band of each CLNA. A reduction from 15% to 20% in noise temperature was confirmed from L to Q bands.

Fig. 2 shows how the aforementioned FOM can be a good predictor of the noise temperature and how the optimized devices show a shift to both the minimum noise temperature and minimum FOM toward lower drain currents when compared with standard ones with poorer noise performance. On the left plot are cryogenic on-wafer dc measurements of the standard and optimized devices, which resemble closely the plot on the right of the cryogenic noise of an amplifier with the device under test (DUT) in the first stage. Fig. 3(a) illustrates the improvement in transconductance ($g_{m,\max} \approx 1450$ mS/mm) and the sharper turn-on of the optimized device for lower drain currents (subthreshold slope of ≈76 mV/dec), while Fig. 3(b) shows the other side of the coin: a higher gate current, that is still low enough for the gate voltages applied at the optimum bias to neglect the added shot noise (pinch-off quality is good $I_{\rm ON}/I_{\rm OFF} \approx 88$ dB).

The transistor scattering parameters were measured on-wafer at cryogenic temperature by Diramics and fitted to the small-signal circuit model of Fig. 1(b). Transistor cryogenic noise parameters are extremely difficult to measure with enough accuracy to be useful for low-noise amplifier (LNA) modeling. Instead, the device noise was modeled according to Pospieszalski [25]. Gate temperature was set to ambient temperature and assigned to R_{gs} and R_{gd} in the small-signal model. Drain temperature was assigned to R_{ds} and T_d was obtained by fitting the cryogenic noise measurements of a well-known wideband amplifier with the device mounted in its first stage. These measurements were done with the cold attenuator (CA) method, as described in Section IV. The estimated drain temperature is 900 K. Table I lists the values of the model parameters for the standard and optimized devices. Gate leakage current shot noise was found quite irrelevant for this device and frequency range. It is significant to note that there is an undesirable increase in C_{gs} due to the thinner barrier layer, which shifts the frequency response and can make matching of the transistor more challenging.

TABLE I
CRYOGENIC MODEL PARAMETERS OF A STANDARD (S) AND OPTIMIZED (O) 2 × 100 μM DIRAMICS INP HEMT

	Intrinsic										Noise		
	C_{gs}	C_{gd}	C_{ds}	R_{gs}	R_{gd}	R_{ds}	G_{gsf}	G_{gdf}	g_m	τ	T_g	T_d	I_g
S	126	46	46	0.6	9	69	0	1m	189	70	T_{amb}	800	0
O	169	37	64	0.8	16	76	5.2m	0.4m	255	100	T_{amb}	900	48

	Extrinsic						Pads							
	R_g	R_d	R_s	L_g	L_d	L_s	C_{gpad}	G_{gsub1}	G_{gsub2}	C_{dpad}	R_{dsub1}	R_{dsub2}	C_{pgd}	C_{spad}
S	0.5	0.9	0.7	68	62	8	10	18T	28T	9	38	3G	1	177
O	0.5	0.9	0.7	65	61	1	11	26P	1P	9	48	1T	1	186

T_{amb} = 15 K – V_{ds} = 0.5 V, I_d = 30 mA/mm – Units are fF, Ω, mS and ps

III. AMPLIFIER DESIGN AND FABRICATION

The presented CLNA is based on a previous 2–14 GHz design used in the front end of very-long-baseline interferometry (VLBI) radio-astronomy receivers in a balanced configuration [15], [19]. The development of the optimized devices and the new demands from the radio-astronomy sub-mm-wave community opened the door to a redesign aimed to widen the band toward 18 GHz with top noise performance by incorporating one of these transistors in the first stage.

An HEMT-based design in this band aims for the lowest noise, flat gain, low output return loss, and unconditional stability, but the input return loss (IRL) at the lower band end was not included in the optimization. The possibility of a mixer–CLNA codesign avoiding the 50-Ω input matching is out of the scope of this work. The complex noise interaction between the CLNA and the mixer is not only dependent on the amplifier IRL but also its effect has to be tested for each particular mixer design (an illustrative result is given in Section IV). Note that the poor IRL could deteriorate the image rejection of 2SB mixers. These potential problems could be overcome while keeping the same FBW and similar noise performance by using this design in a balanced configuration [26]. The ultra-wideband quadrature hybrid couplers needed are feasible, as good performance hybrids with the same FBW (1.5–15.5 GHz) have been already developed for VLBI receivers [15]. The estimated average noise penalty with respect to the single-ended option would be around 1–1.5 K. The required similarity in performance of the amplifier

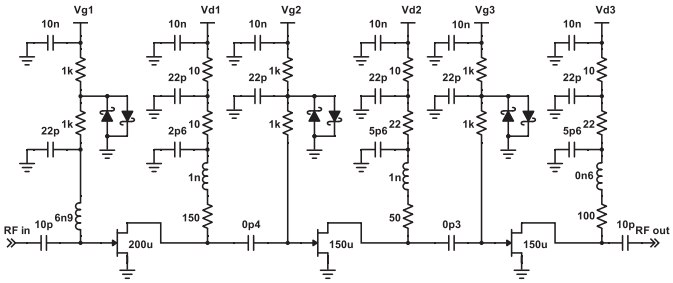
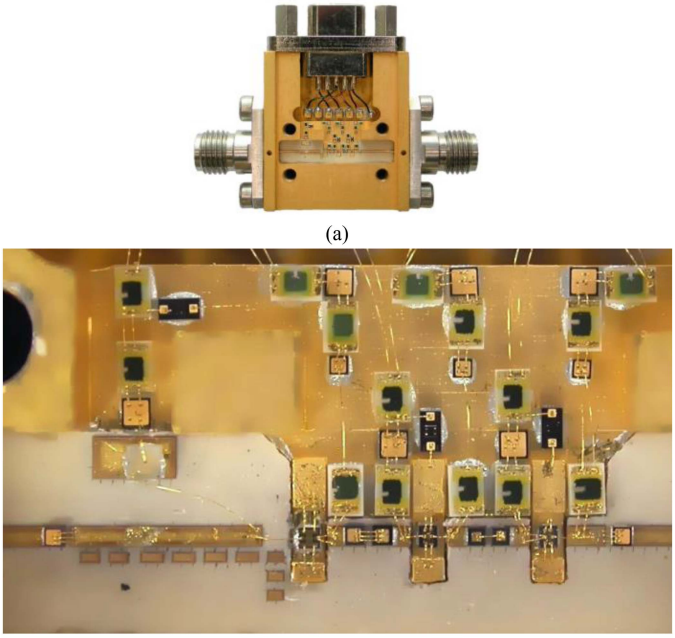


Fig. 4. Simplified schematic of the three-stage 2–18 GHz LNA. SI units used.



(a)

(b)

Fig. 5. (a) Photograph of the three-stage 2–18 GHz CLNA without cover. Dimensions excluding connectors are 20 × 22 × 9 mm. (b) Detail of the circuit.

units paired to guarantee good results [26] is perfectly within the present fabrication tolerances, as demonstrated in the production of other wideband balanced amplifiers [19].

The amplifier is a three-stage common source design implemented in microstrip hybrid—chip and wire—technology, fast to produce, modify, and tune and with the added advantages over a monolithic microwave-integrated circuit (MMIC) approach of allowing different transistor technologies for each stage and having lower loss in the critical input matching circuit. However, MMIC-based LNA designs can achieve better repeatability within the same batch, easier manufacturability for large series, and easier integrability with SIS and in balanced configurations, and they may also be advantageous at higher microwave frequencies. A simplified schematic and a photograph of the amplifier are shown in Figs. 4 and 5.

Section II presents the characteristics of the device used that minimize noise and avoid high-frequency oscillations and describes how it was measured and modeled. However, in ultra-wideband CLNAs, where the input matching circuit must be as simple as possible, the gate width is a key design parameter. The selection of the gate width depends on the frequency band, as it fixes the real part of the optimum noise impedance $R_{\rm opt}$. Wider gates present lower resistance, which is good toward low frequencies, where $R_{\rm opt}$ grows very rapidly, but not so much above a few GHz where its value is already well below 50 Ω. In our case, in addition to device modeling and simulation, we tested transistors from 150 to 250 μm total gate widths in the 2–14 GHz amplifier. The chosen gate periphery was 200 μm. Still, the optimum noise impedance of an HEMT is highly reactive, but this is more easily matched by the reactance of a bond wire. The second and third stages feature the original design of six-finger 25 × 0.1 μm gate InP HEMT devices [1] (as used in [27]). This smaller size favors gain equalization by improving matching in the higher end of the band, where the noise-optimized first stage has an important gain roll-off. Models of these devices were obtained by test fixture measurements.

The microstrip circuits are implemented in a soft laminate[2] with excellent thermal properties at cryogenic temperature. However, most of the matching and the in-band stabilization (critical with HEMT devices) are actually achieved with lumped chip components and bond wires. It was of particular importance careful selection and modeling of the chip resistors, spiral inductors, and MIS capacitors at cryogenic temperature [28], [29], [30].

In such a wideband amplifier, the classical approach of separating design goals per stage is not really applicable, as most of the performance parameters are distributed in all stages. Not only noise optimization is reserved only for the first stage but also the second one contributes significantly to the noise budget at high frequency because of the low gain of the first due to the aforementioned roll-off.

Classical inductive source degeneration provided by bond wires is used to improve the in-band stability of the amplifier, and in the first stage also to bring closer the minimum noise and input conjugate impedances. Furthermore, stability and gain equalization are attained by drain resistive loading[3] and with the small interstage dc-blocking capacitors[4] (combined with their bond wires).

Note that power dissipation and input reflection were not priority design goals, and thus, other parameters were not compromised substantially. On the contrary, unconditional stability forced painful trade-offs in gain, flatness, and reflection.

A significant improvement over the past designs was introducing the first-stage gate bias through a small quartz chip spiral inductor,[5] instead of a conical inductor or a high-value resistor as in the other stages. This low loss, low parasitic component is also involved in the noise matching, and it reduced by 10% the noise temperature with respect to the conical inductor option; the selection of the right value achieved a flattening of the gain at the high end of the band by inductive peaking.

[1] HRL Laboratories, LLC, H2·150

[2] Rogers RT/duroid 6002, 5 mil $\varepsilon_r = 2.94$ dielectric, 17 μm electrodeposited copper cladding and 6 μm solft gold plating.

[3] State-of-the-art SOA0302APG series.

[4] Skyworks SC series and MACOM 91 series.

[5] Piconics SP4P5-20-QCW

The amplifier has independent bias lines for each stage featuring two *R–C* filtering sections to decouple the RF and electrostatic discharge (ESD) protection elements in the gate lines: a 10 nF CG0 capacitor acting as a charge divider and two antiparallel Schottky GaAs diodes to limit the gate voltage. All components are mounted directly on the module, as seen in Fig. 5.

All the fabrication (microstrip laser structuring, module machining, and plating) were performed in-house. The amplifier was assembled on a gold-plated aluminum module fitted with 2.92 mm coaxial connectors and an micro-D dc connector, following similar procedures to the ones established for the production of ALMA bands 5, 7, and 9 IF amplifiers [27].

We expect good repeatability of the results of this design, based on the similarity to the 2–14 GHz design and other previous designs [27] for which a large number of units were assembled. The construction techniques are identical, the sensitivity to bond wires and component values is comparable, and the expected dispersion in transistor parameters is the same. As an example, a variation of 10% in the length of the most critical bond wires (in the first-stage transistor source pads) produces only a minor impact on the gain flatness (changing the slope to 0.3 dB).

IV. Amplifier Characterization

A. Measurement System

The characterization of the cryogenic noise of a CLNA is a challenging task, especially at low frequency, where the uncertainty levels can easily be comparable with the measurand and the results from different laboratories may differ significantly. Two different measuring methods have been used based on the practical convenience and accuracy: the CA and the variable temperature cryogenic load (VTCL).

The CA method uses an external diode noise source of high (>12 dB) excess noise ratio (ENR) and an attenuator (typically 15–20 dB) cooled to cryogenic temperature and connected to the input of the DUT. The noise source can be switched quite fast (≈40 ms period) under the control of commercial noise figure measurement equipment, allowing efficient frequency sweeps, switching between on and off at each point *s*. This was the method of choice when optimizing the bias of the LNA. However, the accuracy depends strongly on the complex calibration of the loss of all the elements in the input path and on the true value of the physical temperature of the attenuator.

This method was implemented in a system built for ALMA IF LNAs measurements based on a CTI 1020 closed cycle refrigerator capable of cooling the DUT to 14 K [31], but with some significant improvements (see Fig. 6). The input cable serving as a thermal break between the input hermetic transition and the CA is a stainless-steel coaxial airline crafted in-house to reduce the uncertainties associated with dielectric displacements due to thermal cycling. The 15 dB CA is based on a GaAs MMIC [32] [see Fig. 6(b)] soldered with indium to a gold-plated oxygen-free copper chassis. The residual heat coming from the inner conductor of the coaxial line is sunk very effectively to the cold plate, thanks to the excellent thermal conductivity of the GaAs substrate at cryogenic temperatures,

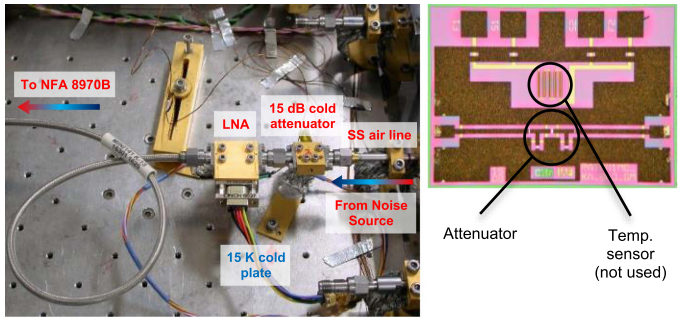


Fig. 6. (a) 1020-3 measurement system based on the CA method. (b) GaAs chip with the π-type attenuator. A Lake Shore calibrated diode sensor inside the attenuator body is used instead of the sensor integrated into the chip.

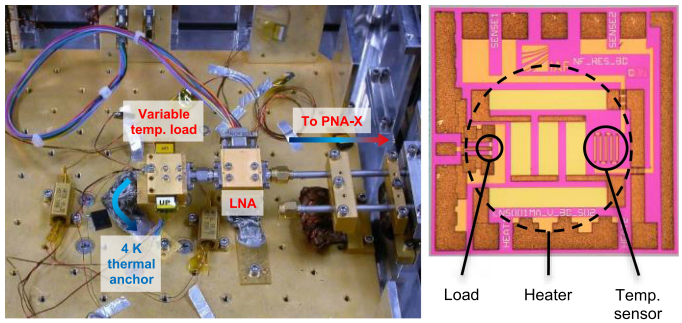


Fig. 7. (a) SUMI-1 measurement system based on the VTCL method. (b) GaAs chip integrating the load, the heater, and the temperature sensor.

and therefore, the reading of the temperature sensor reproduces accurately the real attenuator temperature. A calibrated diode sensor with better sensitivity at very low temperatures is used instead of the resistive sensor integrated into the chip. The electrical performance is very good, with more than 20 dB return loss in the frequency range of the measurements presented (up to 26.5 GHz). The MMIC NiCr thin film resistors are quite invariant with temperature, but the variation of loss upon cooling of the pure metals in the microstrip access lines and connectors (around 0.2 dB at 10 GHz) is significant and must be characterized and corrected for.

The VTCL method uses a matched load cooled to a controllable cryogenic temperature inside the cryostat and connected to the input of the amplifier as a noise source. This method enables higher accuracy since it depends only on the calibration of the load temperature sensor, given that the loss of the connection to the DUT is low and the system gain is stable throughout the measurement. However, the process of changing the physical temperature of the load is slow (≈15 s stabilization time); therefore, it was chosen only for final measurements.

This method was implemented in a system based on a Sumitomo RDK 415D refrigerator capable of cooling the DUT to 5 K (see Fig. 7). The VTCL used [33] is based on a GaAs chip [see Fig. 7(b)], which contains a temperature stable high-frequency 50 Ω NiCr termination, a 1 kΩ NiCr heating resistor, and a resistive temperature sensing element. The chip is mounted with

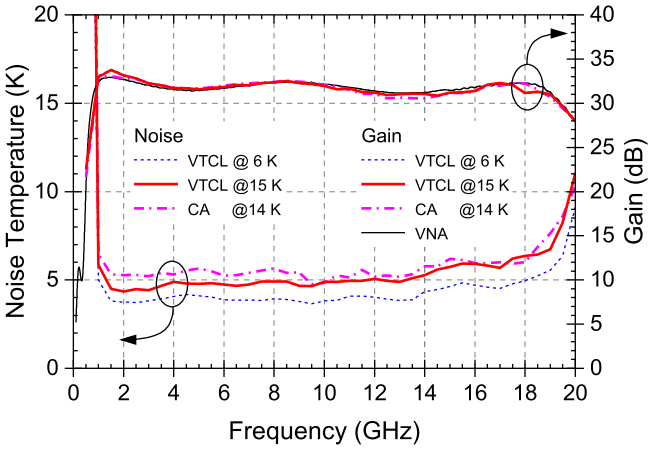


Fig. 8. Comparison between the measurements of the LNA with the CA and the VTCL near 15 K ambient temperature. An additional dotted trace shows the results with the VTCL at 6 K ambient. Gain data are obtained in the same noise figure analyzer measurements, except for the black thin line taken with a vector network analyzer (VNA).

silver epoxy [34] on a gold-plated brass chassis fitted with a 2.92 mm coaxial connector. A PID temperature controller (Lake Shore model 336) was used for the cryogenic temperature measurement and control. For our measurements, the hot and cold temperatures used were 45 K and 25 K, respectively. Within this range and with the calibrations performed, the estimated accuracy of the thermometer reading is better than ±0.15 K. The controller has two independent PID control loops, one used for stabilizing the temperature of the cryogenic amplifier (with heating resistors attached to the cold plate and a diode sensor in the body of the LNA) and the other for controlling the temperature of the VTCL. The time needed to change the temperature from 25 to 45 K or vice-versa and to stabilize within 0.03 K is 15 s. The return loss of the VTCL module is higher than 22 dB up to 26.5 GHz. The noise power is measured with a 50 GHz PNA-X noise receiver.

The noise error budget estimated by Monte Carlo simulation for the amplifier presented here (including the calibration error) is ±1.2 K for the CA system and ±0.7 K for the VTCL system (coverage factor $k = 2$) [28]. Both systems are relatively immune to the IRL of the amplifier. The dominant contributors to the error are, in the case of the CA system, the uncertainties in the source ENR, and in the CA value and its temperature. For the VTCL system, the errors come mainly from uncertainties in the hot and cold temperatures of the load and the small gain drift of the system between the hot and cold sweeps.

Both systems compare fairly well as Fig. 8 shows. The difference in average noise is less than 0.5 K, well inside the error bars. The noisier and slightly rippled magenta dash-dot trace of the CA measurement reveals the higher uncertainties in the calibration due to the reflections within noise source, attenuator, and DUT. The data presented in the rest of this article have been obtained at an ambient temperature of 6 K, closer to the typical 4–5 K of a Dewar for SIS mixers, using the VTCL method. The blue dotted trace represents this reference measurement. It is noteworthy that there is an offset of 1 K in noise temperature between 15 and 6 K ambient data.

TABLE II
NOMINAL CRYOGENIC BIAS SETTINGS

Stage	Device	V_{dd} (V)	V_{ds} (V)	I_d (mA)	V_{gs} (V)
1	Diramics 2F×100 µm	1.70	0.65	6	+0.21
2	HRL 6F×25 µm	0.70	0.27	5	-0.08
3	HRL 6F×25 µm	1.00	0.32	5	-0.04

Cryogenic *S*-parameters were measured with an Agilent E8364B vector network analyzer in a setup similar to Fig. 6 but removing the CA [24]. The system is calibrated at room temperature up to 26.5 GHz with the reference planes inside the cryostat, using an electronic calibration module in the position of the DUT. A small correction to the transmission (S_{21}) is applied to compensate for the reduction of loss of the cold copper cable at cryogenic temperature. A cleaner view of the reflection (S_{11} and S_{22}) is obtained by applying a gate in the time domain to cancel the effect of the small changes in the stainless-steel cables when cooled.

Of special interest in this type of amplifier is the characterization of the stability at cryogenic temperature. In Section III, it justified the importance of a stabilizing network for amplifiers based on HEMT devices. Unconditional stability in the frequency range covered by the *S*-parameter measurements can be checked at each bias point by calculating the Rollet factor. However, the extremely high f_T and $f_{\max}$ of these transistors favor the appearance of very high-frequency oscillations [21], [22], well above the measuring range of laboratory microwave instrumentation. A very effective way to detect them is by measuring the dc curves of each stage (I_d–V_d), which allows an easy identification of the problematic bias regions. Oscillations usually show up as sharp changes in the I_d–V_d curves slopes. The verification of the dc curves was done using in-house software and high-precision dc power supplies (Agilent N3280A) in constant voltage mode. The curves are measured during the *S*-parameter testing cool down, with the amplifier connected to a VNA (with the generator switched off) and also in another cool down with shorts at the input and output connectors to reproduce the most unfavorable loading condition.

B. Results

The amplifier has been measured using the bias settings of Table II, with a power dissipation of 17.7 mW (where V_{dd} refers to the power supply drain voltage and V_{ds} is the voltage at the transistor drain terminal). Low-power dissipation was not a priority in this prototype; nevertheless, we have now the expertise to reduce the series drain resistor voltage drop (accountable for 11.5 mW of dissipation) by a redesign of the bias networks. The possibility of independently biasing the three stages allows for better combined optimization of the performance parameters of the amplifier, i.e., noise temperature, gain flatness, output reflection, or linearity, as well as for the identification of instabilities by inspection of anomalies in the device I_d–V_d curves.

The measured noise temperature is rather uniform in the 2–18 GHz band, ranging between 3.6 and 4.9 K, with an average

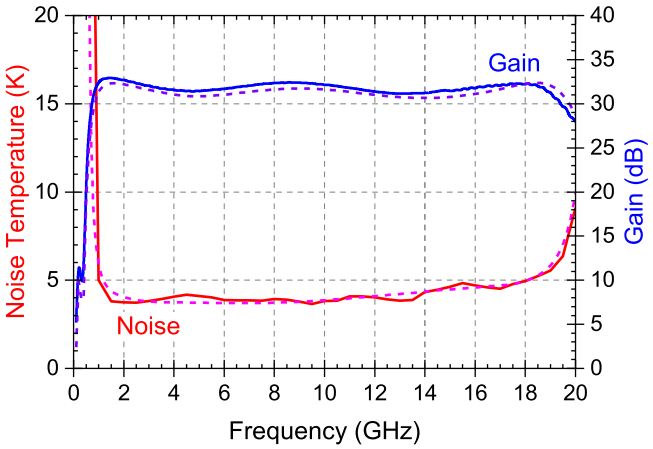


Fig. 9. Measured (solid lines) and simulated (dashed lines) gain and noise temperature of the LNA at 6 K ambient and nominal bias (see Table II).

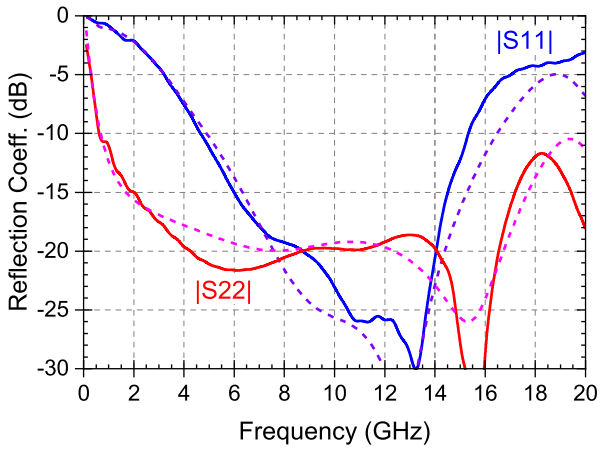


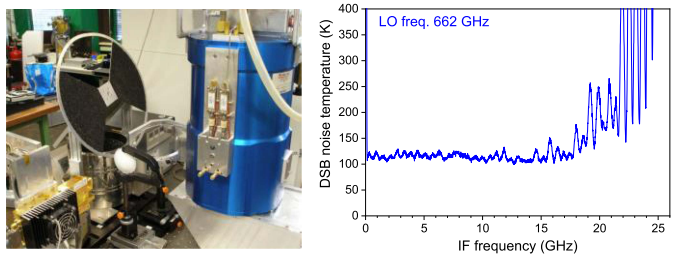
Fig. 10. Measured (solid lines) and simulated (dashed lines) input and output reflection of the LNA at 15 K ambient and nominal bias (see Table II).

of 4.1 K. A slightly higher bias of the first stage (increasing 0.2 V the drain voltage) reduces this value just below 4 K. These noise temperature numbers are, to the best of our knowledge, the lowest reported for an amplifier in a 16 GHz wideband. Gain is also very flat considering the band span, with 31.8 dB on average and a peak-to-peak ripple of just 1.6 dB. The output return loss is above 15 dB for most (95%) of the band.

As stated before, using InP HEMT technology for such wide FBW allows to reach ultimate noise performance, but an acceptable input matching is not feasible at low frequencies. Therefore, IRL was not a design goal, and no attempt to optimize it was made. Results above 12 dB are obtained between 5 and 15 GHz.

Figs. 9 and 10 show that the LNA behaves very similarly in the 1–19 GHz band. The average noise temperature is 4.2 K, peak-to-peak gain ripple increases only up to 1.8 dB, and output return loss is now higher than 15 dB in 85% of the band. This 18 GHz wideband represents an FBW of 180%.

Simulated and measured values agree remarkably well in noise and gain (see Fig. 9), and the reflection results fit the predictions also quite closely (see Fig. 10). This owes to the careful modeling of the devices and components. The small discrepancies in return loss at the top end of the band may be



(a) (b)

Fig. 11. (a) Experimental setup, including the wet cryostat (blue, right), the local oscillator (LO) block (golden, left), an high-density polyethylene (HDPE) lens and beamsplitter between them, and a chopper with absorber (black) on top of an LN2 bucket (silver) (hot/cold loads). (b) DSB IF noise temperature results in an LO frequency of 662 GHz.

attributed to the tolerance of the interstage capacitors between the first and second stages. Only a few marginal modifications in the LNA model to account for the variation of bond wire lengths were implemented after fabrication.

The tradeoffs in performance for stability paid off, as the amplifier is unconditionally stable for all bias settings evaluated. The dc curves do not show any signs of instabilities for any stage, either with the ports loaded with 50 Ω or a short circuit; only for very high bias of the HRL transistor of the second stage, hints of high-frequency oscillations appear.

Linearity was checked at 6 K ambient. A 1 dB compression point (P1dB) and third-order intercept point (TOI) were measured with a PNA-X N5247A at several bias settings. At 3 GHz (in the least linear part of the band) and with the nominal bias of Table II, the input P1dB is −40.5 dBm and TOI is −31.5 dBm. These values could be improved significantly by raising the drain voltage and current of the second and third stages or by using a GaAs transistor with better linearity in the last stage (but which also requires a higher bias setting). However, for the intended application, the power level at the input is extremely low; thus, the linearity requirements are relatively lenient: this LNA complies with ALMA output P1dB specifications of −20 dBm by an ample margin of more than 10 dB. On the contrary, a high-power dissipation could jeopardize the cooling capacity of the Dewar in the critical 4 K stage where the SIS mixers and LNAs stand.

Table III compares the performance of the presented CLNA in the nominal 2–18 GHz and extended 1–19 GHz bands with the best amplifiers with comparable FBW, total bandwidth, and noise temperature found in the literature, and also with improved commercial versions that have evolved from some of them. Our amplifier stands out in noise temperature for a bandwidth of 18 GHz (180% FBW).

C. Tentative Tests in a THz Receiver

To illustrate the "in the field" possibilities of a single-ended amplifier like this, with its IRL limitations, when combined with a practical mixer, it was tested in the IF chain of a double sideband (DSB) sub-mm receiver. The experimental setup used a wet cryostat with an ALMA band 9 (602–720 GHz) SIS chip [see Fig. 11(a)], described in detail in [36]. The IF amplifier was an unoptimized early prototype with standard devices. Its noise

TABLE III
COMPARISON OF CRYOGENIC MULTIOCTAVE LNAS

Reference	Technology	Band (GHz) (FBW)	T_{av} (T_{min}-T_{max}) @T_{amb} (K)	Gain (dB)	P_{dis} (mW)
[7] JPL 2006	100 nm InP MMIC	1-11 (167%)	3.9 (2.3-5.3) @4.1	31.5 ± 1.8	24
[8] Caltech 2013	70 nm mGaAs MMIC	1-16 (176%)	6.3 (4.5-10.4) @21	36.9 ± 1.9	15
[9] CTH 2014	100 nm InP MMIC	6-20 (108%)	5.8 (4.4-9.1) @10	35.9 ± 0.8	13
[10] CTH 2018	100 nm InP MMIC	0.3-14 (192%)	3.5 (2.2-6.2) @4	41.6 ± 1.4	12
[11] CMT	70 nm mGaAs MMIC	1-18 (179%)	6.3 (3.9-12.7) @12	35.3 ±1.2	30
[12] LNF	100 nm InP MMIC	4-20 (133%)	3.8 (2.5-7.1) @5	32.8 ± 1.8	22
This work	100 nm InP hybrid	2-18 (160%)	4.1 (3.6-4.9) @6	31.8 ± 0.8	18
This work	100 nm InP hybrid	1-19 (180%)	4.2 (3.6-5.5) @6	31.9 ± 0.9	18

[10] is commercially available (LNF)
[11] and [12] are commercially available versions of [8] and [9] respectively, optimized for a wider band [11] or using better devices [12]
[12] has a nominal band in the datasheet of 6-20 GHz, but we present its results in an extended 4-20 GHz band

temperature was double that of the final unit, but the noise and gain performance were acceptable down a few MHz due to the absence of the gate inductor.

The results of the *Y*-factor measurements (performed using mm-wave absorbers at room and liquid nitrogen temperatures) at one sample LO frequency are displayed in Fig. 11(b). It is remarkable that a quite uniform noise response extends almost down to dc (despite the poor IRL of the LNA below 5 GHz) and up to 18 GHz (probably limited only by the warm IF components of this quick test).

V. CONCLUSION

This article has demonstrated a cryogenic amplifier with the best-known noise performance in a 16 GHz wideband, from 2 to 18 GHz, together with a very flat gain of 32±0.8 dB and an output reflection below −15 dB in most of the bands. Furthermore, 4 K noise temperature results are extensive with almost no degradation in gain and return loss to the 1–19 GHz band. Besides, to achieve these unique characteristics, a new generation of InP indium–phosphide pseudomorphic high-electron mobility transistor devices with state-of-the-art noise and enhanced stability was developed, featuring changes in layout and epitaxial layer structure.

This band is of utmost importance for the future upgrades of the major sub-mm radio-astronomy observatories of the world where an amplifier of this kind has been demanded by the front-end development groups. The question of whether a higher IF band with, most likely, better input reflection (as 4–20 GHz) is really more convenient from the system point of view remains open. It is undeniable that the excellent noise results from almost dc to 18 GHz demonstrated in a THz receiver are very promising, but a fair comparison with other amplifier options demands more measurements, including image rejection. Nor can we forget that the possibility of balancing this amplifier (realizable with existing technology) would bring near perfect matching with the mixer.

The prototype built is a robust design easily producible. However, some feasible upgrades have been mentioned that would greatly benefit the sub-mm front-end architecture, namely, the integration of a bias-T to dc feed the mixer and the reduction of power dissipation by using optimized transistors in all stages (which also have higher gain) and implementing known solutions to cut the voltage drop in the bias networks.

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Ralf Flückiger, photograph and biography not available at the time of publication.

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