A Terahertz Monostatic Transceiver in 90-nm SiGe BiCMOS

Christoph Mangiavillano, Alexander Kaineder, Klaus Aufinger, *Member, IEEE*, and Andreas Stelzer, *Member, IEEE*

***Abstract*—A combined common collector harmonic mixer and frequency multiplier is designed to operate at the fourth harmonic in a transceiver at around 0.88 THz in a 90-nm SiGe bipolar CMOS technology with an f_T/f_{max} of 300/480 GHz. The transceiver occupies a chip area of 1.35 mm^2 with a current consumption of 144 mA when connected to a 3.3-V supply. Measurements reveal an effective isotropic radiated power of −30 dBm at 0.888 THz and a system receiver conversion gain of −4 dB as well as a single-sideband noise figure of 57 dB at 0.912 THz.**

***Index Terms*—Mixer, multiplier, on-chip antenna, SiGe bipolar CMOS (BiCMOS), terahertz (THz), transceiver.**

I. Introduction

CMOS and SiGe bipolar CMOS (BiCMOS) technologies can offer high integration levels for low-cost mass-market applications [1]. Current BiCMOS research offers f_{max} at around 650 GHz [2] with typical BiCMOS production technologies having an f_{max} of 450–480 GHz [3], [4] and CMOS research offering f_{max} of 450 GHz [5]. Using silicon-integrated technologies at terahertz (THz) frequencies, therefore, becomes challenging due to the absence of practical transistor gain above $f_{max}/2$, currently only demonstrated at 1 THz using a III–V InP high-electron-mobility transistor with f_{max} of 1.5 THz [6]. Nevertheless, state-of-the-art THz designs are commonly implemented using bulky split-block designs incorporating III–V Schottky diodes, which show excellent receiver noise temperatures of around 3000 K at 0.85 THz [7], 0.874 THz [8], and 1.134 THz [9]. Similarly, an output power of around 2 mW has been achieved using a Schottky diode frequency tripler at 1.03 THz [10]. Subharmonic techniques are required when designing in silicon-integrated technologies using frequency multipliers without end-of-chain power amplifiers at the transmitter (TX) and direct-subharmonic mixers without low-noise amplifiers before the receiver (RX) mixer. External lenses offering more than 20 dB of gain enhancement [11], [12] motivate the use of a monostatic transceiver with a single on-chip antenna to improve the effective isotropic radiated power (EIRP) and overall signal-to-noise ratio (SNR) at THz frequencies.

This work builds upon the coupler-free monostatic architecture [3] to demonstrate silicon-integrated single-chip transceiver operation at frequencies around 0.88 THz in the same 90-nm SiGe BiCMOS technology with f_T/f_{max} of 300/480 GHz using a common collector architecture operating at the fourth harmonic.

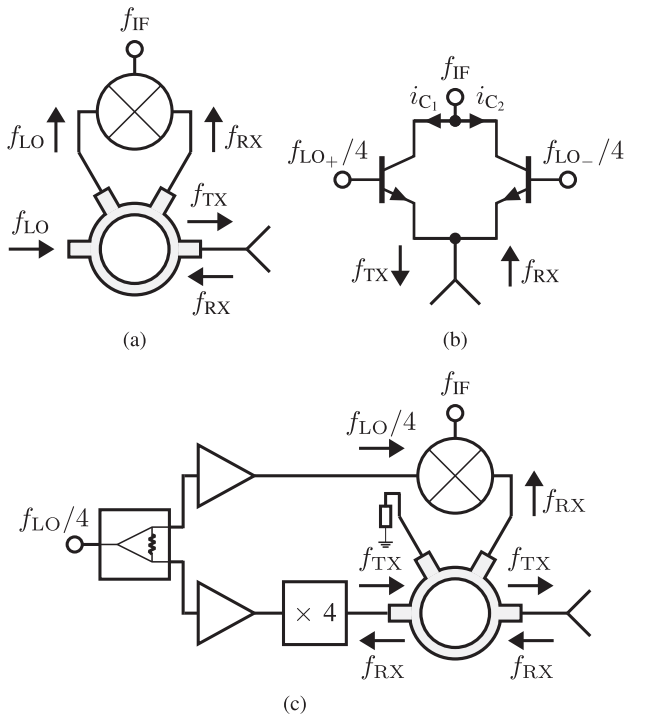

Fig. 1. Illustration of (a) conventional monostatic transceiver with fundamental rat-race coupler, (b) proposed coupler-free transceiver with subharmonic receiver quadrupler, and (c) conventional monostatic transceiver with fundamental rat-race coupler and division of the LO path before the coupler at the fourth subharmonic frequency.

II. Circuit Design

The conventional rat race coupler architecture, illustrated in Fig. 1(a) would require 3–5-dBm input driving levels at a

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fundamental frequency of 1 THz, considering typical total insertion losses of 3–5 dB from the coupler and a 0-dBm local oscillator (LO) input power requirement for the fundamental-frequency mixer. The achievable LO output power around 1 THz is far below 3 dBm, demonstrated in a 0.92-THz frequency quadrupler with −17 dBm peak output power [13] and a 1-THz spatially power-combined 42-element free-running radiator with an output power of −11 dBm [14]. To relax the LO power requirements, a fourth-harmonic architecture can be implemented, for example, highlighted in Fig. 1(c), where the LO path is split prior to the coupler and a fourth-harmonic mixer is implemented at frequencies where the LO amplitude is significantly higher. Nevertheless, insertion losses may exceed 3–5 dB due to difficulties implementing a matched termination as well as overall impedance matching on all four ports of the coupler is very challenging, considering impedance mismatch due to manufacturing tolerances at the antenna and the circumstance that transistor models are fitted at frequencies roughly an order of magnitude below the intended frequency. Therefore, an architecture without a rat race coupler, as depicted in Fig. 1(b) is preferred to realize monostatic operation at 1 THz.

Following the analysis from [3], the expression for the sum of the collector currents of the integrated common collector quadrupler mixer, depicted in Fig. 1(b) is given as

$$i_{C_1}(t) + i_{C_2}(t) = 2I_S e^{\frac{V_{be}}{V_T}} \left(I_0(z) + I_0(z)\frac{V_{RF}}{V_T}\cos(\omega_{RF}t) \right.$$
$$+ 2I_2(z)\cos(2\omega_{LO}t) + I_2(z)\frac{V_{RF}}{V_T}\cos((2\omega_{LO} \pm \omega_{RF})t)$$
$$\left. + 2I_4(z)\cos(4\omega_{LO}t) + I_4(z)\frac{V_{RF}}{V_T}\cos((4\omega_{LO} \pm \omega_{RF})t) \right) \quad (1)$$

up to the fourth order of modified Bessel functions of the first kind $I_n(z)$, with saturation current I_S, $V_T \approx 26\,\text{mV}$ at room temperature, dc base-emitter voltage V_{be}, radio frequency (RF) amplitude V_{RF}, RF angular frequency ω_{RF}, LO amplitude V_{LO}, LO angular frequency ω_{LO}, and $z = V_{LO}/V_T$. The undesired radiation at $2\omega_{LO}$ is attenuated by the on-chip patch antenna, designed at $4\omega_{LO} = 0.88$ THz, with a simulated realized gain G_{ANT} of 6.5 dBi. The × 12 frequency multiplier and the final subharmonic mixer quadrupler have been designed with comparable biasing and transistor sizing as in [3]. Fig. 2(a) depicts the overall on-chip antenna geometry with simulated return loss S_{11} and simulated realized gain shown in Fig. 2(b) and (c). The antenna is fed using a direct via stack from the emitters of the common collector harmonic mixer doubler at an inset of around 6.5 μm from the wider edge of the central patch. A via at the $\mathbf{E}_0$ position of the central patch, located on the topmost aluminum pad layer connects to the metal 5 ground plane for a dc connection. Fig. 2(d) and (e) demonstrates the simulated S_{11} and simulated realized gain for the fundamental and second harmonic. A peak realized gain of 7 dBi with an overall system efficiency of 70% is simulated at 0.91 THz and the idle frequencies at the fundamental and the second harmonic are attenuated by at least 25 dB. The impedance at the idle

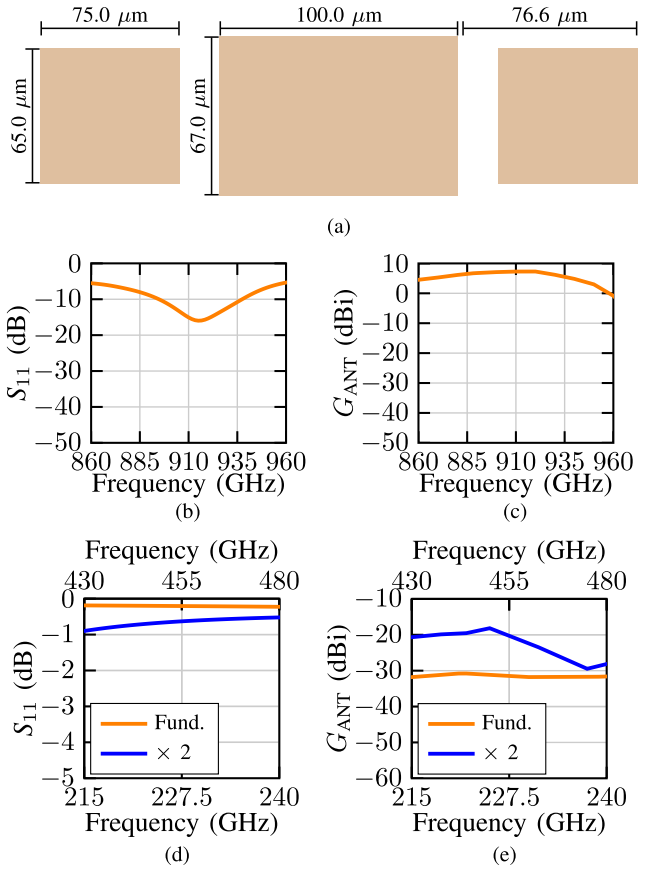

Fig. 2. Antenna (a) dimensions, simulated, (b) S_{11}, (c) realized gain, (d) S_{11} at fundamental and second harmonic, and (e) realized gain at fundamental and second harmonic.

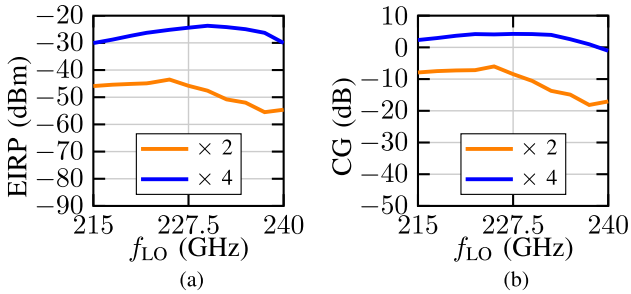

Fig. 3. Simulated (a) EIRP and (b) system conversion gain for second and fourth harmonic versus fundamental frequency.

frequencies is a short circuit with a series resistance of 1.2 and 2 Ω and an equivalent series inductance of 11 and 1.2 pF at a fundamental of 222 GHz and a second harmonic of 444 GHz, respectively. Harmonic balance simulations using a harmonic port with simulated idle-frequency antenna impedances reveal a reduction in output power of 13 and 9 dB when compared to a 50-Ω termination at the undesired idle frequencies of 227.5 and 455 GHz, respectively. Simulated EIRP and conversion gain is illustrated in Fig. 3(a) and (b) for the second and fourth harmonic with input LO frequency.

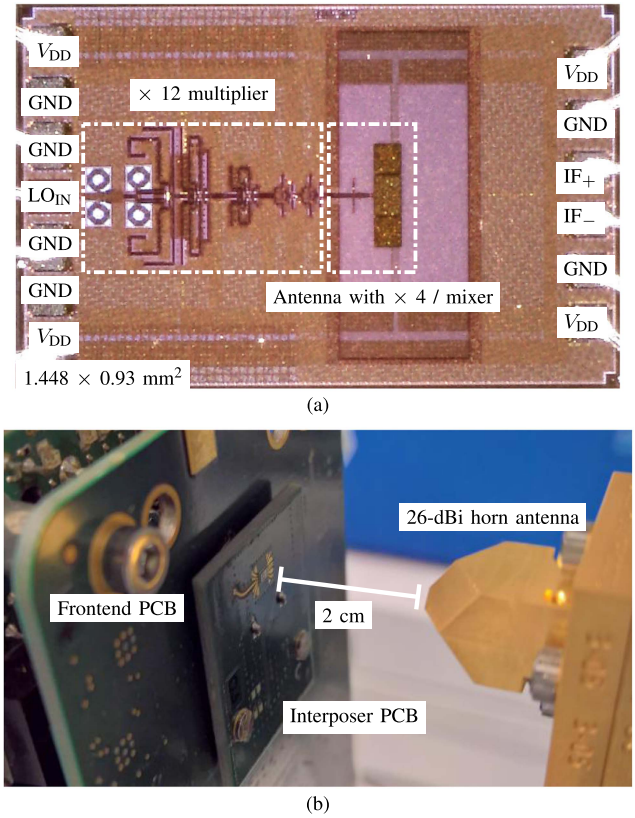

Fig. 4. Photograph of (a) wire-bonded 0.88-THz transceiver chip on interposer PCB and (b) EIRP measurement setup using WR1.0 VDI SAX and 26-dBi SGH with interposer PCB attached to front-end PCB.

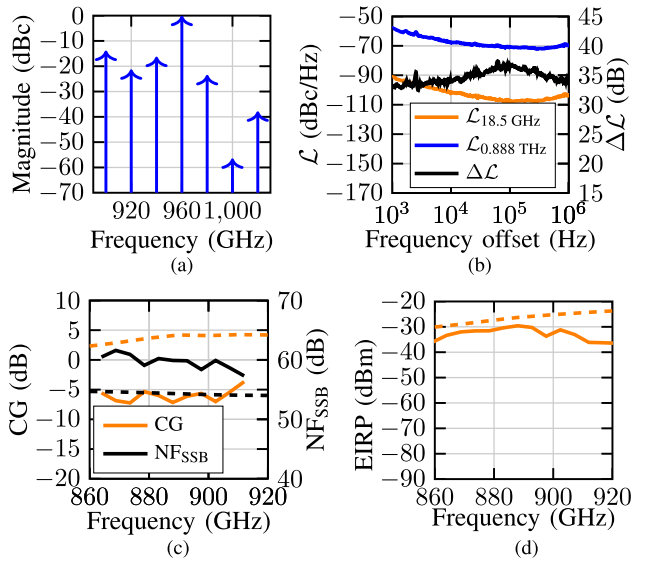

Fig. 5. (a) Measured relative amplitude of multiplied harmonic content with 20-GHz LO input. (b) Phase noise measurement of 18.5-GHz APSIN26G source, 18.5-GHz APSIN26G source multiplied to 0.888 THz and resulting phase noise translation ($\Delta\mathcal{L}$). (c) Measured (solid) and simulated (dashed) system receiver gain and noise figure at $f_{IF} = 100$ kHz using the gain method from [15]. (d) Measured (solid) and simulated (dashed) EIRP.

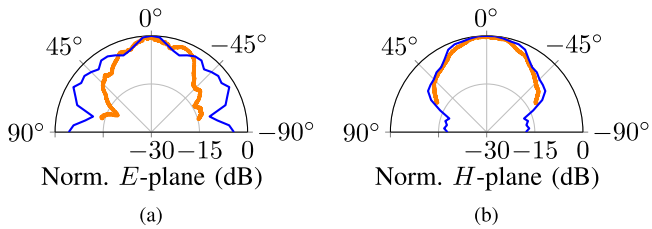

Fig. 6. Measurement (–) and simulation (–) of the normalized beam pattern of (a) E-plane and (b) H-plane at 0.888 THz.

III. Measurements

The 0.88-THz transceiver is characterized in an optical bench-like setting, with the transceiver chip, shown in Fig. 4(a), attached and wire-bonded to an interposer printed circuit board (PCB). In Fig. 4(b), the interposer PCB is mounted on a front-end PCB and separated 2 cm to a 26-dBi Virginia Diodes (VDI) diagonal horn antenna on a WR1.0 VDI spectrum analyzer extender (SAX) for EIRP measurements. A Keysight PXA N9030B signal analyzer is interfaced with the VDI SAX. The manufacturer-provided conversion loss table of the VDI SAX is used for the harmonic-content and EIRP measurements, depicted in Fig. 5(a) and (d), respectively. A peak EIRP of −30 dBm was measured at 0.888 THz, equivalent to an output power of −36 dBm when considering a simulated realized antenna gain of 6.5 dBi. The simulated EIRP is 5 dB higher compared to the measurement. The harmonic content of a 20-GHz input signal is at least 15 dB below the main carrier at 0.96 THz. For conversion gain (CG) and single-sideband noise figure (NF_{SSB}), a second 0.88-THz transceiver is characterized for EIRP and used as a TX source for the first 0.88-THz transceiver, operating as a RX. A peak system CG of −4 dB and a corresponding NF_{SSB} of 57 dB is measured at 0.912 THz.

In addition, the phase noise of a 18.5-GHz input signal and the corresponding × 48 output signal was measured by connecting the VDI SAX-downconverted signal to the R&S FSW-85 signal and spectrum analyzer. The phase noise translation due to the × 48 frequency multiplication is ideally 33.6 dB, compared to 33–37 dB from the results in Fig. 5(b). The 0.88-THz transceiver is mounted on a rotary mount for normalized antenna pattern measurements in Fig. 6(a) and (b), using the EIRP measurement setup of Fig. 4(b). H-plane measurements agree well with the simulations, although E-plane measurements deviate from simulations, possibly due to obstructions such as the bondwires. At 0.444 and 0.222 THz, the EIRP is measured to be 7 and 4 dB, respectively, below the EIRP at 0.888 THz. The RX CG on the other hand is attenuated by 20 and 24 dB at 0.444 and 0.222 THz, respectively. Therefore, future iterations of this design may explore the use of a filter between the integrated 0.88-THz harmonic quadrupler mixer and the radiating antenna for further attenuation of the undesired radiation at 0.444 and 0.222 THz, or alternatively, mounting an external THz filter above the 0.88-THz transceiver.

Overall, the presented and characterized 0.88-THz transceiver is the first demonstration of a monostatic architecture around 1 THz in a silicon-integrated technology. Phase noise measurements at 0.888 THz reveal −70 dBc/Hz at 1-MHz offset with a 18.5-GHz input signal, following theoretical phase noise scaling due to frequency multiplication. Recent phase-locked loop progress at 20 GHz achieving a phase noise of −125 dBc/Hz [16] at 1-MHz offset can further improve the achievable phase noise

by around 20 dB. The integration of the single on-chip antenna with the final common collector harmonic mixer quadrupler allows this transceiver to be fully compatible with gain-enhancing lenses for future imaging and radar applications, for example.

IV. Conclusion

A combined fourth-harmonic mixer and frequency quadrupler is designed using a common collector harmonic mixer and frequency multiplier topology for a monostatic transceiver at around 0.88 THz in a 90-nm SiGe BiCMOS technology with an $f_T/f_{\max}$ of 300/480 GHz. The 1.35-mm^2 transceiver demonstrates a measured peak EIRP of -30 dBm and a minimum single-sideband noise figure of 57 dB, while consuming 144 mA when connected to a 3.3-V supply.

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