Monolithic Integration of a Wafer-Level Thin-Film Encapsulated mm-Wave RF-MEMS Switch in BEOL of a 130-nm SiGe BiCMOS Technology

Alexander Göritz, Selin Tolunay Wipf, Martin Drost, Marco Lisker, Christian Wipf, Matthias Wietstruck, and Mehmet Kaynak

***Abstract*— One of the most significant challenges for the fabrication of any microelectro-mechanical-system (MEMS) device is the low cost and high throughput packaging of the device to protect it from the environmental particles, moisture, and contaminations. In this work, an RF-MEMS switch for millimeter-wave (mm-wave) applications is monolithically integrated into the aluminum-based back-end-of-line (BEOL) of a 130-nm bipolar CMOS (BiCMOS) technology by wafer-level thin-film encapsulation (WLE). Both wet and vapor release techniques are developed and demonstrated for the release of the MEMS device, prior to wafer-level encapsulation packaging. The final device encapsulation is realized as wafer-level packaging with a 3-μm thick metal grid using a stack of Ti/TiN/AlCu/Ti/TiN layers. Finally, a silicon dioxide deposition process with a high deposition rate (HDR) is applied for the full encapsulation of the release holes. The impact of the encapsulation on the RF-MEMS switch performance is evaluated by low-frequency *C–V* and high-frequency *S*-parameter measurements at *D*-Band. The results indicate the full function of the device without a significant performance drop. The encapsulation does not require an extra mask and it is developed as 8-in wafer-level process, thus providing a low cost and high throughput solution for RF-MEMS device encapsulation and packaging.**

***Index Terms*— Bipolar CMOS (BiCMOS), millimeter-wave (mm-wave), packaging, RF-microelectro-mechanical-system (MEMS) switch, wafer-level thin-film encapsulation (WLE).**

I. Introduction

THE continuous interest in microelectro-mechanical-system (MEMS) devices in the last decades have found its market mainly in the areas of accelerometers, inkjet printer heads, microphones, projection display chips, blood and tire pressure sensors, and gyroscopes, mainly dc or low-frequency applications. Although RF-MEMS devices were introduced a couple of decades ago, the market penetration of RF-MEMS has been mainly hampered due to the required reliability specifications, which are very much related to the packaging type and the environment.

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The authors are with the IHP–Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt, Germany (e-mail: goeritz@ihp-microelectronics.com).

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The main fields of applications for the RF-MEMS devices are switching networks, mobile phones, automotive, and consumer electronics [1]–[3]. As an example, the global internet traffic of tablets and smartphones is still growing with an annual growth rate of about 25% from 2014 to 2019 [4], [5]. In such devices, the input and output matching networks, hence, the impedance matching has to be controlled by switches with high performance and low power consumption. For such applications, a promising candidate is the RF-MEMS shunt switch, where a significant capacitance change can be achieved which changes and controls the total impedance [6]. The process integration of an RF-MEMS switch has to be well structured as it determines not only the final performance of the device but also the cost, yield, and reliability. The integration scheme is strongly influenced by the technology environment in which the device is planned to be integrated [7]–[14]. Due to the strong need for high-voltage and control circuits for RF-MEMS devices, a full CMOS or bipolar CMOS (BiCMOS) integration is desired [15]–[17]. Such a monolithic integration provides the shortest connection between the RF-MEMS switches and the high-voltage and control electronics. Monolithic integration can be obtained either by realizing the RF-MEMS switches before the CMOS fabrication, by embedding the switches into the available CMOS or BiCMOS process flow [i.e., intra-CMOS or back-end-of-line (BEOL)], or by adding additional process steps after finalizing the BiCMOS process (i.e., post-CMOS). Either way has its own advantages and limitations, whereat every technique leads to a compromise between the thermal budget, CMOS compatible materials, design rules, and fabrication costs of the available process integration schemes for the specific RF-MEMS devices. The MEMS integration as pre-CMOS or as intra-CMOS into the front-end-of-line (FEOL) fabrication prohibits metals as MEMS material due to their CMOS incompatibility. On the other hand, both the intra-CMOS integration into the BEOL and the post-CMOS integration limits the MEMS materials due to temperature limitation in order to consider the thermal budget of the FEOL fabrication [18], [19].

Packaging is one of the main challenges for MEMS devices. RF-MEMS devices need more complex packages than any other type of device. Without adequate protection from the environment, the use of the RF-MEMS devices is strongly limited by reliability issues [20]–[22]. The mechanically

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movable parts and the sensitive nature against any particle make the packaging process challenging. In addition, RF-MEMS devices require specific environmental conditions in the packaged cavity for a reliable and stable lifetime operation. Although many different integration techniques have been developed and used to package the RF-MEMS devices [23], the method of wafer-level encapsulation seems to be one of the most promising methods, providing high performance, easy integration to the semiconductor foundry, and lower cost [15]–[17]. In such encapsulation processes, small holes above or around the RF-MEMS device are used to release it. After the release, these holes are closed and the RF-MEMS device is sealed, and thus packaged [24].

In this work, we report a full monolithic process integration of a wafer-level thin-film encapsulated RF-MEMS switch for millimeter-wave (mm-wave) application, embedded in the standard BEOL of the 130-nm SiGe BiCMOS SG13G2 technology of IHP. This technology offers a perfect base for the use of a *D*-band RF-MEMS switch due to its high-performance SiGe heterojunction bipolar transistor (HBT) technology with peak values for the transit frequency (f_T) of 505 GHz and for the maximum oscillation frequency (f_{max}) of 720 GHz [25], [26]. The fabrication of the CMOS and BiCMOS technologies is realized by process flow with more than 750 steps, whereat its qualification is done with a significant effort under different conditions; thus the process flow needs to be well-understood in order to realize a successful RF-MEMS integration without any impact to the standard BiCMOS technology.

The article is structured as followed: In Section II, the BEOL stack of the chosen technology is introduced for the understanding of the underlying process conditions. The scheme for the integration of the RF-MEMS switch is explained in Section III, where the layout view of the device together with the detailed operating principle is also provided. As one of the most crucial steps for the packaging process, the release of the RF-MEMS device is presented in Section IV, where the impact of different releasing methods and conditions as well as the required process modifications are discussed. In Section V, the encapsulation process is depicted, in particular, the effect of the nondesired deposition of the encapsulation dielectric layer over the contact regions of the RF-MEMS switch. The effect of the releasing hole dimension on the sealing performance is also presented. The results of C–V and S-parameter measurements, showing the effect of the encapsulation on the performance of the RF-MEMS device are discussed in Section VI. Finally, the article is concluded with some general remarks in Section VII.

II. 130-nm SiGe: C BiCMOS Technology: BEOL Details

The main goal of the chosen process integration scheme is maximizing the electrical and mechanical performance, increasing the yield, and minimizing or avoiding the additional mask layers and process steps from the standard BiCMOS process flow, thus simplifying the process integration.

The standard BEOL of the 130-nm SiGe BiCMOS technology used in this study is a sequence of silicon dioxide (SiO_2) and metal stacks, finalized with passivation, which is based on SiO_2 and a silicon nitride (Si_3N_4) layers. The technology has seven metallization layers in the BEOL stack, which are connected by tungsten (W) via-plugs.

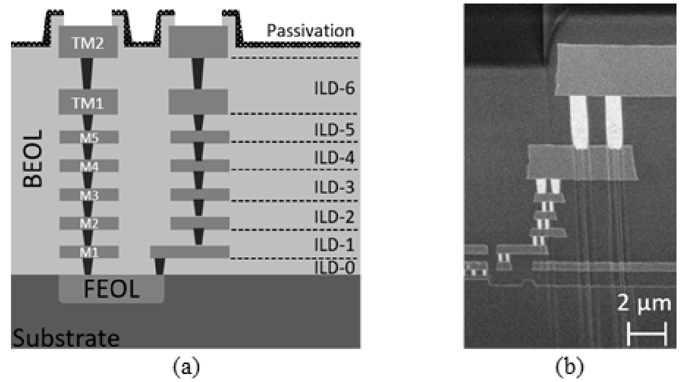

Fig. 1. (a) Cross-section of full 130-nm BEOL as generic and (b) FIB-SEM image.

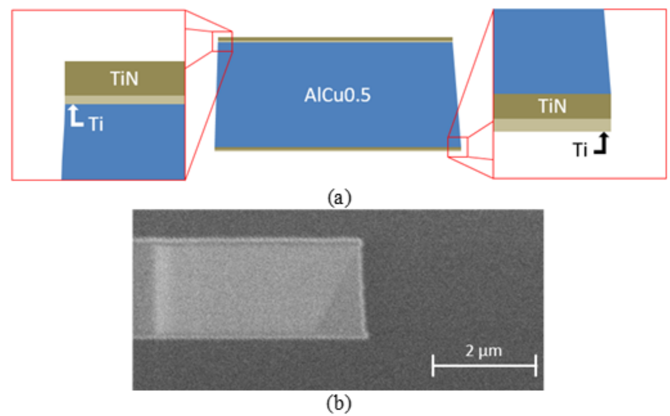

Fig. 2. (a) TM1 stack as generic and (b) as FIB-SEM image.

In Fig. 1, the cross-sectional views of the BiCMOS technology are given. Fig. 1(a) shows the generic cross-section of the technology while Fig. 1(b) is taken by scanning electron microscopy (SEM) after a cross-section preparation by focused ion beam (FIB). Each metallization layer is a stack of Ti/TiN/AlCu/Ti/TiN, from bottom to top (Fig. 2). The lower five metal layers [metal 1 (M1) to metal 5 (M5)] consist of thin metal stacks of approximately 500 nm. The upper two metal layers, namely top metal 1 (TM1) and top metal 2 (TM2), are thicker stacks of 2000 and 3000 nm, respectively. Each metal stack is deposited by physical vapor deposition (PVD). The patterning of metal layers is realized by photolithography with wavelengths of both 248 and 365 nm followed by chlorine-based reactive ion etch (RIE).

After the metal pattering steps, a deposition of SiO_2 interlayer dielectric (ILD) deposition follows. Various types of SiO_2 layers are used during the process for different purposes. The parameters such as level of impurities, growth rate, and mass density of SiO_2 are controlled by precursor, pressure, and energy input during the deposition process which leads to a specific dielectric constant and disruptive strength of the layer. As a high-quality ILD, high-density plasma undoped silicate

TABLE I

SUMMARY OF THE DIFFERENT SILICON OXIDES AND SILICON NITRIDE LAYERS USED IN BEOL STACK INCLUDING THEIR DEPOSITION AND MATERIAL PROPERTIES

	HDP USG	PE-TEOS	HDR SiO_2	Si_3N_4	Si_4N_4 (SiRN)
Temperature ϑ [°C]	400	400	200	400	400
Deposition rate *DR* [nm/s]	10	13	28	18	8
Density ρ [g/cm³]	2.22	2.22	2.11	2.66	2.37
Relative permittivity ε_r [1]	4.6	4.5	4.6	7.3	8.8
Disruptive strength E_d [MV/cm]	4.6	4.1	4.0	4.5	1.2

glass (HDPUSG) is deposited by a special plasma-enhanced chemical vapor deposition (PECVD). The importance of this process is simultaneous deposition and sputtering. Their ratio controls the gap fill and realizes a void-less SiO_2 deposition into metal gaps with high aspect ratios (ARs). After each ILD deposition, chemical mechanical polishing (CMP) is used to provide a leveled ILD. The thicknesses of ILD 1–4, ILD-5, and ILD-6 are targeted as 600, 900, and 3000 nm, respectively. With the defined ILD thicknesses, via plugs are implemented by photolithography and RIE of the via holes. After an ash and wet clean process sequence, thin layers of Ti by PVD and TiN by chemical vapor deposition (CVD) are deposited. In order to complete the via, W is deposited by the CVD process. A CMP step is applied to finish the W-via contacts. A sequence of 1500-nm HDPUSG and 400-nm PECVD-based Si_3N_4 is deposited as the passivation layer. Finally, the contact pads are opened by RIE and cleaned by an ash and wet clean processes, which finalizes the standard BiCMOS process flow. The different types of SiO_2 layers play a crucial role during the release process. Therefore, a summary of different silicon oxides and silicon nitrides used in the BEOL stack, including their deposition and material properties, is provided in Table I.

In this study, some of the aforementioned metallization layers are used as the moving part of the RF-MEMS switch due to their conductive behavior. The ILD silicon dioxide layers are used as sacrificial layers to release the suspended part of the RF-MEMS switch since the SiO_2 layer can be selectively etched against the aluminum-based metallization layers. Section III provides the entire integration scheme of the monolithically integrated RF-MEMS devices.

III. RF-MEMS SWITCH PROCESS INTEGRATION SCHEME IN 130-NM BiCMOS BEOL

Due to the qualified and frozen technologies, most of the changes in the process flow such as thicknesses, material types, or process conditions require a requalification which should be avoided if possible. Therefore, one of the main goals of the process integration scheme is to develop a process flow with minimum change in the qualified BiCMOS flow. Furthermore, the additional number of masks for the integration has to be minimized to keep the overall production costs low. The final performance of the device strongly depends on the process integration scheme, which therefore needs to be carefully studied.

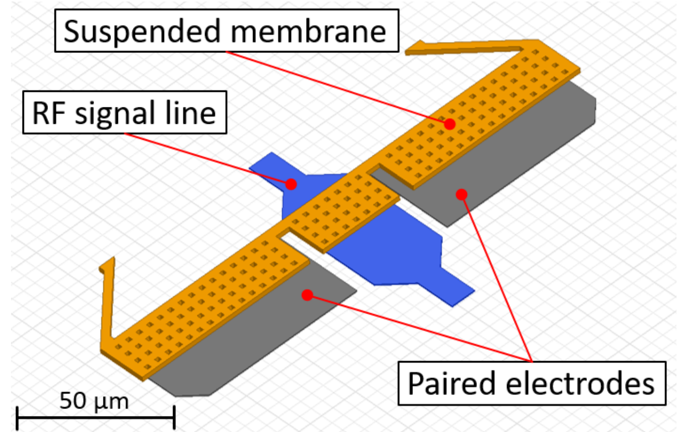

Fig. 3. 3-D model of a RF-MEMS switch with the different functional parts: suspended membrane (orange, for overview halved), RF signal line (blue), and HV electrodes (gray).

The RF-MEMS switch in this study consists of three main parts: a suspended movable membrane, two paired high-voltage electrodes, and the RF signal line (Fig. 3).

The insertion loss (IL) and the isolation (ISO) of the RF-MEMS device are the most critical high-frequency parameters, defining the performance of the device. The IL is strongly affected by the substrate coupling at high frequencies since the silicon substrates used in BiCMOS processes are typically low-resistive (i.e., 50 $\Omega \cdot$ cm). Therefore, the metallization layer used for the RF signal line has to be chosen as M5, in order to realize maximum substrate distance for minimizing the substrate coupling. Considering the need for a suspended membrane in TM1 and an encapsulation grid layer for packaging in the TM2 region, M5 is the most appropriate metallization layer for the RF signal line. Such integration would allow using M4 as the high-voltage electrodes for electrostatic actuation, M5 as the RF signal line, TM1 as suspended movable membrane, and TM2 as the encapsulation shell layer for wafer-level thin-film packaging.

The planned integration scheme is given in Fig. 4. The shape of the membrane plays an important role, as it defines both the distance between membrane and signal line (d_{cont}) and the distance between membrane and electrode (d_{elec}). In order to optimize these parameters, a slightly up-bended suspended membrane (Fig. 5) with a defined bending height is targeted by modifying the thickness of the standard TM1 bottom layers. It is worth mentioning here that the small recipe change of the TM1 layer has no significant effect on the standard BiCMOS process flow; thus electrical properties of TM1 are kept within the qualified process specifications.

With an optimized membrane bending, the overlap region between the membrane and the signal line forms the contact capacitance (C_{cont}), with the strong dependency of d_{cont}, which is used as the controlling parameter for the total capacitance (C_{tot}). In combination with the total inductance (L_{tot}) caused by the membrane and its arms, the resonance frequency of the RF-MEMS switch is set; therefore the operating frequency band, IL, and ISO parameters are defined. Detailed explanations for the operating principles are provided in [27].

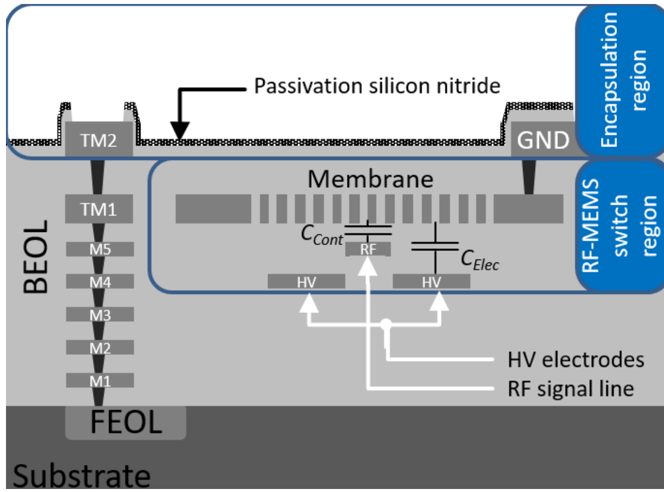

Fig. 4. Schematic cross-section of a not released RF-MEMS switch after standard BEOL fabrication and its localization of the functional parts membrane, RF signal line, and HV electrodes.

In Section IV, the release of the membrane and forming of the suspended RF-MEMS device is discussed for different releasing method and their corresponding impacts.

IV. Release of the RF-MEMS Switch and Its Design Modifications

To release the membrane of the RF-MEMS switch, sacrificial layers of ILD silicon dioxides have to be etched. Two different release techniques have been used, namely HF wet etch and HF vapor phase etch (HFVPE). Both processes have advantages and limitations. The process principle is based mainly on the reaction of HF with SiO_2 to form silicon tetrafluoride (SiF_4) and water (H_2O). Surface processes such as adsorption and diffusion of HF on the SiO_2 surface, and diffusion and desorption of SiF_4 and H_2O from the surface have been extensively considered, as explained in [28].

The aim of the release process is the clean removal of SiO_2 with high selectivity to both the passivation layer (Si_3N_4) and the surrounding metal structures. Table II provides the required process flow, composition, pressure, and temperature details of both processes in detail.

As described under Section II, there are different types of SiO_2 layers in ILD stacks that need to be considered during the etch release process. Table III summarizes the typical etch rate of different silicon oxide and silicon nitride layers, using the two different releasing techniques. The main difference between the releasing techniques is the mole fraction of water during the process. The wet etch solution consists of one-third of deionized (DI) water (H_2O). In contrast, the HFVPE process environment initially consists of about 3.5-vol% H_2O, whereas a small fraction of this creates a film of adsorbed H_2O. Additionally created H_2O, which is formed by the above-mentioned chemical reaction, is in relation to the initial H_2O content in the etchant, significantly larger. The extensive H_2O creation during HFVPE processes, at especially long etch times or high turnovers of SiO_2, cannot be compensated. The consequence is a process parameter shift to a more humid etch environment, which initiates the formation of a metasilicic acid-based residual layer [29].

TABLE II
Comparison of the Two Releasing Methods HF Wet Etching and HFVPE

	Releasing method	
	Wet etch	**HFVPE**
Required Processes	1. HF wet etch 2. Overflow rinse (DI water) 3. Spin rinse dryer (hot nitrogen)	1. HF vapor phase etch
Composition	3.3 Vol.-% Fluoric acid 29.2 Vol.-% Ammonium fluoride 34.2 Vol.-% DI water 33.3 Vol.-% Ethylene glycol	62.0 Vol.-% Hydrogen fluoride 3.5 Vol.-% DI water (vaporized) 34.5 Vol.-% Nitrogen (carrier gas)
Process pressure *p*	760 Torr	9 Torr
Temperature ϑ	ϑ_{fluid} = RT (room temperature)	ϑ_{chuck} = 5°C, ϑ_{wall} = RT

TABLE III
Etch Rates of Wet and Vapor Etch Techniques

	Wet etch [nm/min]	HFVPE [nm/min]
Oxides		
HDPUSG	50	470
PE-TEOS	60	475
HDR	250	1500
Nitrides		
PE-Si_3N_4	2.7	5.3
PE-Si_4N_4 (SiRN)	0.7	1.3
TiN	~ 0	~ 0
Metal compounds		
AlCu	2.5	~ 0

The HFVPE method can achieve significantly higher etch rates compared to the wet etch process thus, shortening the processing time of the release. Regarding the etching of HDPUSG, the HFVPE process has a selectivity of about 89 against the standard plasma-enhanced (PE)-Nitride (Si_3N_4). In contrast, the selectivity of the respective wet process is about 19. However, when using silicon-rich nitride (SiRN, Si_4N_4) instead of Si_3N_4, the selectivity values are 362 and 71 for the vapor and wet etch cases, respectively. Such high selectivity values allow the use of SiRN also as a hard mask and etch stop layer, as well. Moreover, the selectivity against TiN is significantly high for both methods. Furthermore, a very high selectivity to AlCu can only be achieved by the HFVPE process. In the case of the wet release process, the maximum

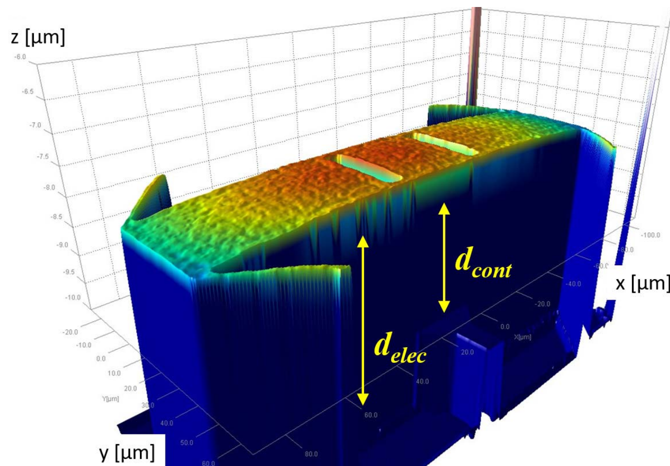

Fig. 5. Measured 3-D profile of up-bended TM1 membrane, including drawn-in distances d_{cont} and d_{elec}.

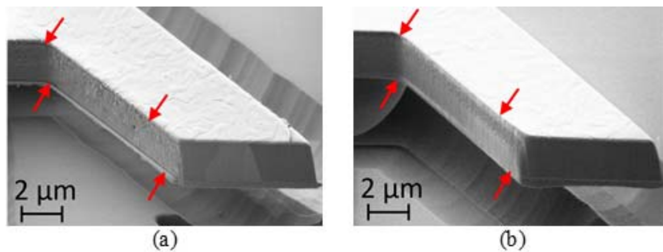

Fig. 6. FIB-SEM image section of a membrane suspension arm of a wet etch released switch (a) in comparison to HFVPE released switch (b), including marks for the laterally accessible AlCu.

selectivity against AlCu is 20. The effect of the limited selectivity against AlCu is given in Fig. 6. The unintentional etch of AlCu reduces the overall width of the membrane arms. Although the small undercut of the AlCu has a negligible effect on the electrical properties of the membrane arm, it has a major effect on the electromechanical dynamics of the RF-MEMS switch.

In summary, the HFVPE process provides a more selective and significantly faster-releasing method. However, it needs some design adjustments to solve issues such as residuals after release and process robustness against process parameter shift. Despite the fact that the vapor etch technique can provide faster etch rates and higher selectivity values, the wet etch release process has the advantage of less residuals and high process robustness. Nevertheless, vertical and lateral etch stops are needed for both methods.

In conclusion, the wet etch process is preferred as the release method for this study. As a consequence, the undesired AlCu etch has been carefully controlled to achieve the final specification of the RF-MEMS switch. In the following sub-chapters, different methods of etch control based on the aforementioned results regarding selectivity are discussed.

A. Vertical Etch Stop

Besides the use of SiRN as a hard mask, it is also used as an etch stop layer for the vertical etch stop (VES) during the RF-MEMS release. Vertical boundaries, which are formed by the SiO_2 deposition on a patterned layer such as the TM1

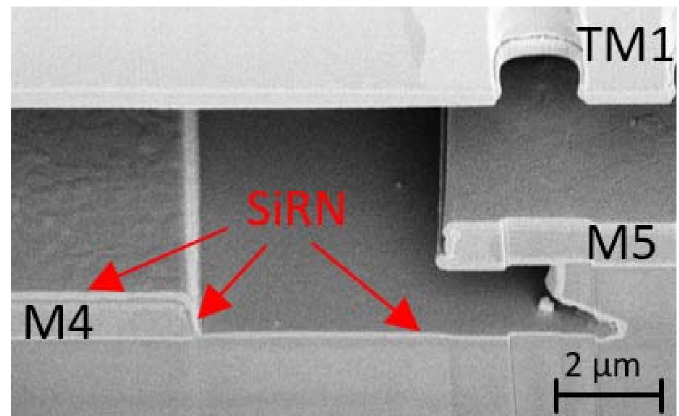

Fig. 7. RF-MEMS cut-out of a SiRN protected HV electrode (M4) as FIB-SEM image cross-sections.

membrane, lead to a locally higher vertical etch rate; therefore, the high-voltage electrodes are reached by the etchant before the entire membrane is completely released [30]. If a VES layer is not used, there is a risk of release of the high-voltage electrodes which may lead to a partial move up when a high actuation voltage is applied. This would yield the risk of a short circuit between the high-voltage electrodes and the movable membrane. Thus, the use of the SiRN-based VES avoids any partial release of the high-voltage electrodes, and also it provides an electrical insulation from the grounded RF-MEMS membrane.

The deposition of a 100-nm thin SiRN VES layer has been developed intended on top of the patterned M4, where HV electrodes are realized. Fig. 7 shows a SEM image of HV electrodes at the M4 layer with SiRN-based VES (red arrows) after the release process. It is clearly seen that there is no under etch of the electrode, ensuring that a well-defined vertical interface is achieved for a reliable operation of the RF-MEMS switch.

B. Lateral Etch Stop

Similar to the control of the vertical etch using the VES layer, the lateral etch should also be controlled. Fig. 8(a) displays an FIB-SEM cross-section of a test RF-MEMS releasing process. Fig. 8(b) and (c) show the schematic view of the cross-section of the same BEOL layer stack, which consists of HDPUSG, PE tetraethoxysilane (PE-TEOS), and the SiRN-based passivation layer. The obvious lateral etch rate difference can be seen in the same figure. A typical isotropic etch condition is provided in Fig. 8(b), whereas a boundary etch condition is marked in Fig. 8(c) for comparison.

In general, the silicon dioxide etch rate is higher when the mass density is lower. However, in this particular case, different types of SiO_2 are stacked which creates several horizontal boundary layers with higher etch rates compared to the bulk of the layer. This is due to the fact that the deposition of an individual ILD oxide layer is performed in three phases namely, the beginning phase, bulk phase, and ending phase. The SiO_2 mass densities created during the beginning and the ending phases are smaller in comparison to the bulk phase due to different deposition conditions. Furthermore, the HDPUSG

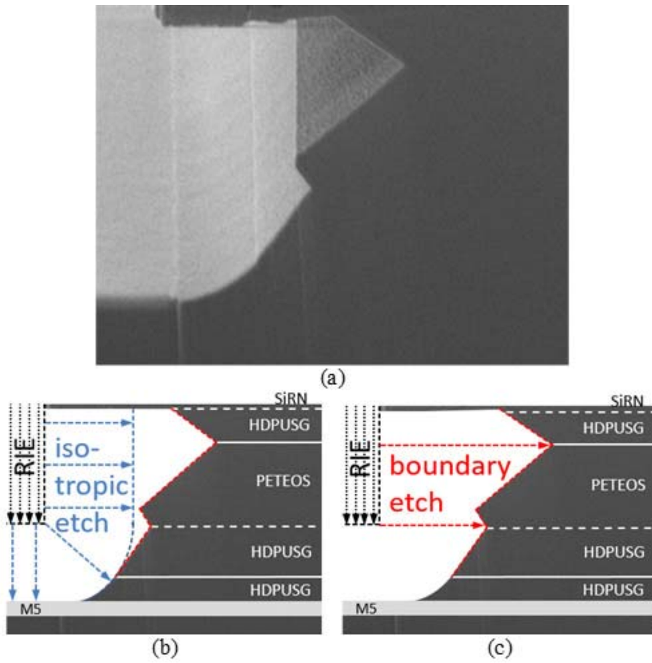

Fig. 8. (a) Etch effect on boundary layers of oxide depositions shown on side part of a released switch as FIB-SEM image of the cross-section. (b) Schematic view of the cross-section with detailed oxide types including the expected isotropic etch (blue dashed line). (c) Unexpected boundary etch.

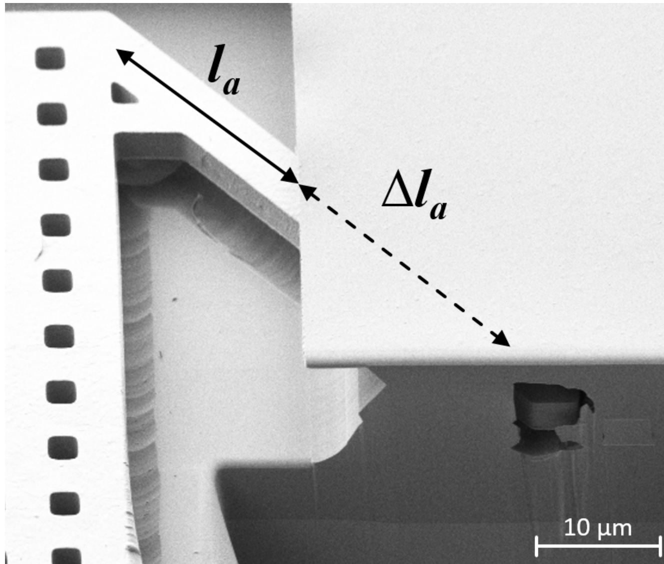

Fig. 9. FIB-SEM image of a significantly more released suspension arm caused by both the higher etch rate of the SiO_2 liner on TM1 and the thermo-mechanically stressed SiO_2 close to the TM1 side.

recipe contains an additional predeposition of a thin SiO_2 liner, which has a higher wet etch rate (65 nm/min, compared to 50 nm/min for bulk HDPUSG).

Another significant lateral etch challenge is the etch rate of the SiO_2 volume surrounding the metal structure. Due to the thermo-mechanical stress induced by the thermal expansion at the process temperature of more than 400 °C (i.e., during SiO_2 or tungsten depositions), the etch rate of the stressed layers gets significantly higher. Fig. 9 shows a SEM image after a wet etch release, where the increased etch rate of the SiO_2

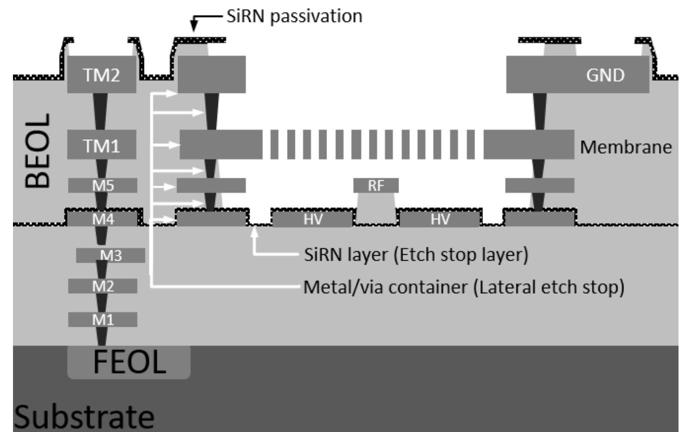

Fig. 10. Schematic of a pad opened RF-MEMS switch including the VES on M4 and the mLES.

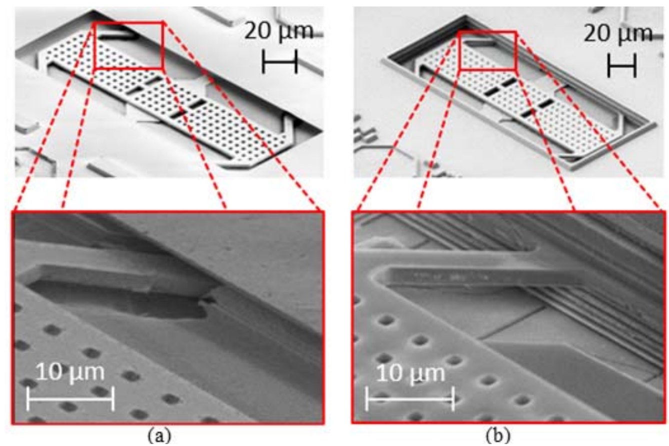

Fig. 11. SEM images (top) and FIB-SEM cross-sections (bottom) of the RF-MEMS switch (a) without metal container-based mLES and (b) with included metal container-based mLES.

surrounding TM1 is clearly shown. The effect of this undesired high etch rate around the metal layers results in an effective suspension arm length of $l_a + \Delta l_a$, instead of the intended length of l_a. The consequence is the longer suspension arms, which are too flexible and make the devices less reliable.

Moreover, the control of the lateral etch around the metal arm gets difficult, which reduces the yield. Out of these results, the main problem can be summarized as the lack of a lateral etch stop layer to control the release etch. In order to overcome this, a metal-based lateral etch stop (mLES) is designed using stacked vias and metals between M4 and TM2, as shown in Fig. 10. Fig. 11 shows two RF-MEMS switches, released without Fig. 11(a) and with Fig. 11(b) mLES approach, showing that in contrast to the RF-MEMS switch without lateral etch stop [Fig. 11(a)], both the membrane position and arm length of the RF-MEMS switch with mLES [Fig. 11(b)] are well defined. A significantly better control of the lateral etch is therefore achieved using the mLES approach.

C. Leveled Passivation

As described under Section III, the TM2 layer is planned as the encapsulation layer. However, the nonflat passivation topography of the BiCMOS process makes this challenging.

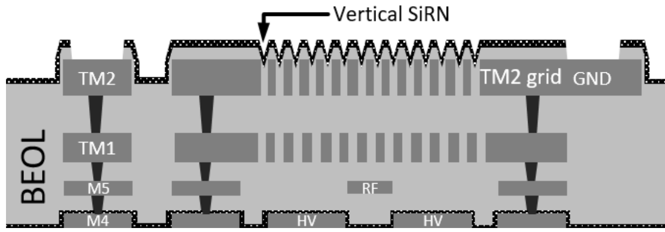

Fig. 12. Schematic of a pad opened RF-MEMS switch with an integrated TM2 grid above the TM1 membrane.

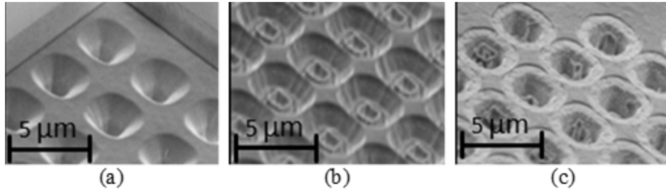

Fig. 13. SEM images of the designed TM2 grid in standard BEOL (a) after passivation deposition of both SiO_2 and SiRN, (b) after passivation opening by RIE, and (c) after MEMS release attempt.

A schematic cross-section of an encapsulation grid implemented in TM2 of the standard BEOL is depicted in Fig. 12, showing that the SiRN used for both passivation and hard mask, has a vertical component. The topography of the standard BEOL leads to a vertical deposition of the passivation SiRN, hence, does not allow to open fully the encapsulation holes. Fig. 13 displays SEM images from different phases in the passivation opening sequence on a TM2 grid for the standard process. Fig. 13(a) shows the grid region after the passivation oxide and SiRN deposition, while Fig. 13(b) shows the same region after the dry etch step of passivation. It can be seen that the vertical SiRN is not completely removed. Finally, a release attempt by wet etch [Fig. 13(c)] shows that the faster etch rate of SiO_2 against SiRN causes remaining SiRN particles, which blocks the wet releasing process through the holes of the TM2 grid. Therefore, planarization of the passivation SiO_2 is necessary before the SiRN deposition. This additional process sequence consists of a SiO_2 deposition and a subsequent CMP process before the SiRN deposition. This way, a fully horizontal and flat deposition of the SiRN passivation is realized above the TM2 grid. Fig. 14 shows SEM images of the encapsulation metal grid after passivation deposition of SiO_2 and SiRN [Fig. 14(a)], the MEMS area opening of the SiRN passivation by RIE [Fig. 14(b)], and the wet release of the RF-MEMS switch [Fig. 14(c)]. It is clearly seen that the problem of residual SiRN particles is avoided by this process flow which allows an effective wet etch release process.

V. Encapsulation of RF-MEMS Switch

A. Encapsulation Process

As the last part of the encapsulation packaging process, the open metal grid holes in TM2 have to be sealed for a full ISO of the RF-MEMS device. The process temperature should be kept as low as possible to not affect the mechanical stress behavior of the suspended membrane. Previously performed

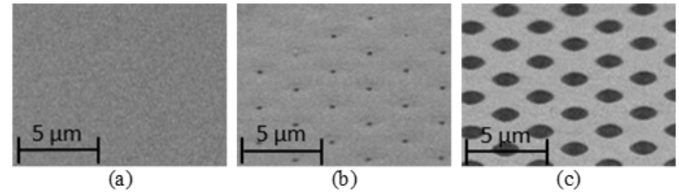

Fig. 14. SEM images of the designed TM2 grid in leveled BEOL (a) after passivation deposition of both SiO_2 and SiRN, (b) after passivation opening by RIE, and (c) after MEMS release attempt.

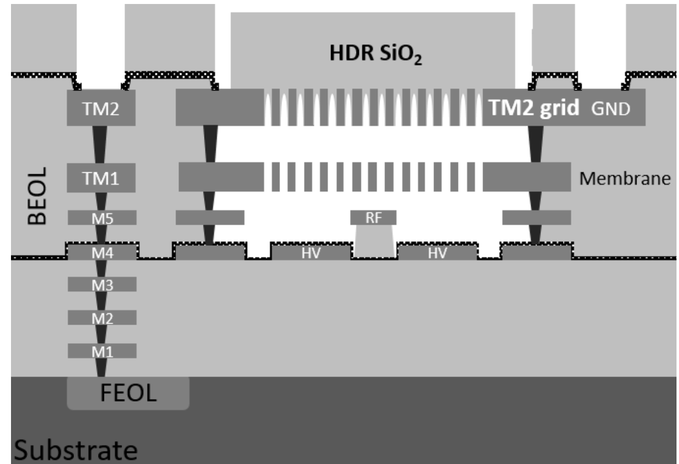

Fig. 15. Generic of an initially encapsulated RF-MEMS switch.

temperature tests on a released membrane have shown that a postprocess temperature of below 250 °C has no significant effect on the suspended structure. A deposition temperature of 200 °C has been used for the SiO_2 deposition process, with a deposition rate (DR) of 1680 nm/min and a very low bottom and step coverage. The SiO_2 has a low mass density due to the low deposition temperature, which is required for the encapsulation process. The schematic cross-section is given in Fig. 15.

B. Determination of the Ideal Grid Hole Size in Standard TM2

Another crucial aspect is the size of the holes. They were investigated regarding reproducibility and the ability to close them with the high deposition rate (HDR) SiO_2 deposition process. Both the hole width (h_w) and hole spacing (h_s) parameters are optimized to achieve the best encapsulation condition.

For the initial tests, four different hole widths were prepared. Fig. 16 illustrates the metal grids with hole width values of 1.25, 1.5, 1.75, and 2.0 μm. Considering the TM2 thickness (d_{TM2}) of 3 μm, the ARs ($\mathrm{AR} = d_{\mathrm{TM2}}/h_w$) are 2.4, 2.0, 1.7, and 1.5, respectively. For reproducibility of the TM2 grid, a hole width of 1.25 μm is identified as the minimum limit. Fig. 17 shows the FIB-cut SEM photographs of the different grid hole dimensions. In terms of the encapsulation ability with a 4000-nm HDR deposition, the hole diameters of 1.75 and 2.0 μm, closing of the grid could not be achieved [Fig. 17(a) and (b)]. The best results have been achieved for

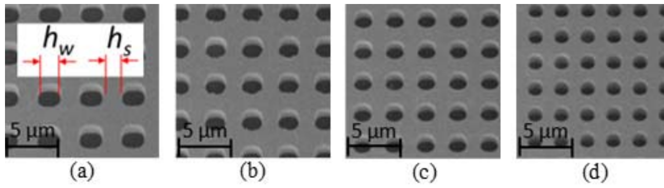

Fig. 16. SEM images about the hole diameter variation with diameters h_w of (a) 2.0 μm, (b) 1.75 μm, (c) 1.5 μm, and (d) 1.25 μm.

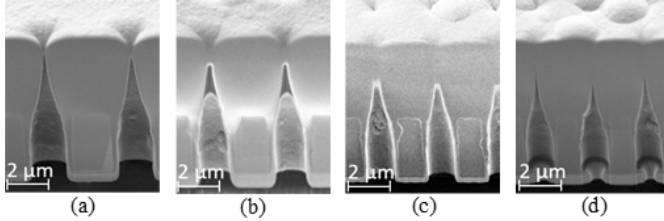

Fig. 17. FIB-SEM images of the SiO_2-deposited WLE hole diameters in TM2 with h_w of (a) 2.0 μm, (b) 1.75 μm, (c) 1.5 μm, and (d) 1.25 μm.

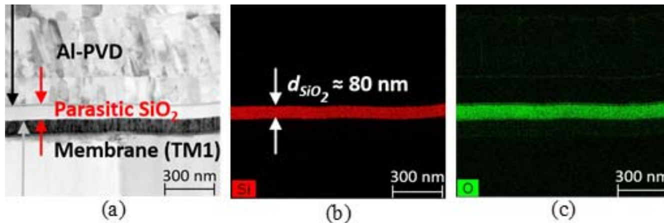

Fig. 18. Investigation results of the parasitic SiO_2 deposition on top of the membrane inside the cavity for a TM2 grid ($h_w = 1.5$ μm) as (a) TEM image, (b) EDX image for silicon, and (c) EDX image for oxygen.

the widths of 1.25 and 1.5 μm [Fig. 17(c) and (d)]. The width of 1.5 μm has therefore been identified as the best compromise between the reproducible fabrication of the grid and the ability to close it.

However, the encapsulation SiO_2 also grows in the cavity, particularly around the contact area of the RF-MEMS switch, thus affecting the electrical performance of the device. First, unwanted deposition of the parasitic SiO_2 layer has an effect on the mechanical behavior of the suspended membrane.

In order to determine the thickness of parasitically deposited SiO_2 on top of the membrane inside the cavity, the following technique has been used. First, the encapsulation has been mechanically removed by an adhesive strip. Afterward, an aluminum layer has been deposited by PVD in order to protect the parasitic SiO_2 from contaminations due to a subsequent lamella preparation by FIB. This lamella is investigated by transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDX). As a result, the encapsulation of a TM2 grid leads to a deposition of a parasitic SiO_2 film with a thickness of about 80 nm on top of the membrane inside the cavity, as given in Fig. 18.

Using the estimation of Stoney's equation for an 80-nm HDR SiO_2 deposition on a silicon test wafer, the intrinsic layer stress (σ_{lay}) has been determined with approximately -180 MPa. Due to an ash process, which is applied for mask removal after a reopening of the pads, this compressive stress state is changed to the tensile stress direction. This tensile stress slightly lifts up the membrane position and decreases the membrane bow. In sum, the distance between the membrane and that between the signal line and electrode are increased more significantly. The consequence is a significantly lower contact capacitance which degrades the ISO. It also increases the pull-in voltage for the electrostatic actuation. Therefore, a low bottom and step coverage deposition process is required to encapsulate the released RF-MEMS device with a minimum amount of SiO_2 deposition inside the cavity.

TABLE IV
COMPLETE PROCESS FLOW FOR WLE ON RF-MEMS

1. Standard fabrication of FEOL & BEOL until patterned M4
2. Insertion of SiRN based VES
3. Fabrication from ILD4 oxide deposition to W CMP (TV1)
4. Deposition of stress compensated TM1 layer stack
5. Fabrication from TM1 patterning to HDPUSG on TM2
6. Deposition of an additional SiO_2 layer (PETEOS)
7. CMP of additional SiO_2 layer
8. Pad patterning
9. Deposition of SiRN passivation
10. Patterning of smaller pads
11. MEMS area patterning
12. MEMS releasing process
13. Deposition of HDR SiO_2
14. Final pad patterning (2nd time)

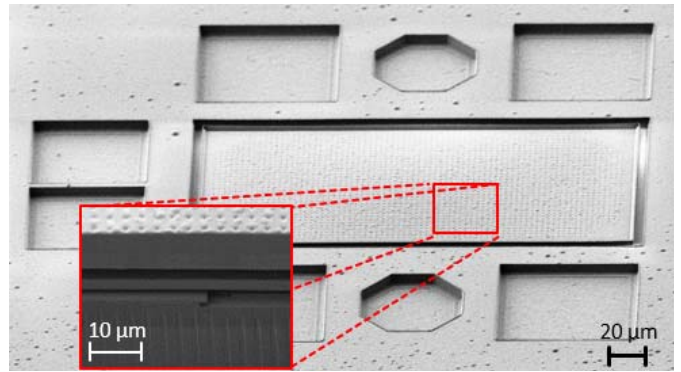

Fig. 19. SEM images of a finished encapsulated RF-MEMS switch.

C. *Final Process Flow of the Wafer-Level Thin-Film Encapsulation Process Integration*

The final process flow mainly consists of standard process steps, which are summarized and listed in Table IV. In addition to the more than 750 steps of the full BiCMOS flow, 56 RF-MEMS steps are added including three additional photolithography masks for the MEMS release. After the application of the complete process flow, the fabrication of a wafer-level thin-film encapsulated RF-MEMS switch has been finalized. A result is shown as an FIB-SEM image in Fig. 19 for both the overall device and the suspended membrane sections, as well.

VI. CHARACTERIZATION AND COMPARISON

The developed fabrication and encapsulation techniques have been applied to an RF-MEMS switch. For the electrical

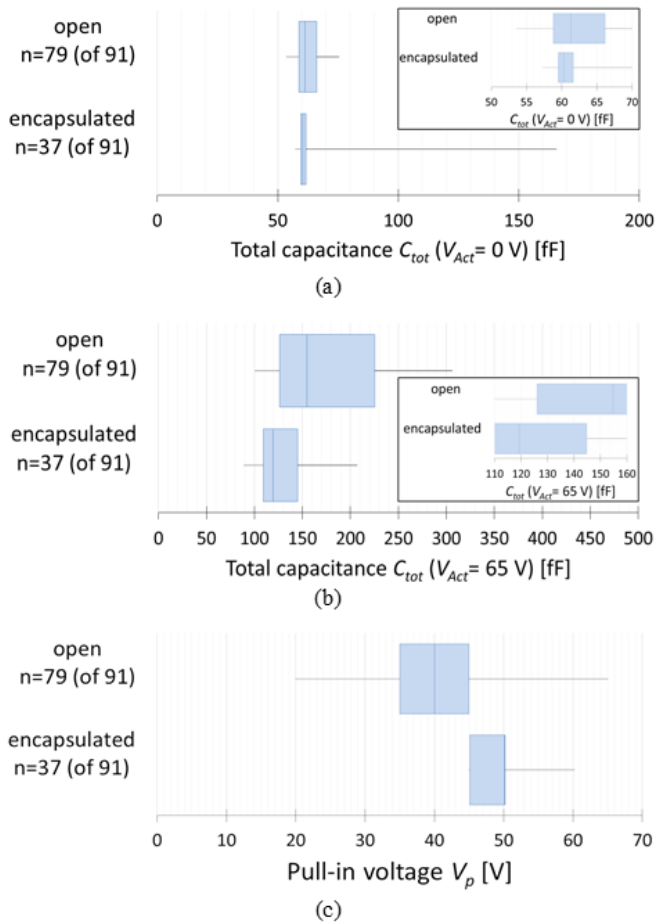

Fig. 20. Box plot analysis regarding the comparison of open and encapsulated RF-MEMS switches related to (a) OFF-state capacitance, (b) ON-state capacitance, and (c) pull-in voltage.

characterization, C–V and S-parameter measurements have been performed. The basic functionality and the encapsulation effects have been identified.

A. C–V-Measurement

C–V measurements were performed using a high-frequency impedance analyzer Agilent E4991A for voltage-depended capacitance measurements at a frequency of $f = 3$ GHz. In order to avoid parasitic effects of the measurement setup, an Open/Short/Load calibration has been performed using an impedance standard substrate (ISS). In detail, the step width V_w for the actuation voltage V_{act} was 5 V and the actuation voltage range has been chosen between the minimum voltage $V_{\text{act,min}} = -65$ V and the maximum voltage $V_{\text{act,max}} = +65$ V, depending on the expected value for pull-in voltage (V_p).

C–V measurements of RF-MEMS switches distributed on an entire wafer have been done and analyzed to see the effect of the process deviation over the 8-in wafer. To determine the impact of the encapsulation on the RF-MEMS switch performance, the mean value ($\bar{x}$), the standard deviation (±1 s) (Table V), and the box plot analysis (Fig. 20) have been used. It can be clearly seen in Table V that the mean value of the OFF-state capacitance C_{tot} (0 V) has a slight increase after the encapsulation process. The ON-state capacitance C_{tot}

TABLE V
SUMMARIZED STATISTICAL RESULTS FOR C–V MEASUREMENT RELATED PARAMETER OF OPEN SWITCHES COMPARED TO ENCAPSULATED SWITCHES

	Open		Encapsulated		Relative change [%]
	$\bar{x}_{open}$	±1s	$\bar{x}_{enc}$	±1s	$\left(\frac{\bar{x}_{enc}-\bar{x}_{open}}{\bar{x}_{open}}\right)$
C_{tot}(0V) [fF]	62.6	4.5	67.2	22.2	+7.4
C_{tot}(65V) [fF]	176.4	58.3	128.1	28.1	-27.4
V_p [V]	41.4	7.6	48.4	3.9	+16.9
Y [%]	86.8		40.7		-53.1

(65 V) change is more significant, the mean value drops from 176 to 128 fF. Furthermore, V_p increases from 41 to 48 V. The main reason for the change of the capacitance and mechanical behavior is the additional process steps of encapsulation. These steps change not only the switch cavity environment, but also changes the suspended membrane stress; thus the final shape. The final shape of the membrane has a strong effect on the contact, which defines C_{Cont}. Therefore, a significant decrease in the ON-state capacitance and also an increase in the pull-in voltage are related to the change in the membrane shape.

Fig. 20 summarizes all the measurement results for the parameters of C_{tot} (0 V), C_{tot} (65 V), and V_p, both for nonencapsulated and encapsulated cases.

The typical C–V behavior of a RF-MEMS switch, fabricated with and without encapsulation process is given in Fig. 21, for a single chip. It can be clearly seen that the pull-in voltage increases while the saturated ON-state capacitance decreases. The general trend of the C–V curve is similar to the nonencapsulated case. The increase of the pull-in voltage is due to the change in the stress of the suspended membrane during the encapsulation process, specifically the parasitic SiO_2 layer deposition. The suspended membrane slightly moves up, which increases the distance between the high-voltage electrodes and the membrane, thus increasing the pull-in voltage. Furthermore, the grain structure of the sputtered AlCu membrane gets annealed and induces a more defined switch behavior with reduced hysteresis effects for the encapsulated case.

In summary, the encapsulation process affects both the mechanical (V_p) and electrical [C_{tot} (0 V), C_{tot} (65 V)] parameters. It has also a negative effect on the yield (Table V). However, the main functionality and the typical C–V behavior of the RF-MEMS device can be still achieved after the encapsulation process. Subsequently, the RF-MEMS switch is characterized at D-band to see the influence of the encapsulation process on the RF performance.

B. S-Parameter Measurement

S-parameter measurements are performed on 8-in wafers. In general, on-wafer two-port S-parameter measurements are realized on a semiautomated wafer probe station. Two ZVA-Z170 (Rohde and Schwarz) mm-wave converters,

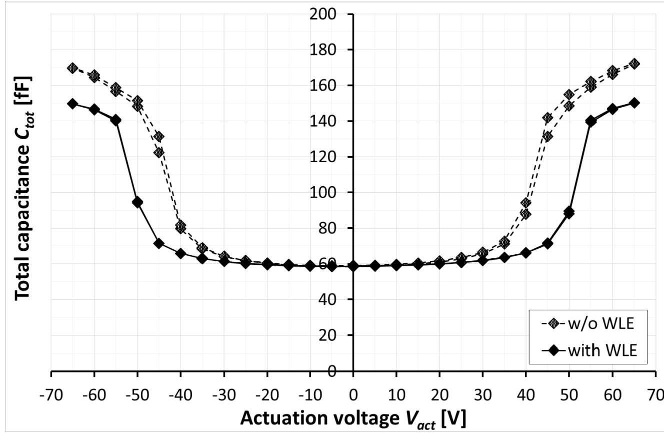

Fig. 21. C–V measurement of RF-MEMS switch in chip 04/05 of both wafer.

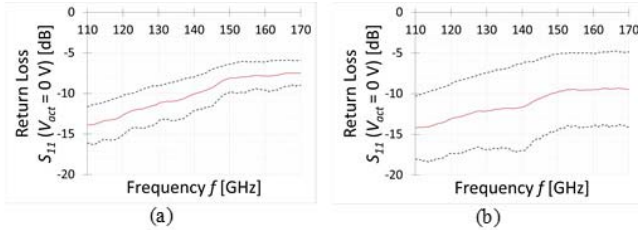

Fig. 22. Return loss of chosen RF-MEMS switch as mean curve (red) and as ±1 s curve (dashed line) for (a) open switch and (b) encapsulated switch.

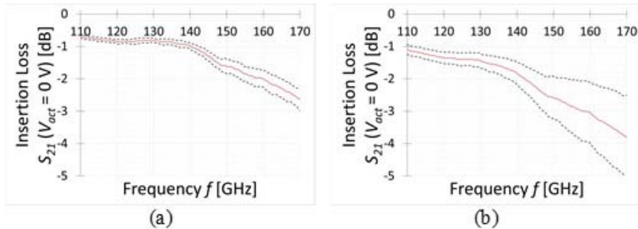

Fig. 23. IL of chosen RF-MEMS switch as mean curve (red line) and as ±1 s curve (dashed line) for (a) open switch and (b) encapsulated switch.

a four-port ZVA24 as vector network analyzer (VNA), and a system controller enable the S-parameter measurement between $f = 110$ and 170 GHz. Furthermore, two Infinity[1] 75 μm pitch ground-signal-ground (GSG) waveguide probes are implemented using a WR6 waveguide S-bend to connect them with the frequency converter. Regarding the calibration, an ISS 138-356 is used together with an RF absorber on an extra ceramic chuck to realize a full two-port line-reflect-reflect-match (LRRM) calibration. The membrane of the RF-MEMS is actuated using a Source Measurement Module.

Fig. 22 shows the S_{11} performance in OFF-state ($V_{\mathrm{Act}} = 0$ V), for both with and without encapsulation layer. Although the mean value of the S_{11} for both cases is similar, the variation over the wafer increases after the encapsulation process. In terms of IL (S_{21} in OFF-state), the encapsulated switches provide slightly higher loss and a wider variation

[1]Trademarked.

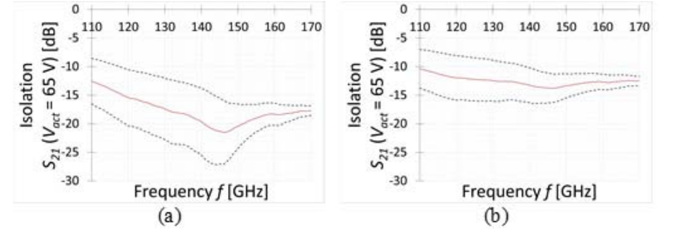

Fig. 24. Chosen RF-MEMS switch in ISO at $V_{\mathrm{act}} = 65$ V as mean curve (red) and as ±1 s curve (dashed line) for (a) open switch and (b) encapsulated switch.

TABLE VI
STATE-OF-THE-ART OF ENCAPSULATED CAPACITIVE SHUNT RF-MEMS SWITCHES

	[31]	[32]	This work
Technology	n. a.	CMOS	0.13 μm SiGe BiCMOS
Realization on/as	Sapphire substrate	Silicon substrate	BEOL integration
Encapsulation method	WLE by thin film	In-Line WLP	WLE by thin film
Frequency [GHz]	10	50	140
C_{tot} (V_{act}=0V) [fF]	-	40	58.6
V_p [V]	41	-	50
V_{act} [V]	-	60	65
C_{tot} (V_{act}) [fF]	-	140	150
S_{11}(V_{act}=0V) [dB]	-	-	-11.5
S_{21}(V_{act}=0V) [dB]	-0.1	-0.5	-1.8
S_{21} (V_{act}) [dB]	-10.7	-15	-13

over the wafer (Fig. 23). This can be explained by the affected OFF-state capacitance due to the encapsulation. Furthermore, the slightly degraded matching has caused an increase in the IL. Fig. 24 summarizes ISO performance (S_{21} in ON-state). Similar to the matching and IL characteristics, a reduced ISO is observed after the encapsulation process. Due to the decreased ON-state capacitance, the strong resonance at D-band is shifted to higher frequencies; hence, the maximum achievable ISO is 15 dB. However, the mean value of the ISO for the encapsulated devices over the 8-in wafer is better than 10 dB over the entire D-band.

At the center frequency of the D-band of 140 GHz, the achieved ISO of more than 10 dB and an IL of less than 2 dB show the very good potential of using the presented encapsulated RF-MEMS device as a switch component in the D-band. To put the obtained results in perspective, the state-of-the-art for encapsulated capacitive shunt RF-MEMS switches is shown in Table VI by considering wafer-level thin-film encapsulation (WLE) and wafer-level packaging (WLP). In sum, the achieved IL is increased with the complexity of RF-MEMS realization with similar values for ISO and for V_p.

VII. CONCLUSION

In this work, the development and encapsulation of a monolithically integrated D-band RF-MEMS switch in a

BiCMOS process environment are demonstrated. The challenges due to the BiCMOS process integration are identified and solutions for each challenge are extensively described. The main challenge of packaging the RF-MEMS devices is solved by a fully wafer-level high throughput encapsulation process. The details of the encapsulation process and the effects of the process on the RF-MEMS device are also studied. Finally, RF-MEMS switches distributed over an 8-in wafer are electrically characterized and the performance changes caused by the encapsulation process are provided. In conclusion, the monolithic integration and encapsulation process is successfully applied to a *D*-Band RF-MEMS switch. Further improvements can be achieved by optimizing the RF design to have a better matching, which would also decrease the IL. Furthermore, the reduced yield due to the encapsulation process can also be improved with further process optimizations.

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Alexander Göritz studied electrical engineering (microelectronics–semiconductor technology) at Technical University Dresden, Dresden, Germany, where he received the Dipl.-Ing. degree in 2011.

In 2012, he joined the Technology Department, IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany, and started to work on the development of RF-microelectro-mechanical-system (MEMS) for millimeter-wave (mm-wave) applications and their wafer-level thin-film encapsulation. In order to release the established MEMS devices, he applies and optimizes the MEMS releasing processes (wet chemical etching, HF vapor phase etching). Since 2014, his field of work is expanded by further tasks related to the development and application of general back-end-of-line (BEOL) process flows to realize BEOL wafers for passive devices in cost-efficient test platforms.

Selin Tolunay Wipf received the B.S. degree from Sabanci University, İstanbul, Turkey, in 2010, the M.S. degree from Boğaziçi University, İstanbul, in 2012, and the Ph.D. degree in millimeter-wave (mm-wave) RF-microelectro-mechanical-system (MEMS) switches in SiGe BiCMOS technologies from Technische Universität Berlin, Berlin, Germany, in 2019, after joining the IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany, and working on RF-MEMS devices.

In IHP Microelectronics, she works on RF design, optimization, and characterization of passive devices.

Martin Drost received the Dipl.-Chem. degree in chemistry and the Ph.D. degree in electron beam-induced processing of nanostructures from the University of Erlangen-Nuremberg, Erlangen, Germany, in 2012 and 2017, respectively.

He joined the Technology Department, IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany, and started working on the development of plasma etch processes, with a focus on back-end-of-line (BEOL) etching of metals and ILDs, and deep Si etching.

Marco Lisker received the Diploma degree in physics and the Ph.D. degree from Otto von Guericke University Magdeburg, Magdeburg, Germany, in 1997 and 2001, respectively. For his Ph.D. thesis, he worked on UV detectors based on wide bandgap materials (e.g., GaN).

From 2000 to 2009, he was with the Department of Electrical Engineering, Otto von Guericke University Magdeburg, where he worked on metal–organic chemical vapor deposition (MOCVD) processes for ferroelectric materials and noble metal electrodes. Since 2009, he has been a Process Engineer and a member of the Research Staff with IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany. Since 2011, he has been the Project Leader for hetero integration projects–a collaboration with the Ferdinand-Braun-Institut, Berlin, Germany. Herein the monolithic integration of SiGe circuit building blocks with InP subcircuits is realized by benzocyclobutene (BCB)-based wafer bonding for millimeter-wave (mm-wave) applications. Since 2016, he has been the Project Leader of graphene integration into the BiCMOS technology in the clean room of the IHP. Since 2017, in parallel, he has been the Project Leader of the GaNonCMOS Project where dc–dc converters are developed with closely integrated GaN switches together with CMOS controller and driver circuits. Since 2021, he has been the Group Leader of the Process Group, IHP Technology. He has authored or coauthored more than 100 papers in journals and conferences.

Christian Wipf received the M.Sc. degree in electrical engineering from the Brandenburg University of Technology, Cottbus, Germany, in 2008, and the Dr.-Ing. degree from the Technical University of Berlin, Berlin, Germany, in 2019, with a focus on designing high voltage control circuits for microelectro-mechanical-system (MEMS) matrix applications.

He joined the IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany, in 2005, where he is currently working in the field of dc and RF characterization of electronic devices and circuits down to cryogenic temperatures with the Technology Department. Furthermore, he is developing radiation-hard devices and circuits.

Matthias Wietstruck received the Diploma degree in microsystems technology from the University of Applied Science HTW Berlin, Berlin, Germany, in 2009.

His current research interests include the development of wafer-level packaging components and technologies for 2.5-D/3-D heterogeneous integration with a focus on millimeter-wave (mm-wave) and subterahertz applications.

Mehmet Kaynak received the B.S. degree from the Department of Electronics and Communication Engineering, Istanbul Technical University (ITU), İstanbul, Turkey, in 2004, the M.S. degree from the Microelectronic Program, Sabanci University, İstanbul, in 2006, and the Ph.D. degree from the Technical University of Berlin, Berlin, Germany, in 2014.

He joined the Technology Group, IHP–Leibniz-Institut für innovative Mikroelektronik, Frankfurt, Germany, in 2008. From 2008 to 2015, he has led the microelectro-mechanical-system (MEMS) development, IHP. From 2015 to 2020, he served as the Department Head of Technology with IHP. Since 2020, he has been a Scientist with the IHP Microelectronics.