Demonstrating 170 °C Low-Temperature Cu–In–Sn Wafer-Level Solid Liquid Interdiffusion Bonding

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***Abstract*— The wafer-level solid liquid interdiffusion (SLID) bonds carried out for this work take advantage of the Cu–In–Sn ternary system to achieve low-temperature interconnections. The 100-mm Si wafers had μ-bumps from 250 μm down to 10 μm fabricated by consecutive electrochemical deposition of Cu, Sn, and In layers. The optimized wafer-level bonding processes were carried out by EV Group and Aalto University across a range of temperatures from 250 °C down to 170 °C. Even though some quality-related process challenges were observed, it could be verified that high strength bonds with low defect content can be achieved even at a low bonding temperature of 170 °C with an acceptable 1-h wafer-level bonding duration. The microstructural analysis revealed that the bonding temperature significantly impacts the obtained phase structure as well as the number of defects. A higher (250 °C) bonding temperature led to the formation of Cu_3Sn phase in addition to $Cu_6(Sn,In)_5$ and resulted in several voids at Cu_3Sn|Cu interface. On the other hand, with lower (200 °C and 170 °C) bonding temperatures, the interconnection microstructure was composed purely of void-free $Cu_6(Sn,In)_5$. The mechanical testing results revealed the clear impact of bonding quality on the interconnection strength.**

***Index Terms*— Cu–In–Sn metallurgy, low-temperature wafer-level bonding, solid liquid interdiffusion (SLID) bonding.**

I. Introduction

THE rapid growth of Internet of Things (IoT) and cyber physical systems (CPSs) and their role in the Trillion Sensor Vision bring about requirements for additional verticality in 3-D packaging, as well as increased diversity in cap wafer materials. This type of highly miniaturized packaging requires a comprehensive understanding of residual stresses incurred during processing. Solid liquid interdiffusion (SLID) bonding has been identified as a solution to realize these more complex 3-D packages while also allowing for hermetic sealing, required for micro-electromechanical systems (MEMSs) [1]–[6]. The main benefit of the SLID bonding over other wafer-level metal bonding methods is that the interconnection, based on the formation of intermetallic compounds (IMC), has a high re-melt temperature that ensures that bonds do not re-melt during subsequent high-temperature processes [7].

Successful SLID bonds utilizing the Cu–Sn system have been carried out at temperatures around 300 °C [2], [3], [8]–[12]. Additionally, several other binary material systems like Ag–In [13]–[15], Au–In [16]–[18], Cu–In [19], Ag–Sn [20], [21], Ni–Sn [22], [23], and Au–Sn [2], [24]–[30] have also demonstrated potential for SLID bonding. Most of these systems require bonding temperatures close to 300 °C, which already is clearly lower than the typical temperatures required in the most commonly utilized eutectic (like Al–Ge), anodic, and glass-frit bonding processes [1]. However, by being able to even further reduce the bonding temperatures, the residual stresses, caused by mismatch in the thermal expansion either locally between Cu and Si or globally between other cap materials (such as germanium, glass, or sapphire), can be minimized [7]. In addition, applications that utilize temperature-sensitive materials, for example, antireflective coatings (ARCs) used in optical MEMS devices, could benefit from the lower processing temperatures.

The objective is to study the possibilities of low-temperature wafer-level SLID bonding down to 170 °C utilizing ternary Cu–In–Sn metallurgy at bonding temperatures that are below currently demonstrated solutions [32]–[34]. Additionally, the effect of bonding temperature on the bond quality, microstructure defect formation, and mechanical reliability will be investigated.

II. Methods and Materials

A. Wafer Preparation

The bonding experiments were carried out using four double side polished (DSP) Si wafers with a ⟨100⟩ crystal orientation. The backsides of the wafers were patterned using a standard

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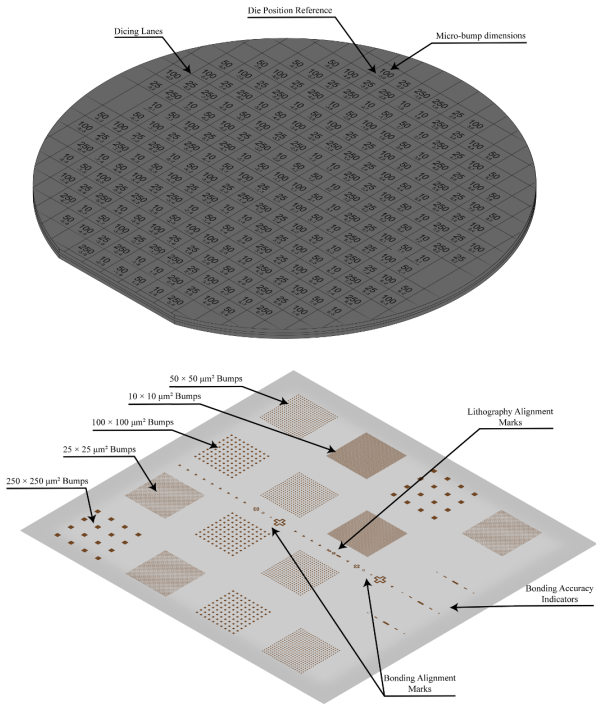

Fig. 1. Wafer layout, bonding features, and alignment marks.

TABLE I
BOND MATERIAL STACKS AND BONDING TEMPERATURES USED IN THE EXPERIMENTS

Bond	Bottom Wafer Layers	Top Wafer Layers	Bonding Conditions
#1EVG	Cu(4μm) / Sn(2μm)	Cu(4μm) / In(2μm)	250°C
#2 Aalto & EVG	Cu(4μm) / Sn(2μm) / In(2μm)	Cu(4μm) / Sn(2μm) / In(2μm)	200°C
#3 EVG	Cu(4 μm) / Sn(2μm) / In(2μm)	Cu(4μm) / Sn(2μm) / In(2μm)	170°C
#4 EVG	Cu(4μm) / In(2μm)	Cu(4μm) / Sn(2μm)	200°C

lithography process and the Si was etched using reactive ion etching (RIE). A 30-nm TiW barrier/adhesion layer followed by a Cu seed-layer of 150 nm was sputtered on the frontside of all wafers. The wafer pattern of the lithography mask, the bond features, and the alignment marks are shown in Fig. 1. A standard lithography process was utilized for the patterning of micro-bumps with dimensions ranging from 10 μm × 10 μm up to 250 μm × 250 μm. The photoresist was stripped and the field metallization layers were etched by means of wet chemistry.

The experiments were carried out using symmetrical and asymmetrical material stacks and different bonding equipment, as shown in Table I. The targeted thickness of 4-μm copper was electrochemically deposited, followed by a desired layer thickness 2-μm Sn and 2-μm In on both wafers. Copper was deposited using NB SEMIPLATE CU 100 using a copper sulfate-based chemistry with a targeted current density of 15 mA/cm^2 in a solution temperature regulated at 21 °C. Tin was deposited using NB SEMIPLATE SN 100 based on a tin methane sulfonic-based chemistry with a current density of 10 mA/cm^2. Indium was deposited in indium sulfamate plating bath from Indium Corporation, with indium pellets used as the anode and current density of 10 mA/cm^2. Copper and tin chemistries were sourced from NB Technologies and electroplating was carried out in open fountain-based electroplating systems. Indium sulfamate plating bath was kept at homogenous condition under constant stirring with a pH level of 1.6 at room temperature.

The electroplated features were measured after each step with a DektakXT contact profilometer and the target thicknesses for Cu, Sn, and In were achieved within ±0.3-μm accuracy over the wafers. For the asymmetrical stacks, either Sn or In was left out from the bond material stack.

B. Wafer Level Bonding and Non-Destructive Characterization at EV Group

The bonding experiments (all four wafer pairs shown in Table I) were carried out by the EV Group. The bonding process is shown in Fig. 2. The wafers were cleaned using organic solvents (prior to citric acid treatment) in order to remove possible organic residues. The wafers were aligned face-to-face on EVG SmartView NT2 semiautomated wafer-to-wafer aligner and subsequently bonded on an EVG520IS semiautomated wafer bonder. The same bonding force and time were used in both the EVG and Aalto processes. The bonded wafers were analyzed by scanning acoustic microscopy (SAM) using a PVA Tepla SAM 450.

C. Wafer-Level Bonding at Aalto

Two wafer pairs (see details from Table I, bond #2) were bonded at Aalto to limit the storage time (<24 h) between plating and bonding processes. This was designed to minimize the possible effects of surface oxidation of the bonding material. The bonding at 200 °C was carried out with a fixed duration of 1 h and utilizing a 4.3 kN bonding force, which leads to a bonding pressure of about 17 MPa as the total area of the microbumps were 2.52 mm^2. Wafers were placed into the AML-AWB-04 wafer bonder and rough aligned at ambient temperature and pressure. The bonding chamber was pumped down and then preheated to 75 °C before carrying out a fine alignment. Contact was made after alignment and then the bonding pressure was applied. A controlled heating cycle of 20 °C/min was initiated until the desired bonding temperature was reached. The wafers were held at the target bonding temperature and pressure for the duration of the hour-long bonding time. After the bonding time had expired, the heaters were switched off and the bonding pressure was released. The wafers were allowed to cool for approximately 1 h until they reached a temperature of 150 °C before the bonding chamber was vented and the bonded wafer pair was removed.

D. Microstructural and Mechanical Characterization

Dicing of all bonded wafer pairs was conducted using a Disco DAD3220 dicing saw. A selection of diced chips was

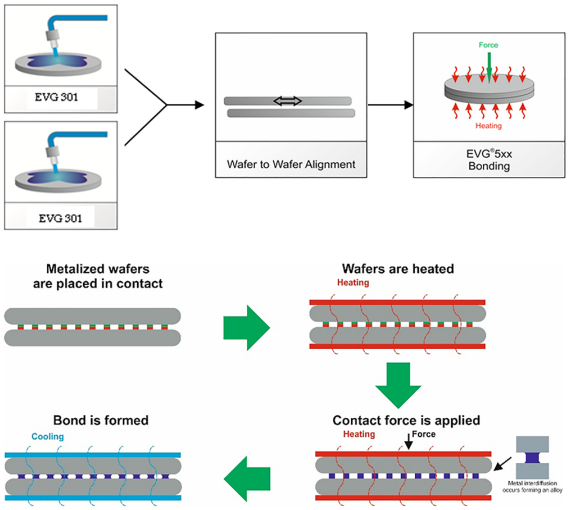

Fig. 2. EV Group bonding process.

molded and prepared for cross section analysis. The tensile strength of as-bonded chips was tested using the MTS 858 system. Chips were mounted on to brass studs using Loctite Power Epoxy. The measured tensile strain rate was 0.01 mm/s. Fracture surfaces and cross sections were then analyzed using optical microscopy as well as with JSM-6330F field emission scanning electron microscope (SEM), which is equipped with energy-dispersive X-ray spectroscopy (EDS). Ion beam polished cross sections were prepared and inspected using a dual-beam (FIB-SEM) JEOL JIB-4700F.

III. Results

Four wafer pairs were successfully bonded at EV Group and two wafer pairs at Aalto University. However, already after the resist stripping process, it was observed that a large fraction of the 10-μm features were absent, as the lithography process had been optimized for larger 250-μm feature sizes. The 10-μm features were present after development of the photoresist and electrochemical deposition of the material stack. However, during the resist stripping and field metallization etching processes, the smallest features were missing or damaged as seen in Fig. 3.

A. SAM Results

The four wafer pairs bonded at EVG were non-destructively studied with SAM. The principle of SAM is explained in Fig. 4, where three cases are illustrated. When a sound wave intersects a bond defect or an air gap, it generates reflecting echos that are stronger and of a different polarity. This causes these areas to appear lighter in the image. On the other hand, a no-defect bond appears darker. This can be seen in Fig. 5, where many of the chips have been successfully bonded, as they appear darker than their surroundings. In addition, it can also be concluded that the bonding accuracy is high with no excessive squeeze-out of the liquid phase. However, from the higher magnification micrograph shown in Fig. 6, it is evident that a notable fraction of the μ-bumps has not been formed properly, that is, the bumps with light contrast indicate an air gap between the interconnection materials when the transducer gate is focused to that specific height in the C-SAM inspection mode.

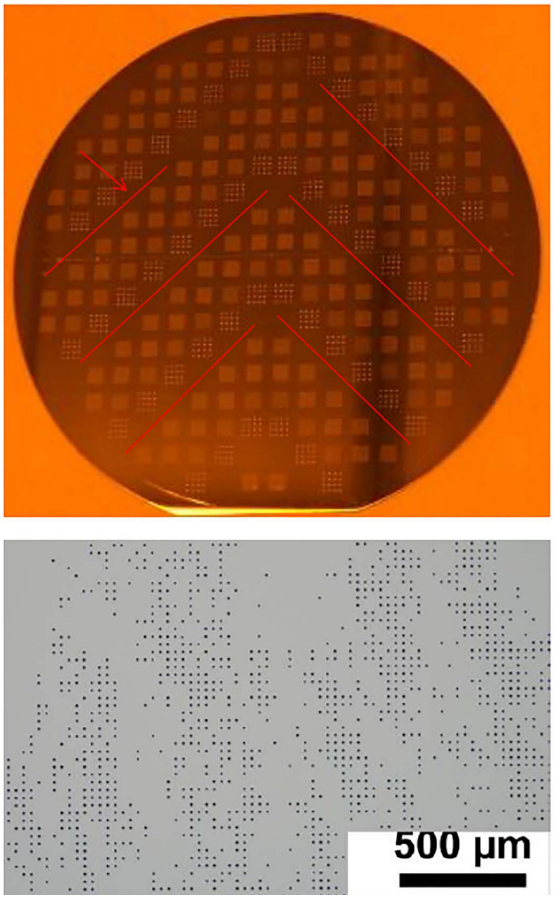

Fig. 3. Optical micrographs of the missing and damaged 10-μm features.

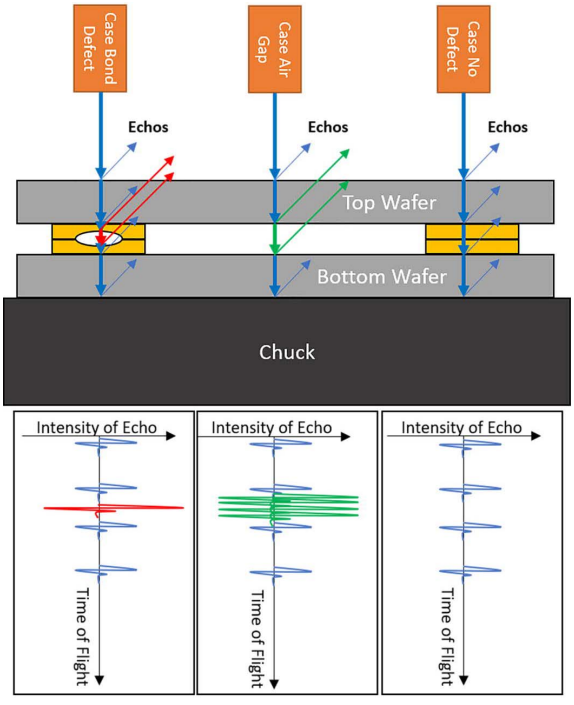

Fig. 4. Principle of SAM defect detection.

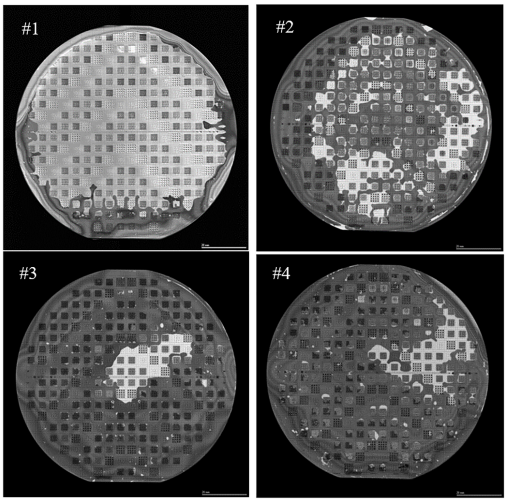

Fig. 5. C-SAM images from wafer-pairs #1–#4 SEM bonded at EVG. NB. The uneven dark gray background contrast is caused by the inflowing water.

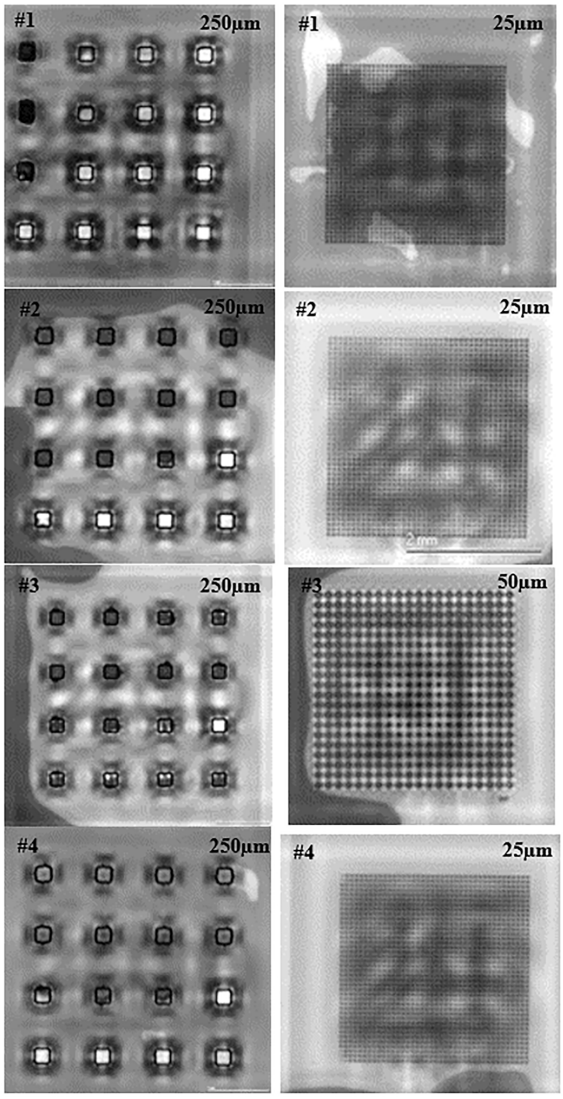

Fig. 6. Higher magnification C-SAM micrograph images from individual chips from wafer pairs #1–#4.

However, based on the SAM results, it is not possible to unambiguously define the bonding yield differences between the bonding temperatures and bond material stacks in wafer, chip, or μ-bump level.

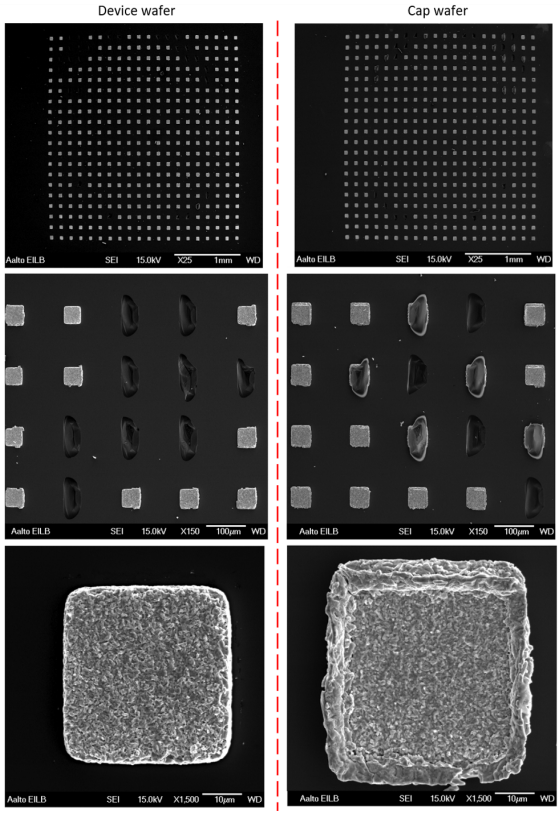

Fig. 7. SEM fracture surface analyses from the detached EVG #2 wafer. Micrographs at the left column are from the device wafer and corresponding cap wafer pictures are on the right. The red dashed line indicates the mirror plane.

B. Microstructural Analysis

After the non-destructive inspection, all bonded wafer pairs were diced. Two wafer pairs (EVG #2 and #4) detached during the dicing, but the other four wafer pairs survived and only the chips containing the 10-μm bumps failed during this process. To verify the root cause for the detachment, the fracture surfaces from EVG #2 wafer was investigated. As shown in Fig. 7, there are clearly two different failure mechanisms or fracture paths. From the chip containing 50-μm bumps, a large majority of the failures can be located at the original bonding interface. When these fracture surfaces were analyzed with the EDS method, it could be verified that both fracture surfaces contain only $Cu_6(Sn,In)_5$ phase. In addition, the surface morphology strongly indicates that the primary reason for the failure was not cohesive fracture through the IMC reaction layer but improper bond formation most likely due to surface oxidation or contamination. Cross-sectional samples from EVG #4 wafer revealed identical results. This conclusion is further supported by the SAM results above. On the other hand, in a few bumps, the bond has formed properly, and the fracture has occurred as cohesive silicon fracture.

The in-depth microstructural analysis focused on the successful wafer pairs that survived the dicing process. Fig. 8 demonstrates SEM cross-sectional micrographs from

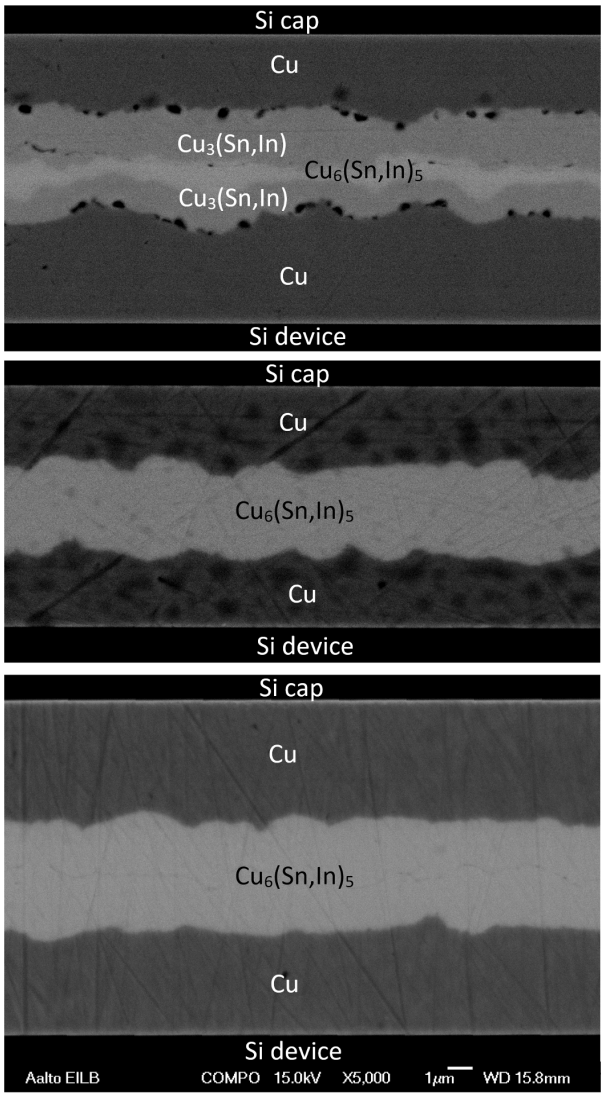

Fig. 8. SEM micrographs from μ-bonds bonded at (a) 250 °C (EVG #1), (b) 200 °C Aalto #2, and (c) 170 °C (EVG #3).

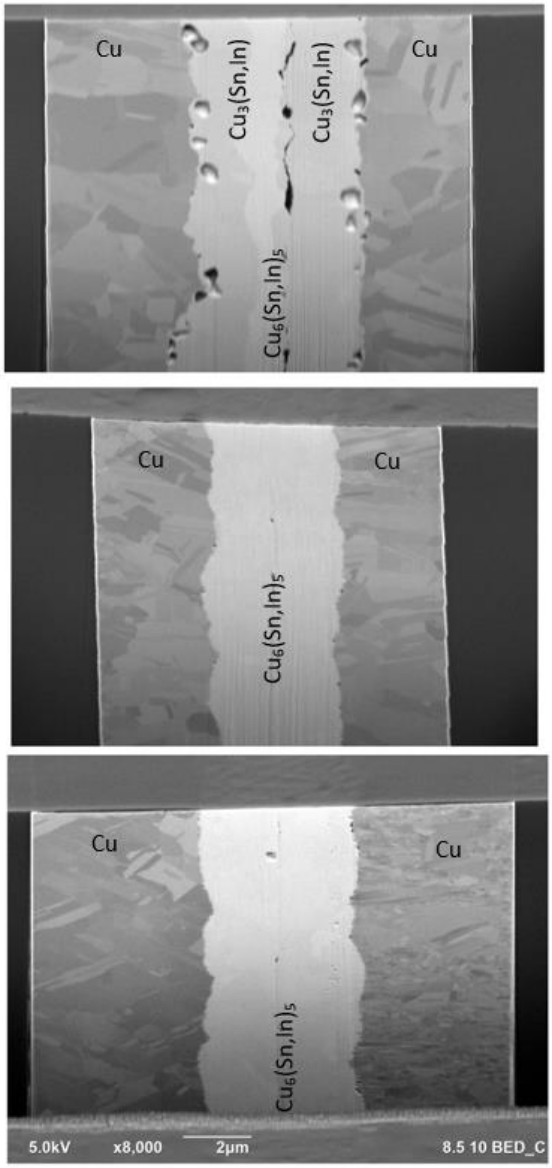

Fig. 9. Micrographs from FIB cuts made from the cross sections shown in Fig. 7 at (a) 250 °C (EVG #1), (b) 200 °C Aalto #2, and (c) 170 °C (EVG #3).

Cu–In–Sn SLID μ-bumps bonded at (a) 250 °C, (b) 200 °C, and (c) 170 °C. The 170 °C and 200 °C bond microstructures appear to be identical containing only a single phase. However, in the 250 °C bond, there are two clearly distinguishable phases present within the reaction zone. In addition, a significant number of voids can be detected at the interface next to copper. On the basis of the EDS analysis results, it can be concluded that the single phase observed in the 170 °C and 200 °C bonds is $Cu_6(Sn,In)_5$, where the Sn to In ratio is close to 1:1 (Cu56 Sn24 In20 at.%). The same phase with the same composition can also be detected at the center of the bond-line in the 250 °C interconnections. However, the majority of the bond microstructure is composed of $Cu_3(Sn,In)$ phase with an average composition of Cu75Sn14In11 at.%. Hence, the voids are located at the Cu|Cu_3Sn interface, which is in good agreement with previous studies of void formation in the binary Cu–Sn system [35]–[37].

To verify that the observed defects are 3-D, to avoid any artifacts caused by mechanical grinding and polishing, as well as to verify that additional defects or phases were not missed, FIB (focused ion beam) cross sections from these cross sections were prepared. The FIB micrographs are presented in Fig. 9. The original cross sections are now at the top of each micrograph. Since the FIB was also equipped with an EDS detector having higher peak resolution, the chemical compositions were again verified. The results confirm the findings; however, it can also be observed that there are clearly additional defects at the center of the bond-line in the 250 °C sample [see Fig. 9(a)]. In addition, the original bonding interface can be partly seen also from the 200 °C [see Fig. 9(b)] and 170 °C bonds [see Fig. 9(c)].

The formation of the interconnection microstructure during bonding can be rationalized by utilizing the vertical (see Fig. 10) and isothermal (see Fig. 11) sections from Cu–In–Sn ternary system [34], [38]. The black dotted line in Fig. 10

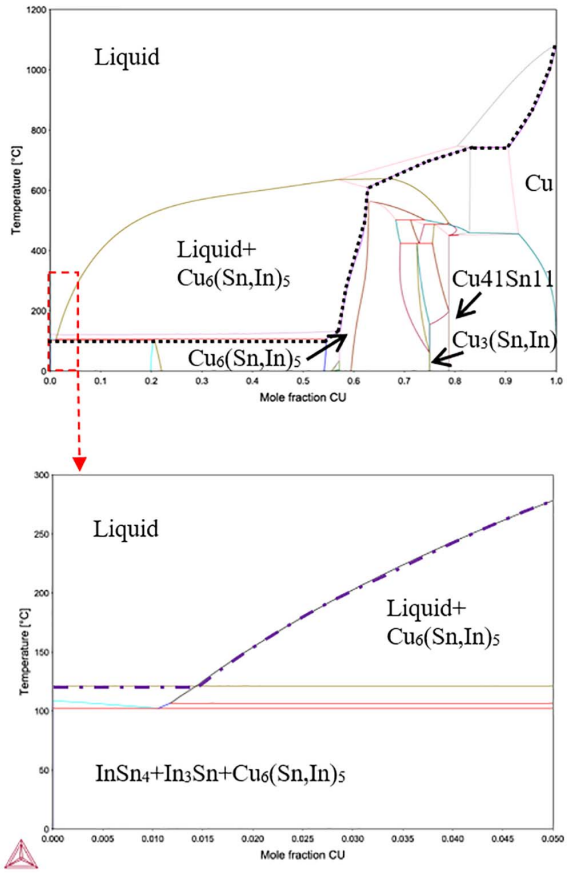

Fig. 10. Vertical section from Sn50In50 (at.%) to pure Cu.

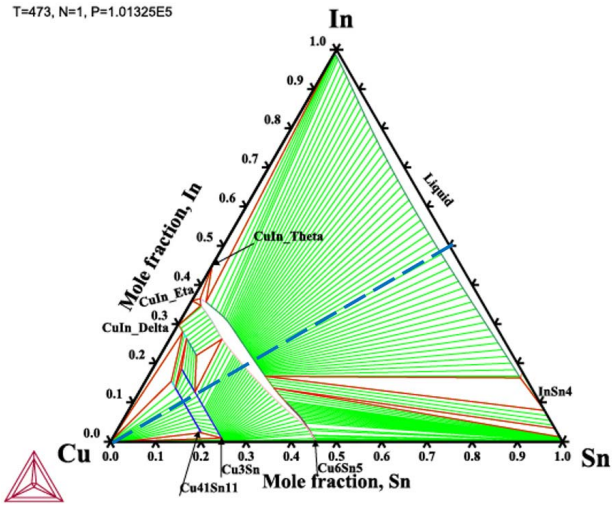

Fig. 11. Isothermal section from Cu–In–Sn system at 200 °C.

Fig. 12. Tensile testing data from three wafer pairs EVG1, EVG3, and Aalto bond bonded at 250 °C, 170 °C, and 200 °C, respectively. The red arrows indicate the samples from which the fractographs are shown in Fig. 13.

indicates the solidus curve, that is, below that curve the liquid phase does not exist. Hence, it is evident that when the liquid phase has been completely consumed by the IMC reactions, the local nominal composition of the reaction zone is >60 at.% Cu and, therefore, the remelting temperature of the interconnection has increased to ~600 °C. Moreover, when compared to the Cu–Sn system, the addition of In has the effect of stabilizing the liquid phase. This has two major impacts: 1) reducing the temperature of the liquidus line (purple dot-dashed line in Fig. 10 inlay) and 2) increases the solubility of Cu into the liquid phase. The increased Cu solubility results in a higher dissolution rate of Cu into the liquid. Overall, this increases the processing temperature window by allowing for lower bonding temperatures to be used without suffering from a marked reduction in the reaction rate and subsequently increased bonding times.

The reaction sequence during the bonding can be rationalized by utilizing the isothermal section from the system at the bonding temperature. As can be seen from Fig. 11 when Cu starts to dissolve into liquid phase having 1:1 Sn to In ratio (the local nominal composition starts to follow the blue dashed contact line), the liquid phase becomes supersaturated with Cu and in local equilibrium with $Cu_6(Sn,In)_5$. According to the isothermal section, $Cu_6(Sn,In)_5$ cannot be in local equilibrium directly with Cu and therefore either $Cu_3(Sn,In)$ (or CuIn_Delta) and Cu41Sn11 phases should nucleate between $Cu_6(Sn,In)_5$ and Cu. However, as has been previously reported, the solubility and stabilizing effect of In to $Cu_6(Sn,In)_5$ is significantly higher than that to $Cu_3(Sn,In)$ and Cu41Sn11 [34]. Therefore, even though this interface is not thermodynamically stable, the driving force for nucleation and growth of these additional phases is extremely low.

C. Mechanical Testing Results

The mechanical testing results are shown in Fig. 12. During the tensile testing, several samples failed during handling, and these are marked as data points below 10 MPa threshold fracture strength. As can be seen from Fig. 12, extremely large scatter in the results was observed. The highest tensile strengths were 40–50 MPa. Somewhat surprisingly, the high values exceeding 25 MPa were more common in the 200 °C and 170 °C low-temperature bonds rather than the 250 °C bonds. In order to rationalize the obtained values, fracture surfaces of the tested samples were analyzed with optical microscopy and SEM. These investigations (see Fig. 13) revealed that the majority of all fractures were failures through incompletely formed bonds (similar fracture surfaces as were observed from the detached EVG #2 wafer). Bulk silicon cohesive fractures and small number of adhesion failures

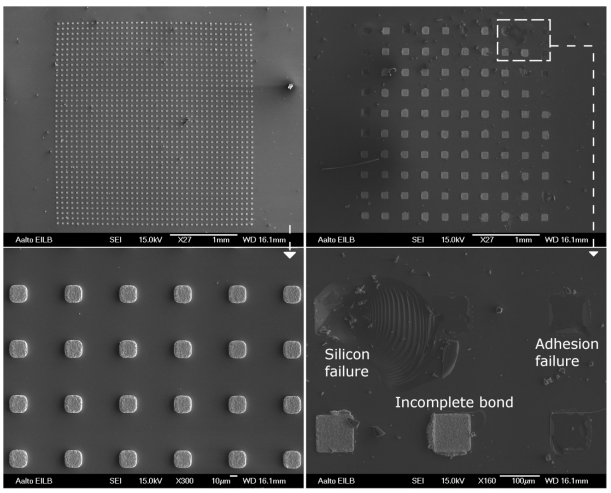

Fig. 13. Fracture surfaces after tensile testing. (Left) EVG 1 ($T_{\text{bonding}} = 250$ °C) chip with 25-μm bumps where the fracture strength was <10 MPa and practically all bonds were unsuccessfully formed. (Right) EVG 3 ($T_{\text{bonding}} = 170$ °C) chip with 100-μm bumps where the fracture strength was >40 MPa and the relative amount of cohesive bulk Si fractures was high. The corresponding datapoints are highlighted in Fig. 12.

propagating Si|TiW or TiW|Cu interfaces were also observed. As seen from Figs. 12 and 13, there is a clear correlation between the fracture strength and distribution of the failure locations: the higher the observed fracture strengths, the more cohesive silicon failures were observed. This strongly indicates that when the low-temperature Cu–In–Sn bonds are properly formed their strength sufficient, and the bonds themselves will not be the limiting factor for mechanical reliability performance.

IV. Conclusion

Low-temperature wafer-level SLID bonds were successfully fabricated down to 170 °C. The bonds manufactured at 170 °C and 200 °C showed minimal voiding and defects. The addition of indium to a traditional Cu–Sn system appears to significantly stabilize the $Cu_6(Sn,In)_5$ phase. However, the 250 °C bonded samples had significantly higher number of voids and were composed of two phases $Cu_3(Sn,In)$ and $Cu_6(Sn,In)_5$. Tensile tests demonstrated that the successfully formed high-quality Cu–In–Sn bonds outperformed the under-bump metallization strength. Further experiments will be carried out to characterize the mechanical properties of the indium containing intermetallic phases. Additionally, process-related optimizations such as lithography optimization for smaller micro-bumps and optimizing a stable process to bond asymmetrical materials stacks are required. The full use of EVG's advanced wafer bonding and destruction-free analysis capabilities will be utilized further for enhanced test wafer processing conditions.

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References

[1] M. Tilli, M. Paulasto-Krockel, M. Petzold, H. Theuss T. Motooka, and V. Lindroos, *Handbook of Silicon Based MEMS Materials and Technologies*, 3rd ed. Amsterdam, The Netherlands: Elsevier, 2020.

[2] H. Xu *et al.*, "Wafer-level SLID bonding for MEMS encapsulation," *Adv. Manuf.*, vol. 1, no. 3, pp. 226–235, Sep. 2013.

[3] A. Hilton and D. Temple, "Wafer-level vacuum packaging of smart sensors," *Sensors*, vol. 16, no. 11, p. 1819, Oct. 2016.

[4] V. Vuorinen, "Wafer-level metal bonding for MEMS/MOEMS devices," in *Proc. IEEE 26th Int. Symp. Design Technol. Electron. Packag. (SIITME)*, Oct. 2020.

[5] V. Vuorinen, G. Ross, H. Viljanen, J. Decker, and M. Paulasto-Krockel, "Process integration and reliability of wafer level SLID bonding for poly-Si TSV capped MEMS," in *Proc. 7th Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Dresden, Germany, Sep. 2018, pp. 18–21.

[6] V. Drăgoi, E. Cakmak, and E. Pabo, "Metal wafer bonding for MEMS devices," *Romanian J. Inf. Sci. Technol.*, vol. 13, no. 1, pp. 65–72, Jan. 2010.

[7] A. Lis, S. Kicin, F. Brem, and C. Leinenbach, "Thermal stress assessment for transient liquid-phase bonded Si chips in high-power modules using experimental and numerical methods," *J. Electron. Mater.*, vol. 46, no. 2, pp. 729–741, Feb. 2017.

[8] A. Duan, K. Wang, K. E. Aasmundtveit, and N. Hoivik, "Reducing the bond frame width in Cu/Sn SLID wafer level packaging," in *Proc. 4th Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Sep. 2012, pp. 1–5.

[9] P. Ramm, J. J.-Q. Lu, and M. M. V. Taklo, *Handbook of Wafer Bonding*. Hoboken, NJ, USA: Wiley, 2012.

[10] M. Brincker, S. Söhl, R. Eisele, and V. N. Popok, "Strength and reliability of low temperature transient liquid phase bonded Cu Sn Cu interconnects," *Microelectron. Rel.*, vols. 76–77, pp. 378–382, Sep. 2017.

[11] C.-T. Ko and K.-N. Chen, "Wafer-level bonding/stacking technology for 3D integration," *Microelectron. Rel.*, vol. 50, no. 4, pp. 481–488, Apr. 2010.

[12] H. Liu, G. Salomonsen, K. Wang, K. E. Aasmundtveit, and N. Hoivik, "Wafer-level Cu/Sn to Cu/Sn SLID-bonded interconnects with increased strength," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 9, pp. 1350–1358, Sep. 2011.

[13] T.-T. Luu, A. Duan, K. E. Aasmundtveit, and N. Hoivik, "Optimized Cu-Sn wafer-level bonding using intermetallic phase characterization," *J. Electron. Mater.*, vol. 42, no. 12, pp. 3582–3592, Dec. 2013.

[14] W. P. Lin, C. Sha, and C. C. Lee, "40 μm flip-chip process using Ag–In transient liquid phase reaction," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 6, pp. 903–908, Jun. 2012.

[15] C. Lee *et al.*, "Characterization of intermediate In/Ag layers of low temperature fluxless solder based wafer bonding for MEMS packaging," *Sens. Actuators A, Phys.*, vol. 154, no. 1, pp. 85–91, Aug. 2009.

[16] J.-C. Lin, L.-W. Huang, G.-Y. Jang, and S.-L. Lee, "Solid-liquid interdiffusion bonding between in-coated silver thick films," *Thin Solid Films*, vol. 410, nos. 1–2, pp. 212–221, May 2002.

[17] B. J. Grummel, Z. J. Shen, H. A. Mustain, and A. R. Hefner, "Thermo-mechanical characterization of Au-In transient liquid phase bonding die-attach," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 5, pp. 716–723, May 2013.

[18] V. Chidambaram, C. Bangtao, G. C. Lip, and D. R. M. Woo, "Au-In-based hermetic sealing for MEMS packaging for down-hole application," *J. Electron. Mater.*, vol. 43, no. 7, pp. 2498–2509, Jul. 2014.

[19] L. Deillon, A. Hessler-Wyser, T. Hessler, and M. Rappaz, "Solid-liquid interdiffusion (SLID) bonding in the Au-In system: Experimental study and 1D modelling," *J. Micromech. Microeng.*, vol. 25, no. 12, Dec. 2015, Art. no. 125016.

[20] Y.-C. Chen and C. C. Lee, "Indium-copper multilayer composites for fluxless oxidation-free bonding," *Thin Solid Films*, vol. 283, nos. 1–2, pp. 243–246, Sep. 1996.

[21] Q. Guo, F. Yu, H. Chen, and M. Li, "Microstructure evolution during reflow and thermal aging in a Ag@Sn TLP bondline for high-temperature power devices," *J. Mater. Sci., Mater. Electron.*, vol. 29, no. 4, pp. 3014–3024, Feb. 2018.

[22] J. F. Li, P. A. Agyakwa, and C. M. Johnson, "Kinetics of Ag3Sn growth in Ag–Sn–Ag system during transient liquid phase soldering process," *Acta Mater.*, vol. 58, no. 9, pp. 3429–3443, May 2010.

[23] S. W. Yoon, M. D. Glover, and K. Shiozaki, "Nickel-tin transient liquid phase bonding toward high-temperature operational power electronics in electrified vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2448–2456, May 2013.

[24] H. P. R. Frederikse, R. J. Fields, and A. Feldman, "Thermal and electrical properties of copper-tin and nickel-tin intermetallics," *J. Appl. Phys.*, vol. 72, no. 7, pp. 2879–2882, Oct. 1992, doi: 10.1063/1.351487.
[25] T. Suni *et al.*, "Wafer-level AuSn and CuSn bonding for MEMS encapsulation," in *Proc. Eur. Microelectron. Packag. Conf.*, 2013, pp. 1–5.
[26] T. A. Tollefsen, A. Larsson, O. M. Lövvik, and K. Aasmundtveit, "Au-Sn SLID bonding—Properties and possibilities," *Metall. Mater. Trans. B*, vol. 43, no. 2, pp. 397–405, 2012.
[27] H. Xu *et al.*, "Reliability performance of Au-Sn and Cu-Sn wafer level SLID bonds for MEMS," in *Proc. 5th Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Sep. 2014, pp. 1–5.
[28] K. E. Aasmundtveit, T. T. Luu, H. V. Nguyen, R. Johannessen, N. Hoivik, and K. Wang, "Au-Sn fluxless SLID bonding: Effect of bonding temperature for stability at high temperature, above 400°C," in *Proc. Electron. Syst. Integr. Technol. Conf. (ESTC)*, 2010, p. 5.
[29] S. Marauska, M. Claus, T. Lisec, and B. Wagner, "Low temperature transient liquid phase bonding of Au/Sn and Cu/Sn electroplated material systems for MEMS wafer-level packaging," *Microsyst. Technol.*, vol. 19, no. 8, pp. 1119–1130, 2013.
[30] T. A. Tollefsen, O. M. Løvvik, K. Aasmundtveit, and A. Larsson, "Effect of temperature on the die shear strength of a Au-Sn SLID bond," *Metall. Mater. Trans. A*, vol. 44, no. 7, pp. 2914–2916, Jul. 2013.
[31] T. A. Tollefsen *et al.*, "Au-Sn SLID bonding: A reliable HT interconnect and die attach technology," *Metall. Mater. Trans. B*, vol. 44, no. 2, pp. 406–413, Apr. 2013.
[32] J. Hotchkiss *et al.*, "Study of Cu-Sn-In system for low temperature, wafer level solid liquid inter-diffusion bonding," in *Proc. IEEE 8th Electron. Syst.-Integr. Technol. Conf. (ESTC)*, Vestfold, Norway, Sep. 2020, pp. 1–5, doi: 10.1109/ESTC48849.2020.9229696.
[33] G. Ross, J. N. Tiwary, D. Hongqun, V. Vuorinen, and M. Paulasto-Kröckel, "Low temperature wafer-level Cu-In-Sn solid liquid interdiffusion bonding," in *Proc. Pacific Rim Meeting Electrochem. Solid-State Sci. (PRiME)*, Oct. 2020.
[34] V. Vuorinen, H. Dong, G. Ross, J. Hotchkiss, J. Kaaos, and M. Paulasto-Kröckel, "Wafer level solid liquid interdiffusion bonding—Formation and evolution of microstructures," *J. Electron. Mater.*, vol. 50, pp. 818–824, Oct. 2020.
[35] H. K. Kannojia and P. Dixit, "A review of intermetallic compound growth and void formation in electrodeposited Cu-Sn layers for microsystems packaging," *J. Mater. Sci., Mater. Electron.*, vol. 32, no. 6, pp. 6742–6777, Mar. 2021, doi: 10.1007/s10854-021-05412-9.
[36] G. Ross *et al.*, "Interfacial void segregation of Cl in Cu-Sn microconnects," *Electron. Mater. Lett.*, vol. 13, no. 4, pp. 307–312, Jul. 2017.
[37] G. Ross, P. Malmberg, V. Vuorinen, and M. Paulasto-Kröckel, "The role of ultrafine crystalline behavior and trace impurities in copper on intermetallic void formation," *ACS Appl. Electron. Mater.*, vol. 1, no. 1, pp. 88–95, Jan. 2019.
[38] X. J. Liu *et al.*, "Experimental determination and thermodynamic calculation of the phase equilibria in the Cu-In-Sn system," *J. Electron. Mater.*, vol. 30, no. 9, pp. 1093–1103, Sep. 2001.

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