Modeling and Analysis of Silver-Sintered Molybdenum Packaging for SiC Power Modules With Improved Lifetime and Temperature Range

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***Abstract*— With the application of wide-bandgap devices, the packaging technology of power modules is faced with elevated challenges. This article proposes a new packaging concept for silicon carbide (SiC) power modules. The main objective is to improve the lifetime and temperature range, while the proposed packaging also has the potential to reduce stray inductance and simplify the fabrication process. In the proposed concept, sintered nano-silver is selected as the die bonding. The conventional direct-bonded copper substrate is replaced by a molybdenum layer and a bismaleimide triazine resin layer which has a low thermal expansion coefficient. A steady-state thermal–mechanical analysis is conducted to verify the material selection. Furthermore, a transient thermal–mechanical analysis based on Joint Electron Device Engineering Council (JEDEC) temperature cycling methods is carried out, whose results are applied in the Coffin–Manson lifetime model to evaluate the advantages of the proposed silver-sintered molybdenum packaging. The results demonstrated that the proposed packaging technology could improve the lifetime by over 1000 times and increase the maximum operating temperature by nearly three times. Finally, a feasible process of sintering SiC chips on molybdenum substrates is proposed, which achieves a uniform and low porosity bonding.**

***Index Terms*— Device lifetime, power electronics, semiconductor device packaging, silicon carbide, wide-bandgap devices.**

I. Introduction

SEMICONDUCTOR power modules are key components in power electronics systems. They determine the cost and performance of the system to a large extent. Due to the mass implementation of power electronics in a wide range of applications, such as electrified vehicles and renewable energies, the power module industry is rapidly expanding. Yole development forecasts that power modules will have a total market of U.S. $7.6 billion by 2025, with a five-year compound annual growth rate of 9.1%. The largest part of the growth will be contributed by the electric vehicle industry [1]. The growing market and the need to save energy pose elevated challenges to the reliability, efficiency, power density, and cost of power modules. The U.S. Department of Energy has set targets for high-voltage power electronics, requiring reducing the cost to U.S. $2.7 per kW, doubling the lifetime, and increasing the power density to 100 kW/L by 2025 [2]. The improvement in power modules is important to achieving these goals. Power modules are critical components in terms of cost and reliability, and their efficiency determines the size of the cooling system, which heavily affects the power density of a converter. However, the performance of power modules does not just rely on the semiconductor dies, but is also affected by the packaging of the device.

The conventional packaging technology is based on the direct-bonded-copper (DBC) substrate and bond wires. This technology has been applied in most of the existing modules and is still the most prevalent option in the market. However, the traditional packaging is facing challenges with growing performance requirements [3]. The large variations in the coefficient of thermal expansion (CTE) between the semiconductor, copper, and ceramic material causes significant thermal stress at high temperature, limiting the maximum operating temperature and lifetime of the module. Meanwhile, bond wires introduce larger stray inductance to the circuit. The stray inductance leads to a voltage spike, which will limit the operating voltage of the module. Moreover, the DBC substrates are relatively expensive to be manufactured [4].

Over the years, wide bandgap (WBG) devices have been regarded as the future of power electronics. The silicon carbide (SiC) MOSFETs, specifically, are suitable for the next-generation traction applications due to their superior dielectric breakdown field intensity and temperature range. The application of SiC MOSFETs brings challenges to the packaging design. Compared with conventional silicon (Si)-based insulated -gate bipolar transistor (IGBTs) and diodes, SiC MOSFETs of the same rating can be 3× smaller in size [5], [6], which increases concerns of

Manuscript received October 6, 2021; accepted October 30, 2021. Date of publication November 8, 2021; date of current version December 16, 2021. This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC). Recommended for publication by Associate Editor K. Bock upon evaluation of reviewers' comments. *(Corresponding author: Yuhang Yang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCPMT.2021.3126284.

Digital Object Identifier 10.1109/TCPMT.2021.3126284

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temperature and stress concentration. Meanwhile, SiC MOSFETs can handle high temperatures over 200 °C [7], while conventional packaging can barely match this range due to thermal stress concerns caused by the DBC substrate. Novel packaging technologies are needed to achieve a higher temperature range of SiC devices and improve the thermal–mechanical reliability. In addition, SiC devices are more sensitive to stray inductance due to their faster switching speed. Thus, bond wires should be replaced by low-inductance interconnections, such as planar leads.

Innovations have been proposed in the literature to address those challenges. For example, several studies verified that the printed-circuit-board (PCB) embedded packaging technology could shorten the circuit loop and minimize the stray inductance [8]–[10]. Flip-chip and press-pack designs could simplify the electrical contact and increase power density [11]–[14]. To improve the lifetime, novel thermal management solutions, such as double-sided cooling and integrated cooling [13], [15], [16], were implemented. On the other hand, efforts have been spent on investigating new materials with suitable CTE and higher strength, especially for critical components such as the die bonding [8], [13], [17], [18].

A silver-sintered molybdenum packaging concept is proposed in this article for SiC power modules. The primary target is to improve the lifetime and the temperature range of the module. Thus, CTE-matched materials, such as molybdenum (Mo) and bismaleimide triazine (BT) resin, are selected. The SiC MOSFET die is attached to the Mo substrate using nano-silver sintering technology, which is proved to have improved strength compared with regular soldering technologies [19]. Besides, the interconnections are achieved by low-inductance planar leads. Another potential benefit of this concept is that the manufacturing process would be simpler and cheaper due to the reduction of layers and the elimination of the DBC substrate. In Section II, the proposed packaging concept is introduced in detail. Single-die modules based on the proposed packaging and the conventional DBC packaging are designed. Then, in Section III, steady-state finite-element analysis (FEA) is conducted to compare the thermal–mechanical performance of different modules and finalize the material selection. Section IV studies the lifetime and temperature range advantages of the proposed module using Joint Electron Device Engineering Council (JEDEC) standard temperature-cycling methods and the renowned Coffin–Manson lifetime model. In Section V, the manufacturability of proposed packaging technology is discussed. And a feasible solution for the key step, the nano-silver sintering on molybdenum, is proposed and evaluated. Finally, the summary and future plan are presented in Section VI.

II. Concept Proposal

The proposed packaging concept uses CTE-matched materials and simplified layer configuration to achieve a better lifetime and an easier manufacturing process.

A. Layer Stack-Up

The layer stack-up of the proposed packaging design is illustrated in Fig. 1. Instead of using a DBC substrate, this module has a metallic substrate whose CTE is closer to that of SiC. The material selection of this substrate will be discussed in Sections II-B and III. The same metallic material is used for all the metal layers, including the heatsink and the lead interconnections. The SiC die is directly bonded to the substrate using nano-silver sintering bonding. The same bonding approach is adopted for the leads on top. The insulation between the heatsink and the substrate is achieved by a resin bonding layer which also has a similar CTE to other materials. In general, the major constituents in the module have a small variation in CTE. The module is then encapsulated in silicone gel for protection against the environment. Silicone gel is a very soft material whose modulus is 10^5–10^6 times smaller than other materials. Therefore, the effect of silicone gel on the mechanical behavior of other materials is ignored in the following analysis.

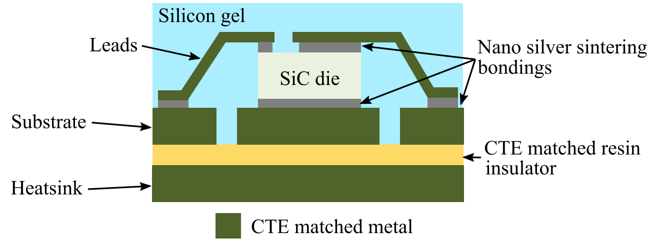


Fig. 1. Layer stack-up of the proposed module.

TABLE I
METALLIC MATERIALS FOR POWER ELECTRONICS PACKAGING AND THERMAL MANAGEMENT [20]–[23]

Material	Density (g/cm^3)	γ (%IACS)	k (W/m-K)	CTE (1×10^{-6}/K)
SiC	3.1	-	120	4.0
Pure Mo	10.2	0.32	140	5.3
Mo-Cu Alloy (15% -60% Cu)	9.4 - 10	0.37 - 0.65	170 - 290	6.8 - 11.5
Pure W	19.27	0.31	170	4.6
W-Cu Alloy (10% - 50% Cu)	11.7 - 16.75	0.27 - 0.56	$>$ 170	7.4 - 13
Kovar Alloy	8.3	-	17	5.9

B. Material Selection

Material selection is critical for the proposed module to achieve desired thermal–mechanical benefits. The CTE-matched metal has the greatest impact on the module's structural performance since it is used in all the metal layers (the substrate, the heatsink, and leads) and takes the majority of the volume. Specifically, they are directly contacted with the weakest point, the bonding layers. Thus, the selection of this material should be investigated in detail.

Table I [20]–[23] show several metallic materials which are seen as suitable candidates for power electronics thermal management and packaging. They typically have much smaller

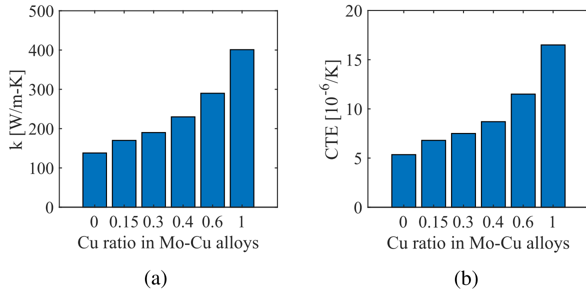


Fig. 2. Key properties of Mo–Cu Alloys with different Cu ratios. (a) k. (b) CTE.

CTE than copper and aluminum. Besides, γ denotes the electrical conductivity, and k represents the thermal conductivity.

Among those materials, pure Mo and Mo–Cu alloys have low CTE, good thermal conductivity, and relatively low mass density. Thus, they are selected as candidates for the metal layers. The selection will be finalized in the following simulations. On the contrary, other materials have unbalanced properties. Kovar alloy has low CTE and mass density, but its thermal conductivity is too low compared with other materials. Tungsten (W) and W–Cu alloys have slightly higher thermal conductivity than pure Mo and Mo–Cu alloys, however, they have higher CTE and doubled mass density. In addition, W series elements are extremely hard to be manufactured.

The thermal–mechanical properties of pure Mo and Mo–Cu alloys are shown in Fig. 2 [22], [23]. Alloys with a higher Cu ratio have a higher thermal conductivity which tends to reduce the thermal resistance and junction temperature. However, it will also lead to a larger CTE, which might induce greater thermal stress. An in-depth analysis is required to determine what ratio of Cu benefits the thermal–mechanical performance of the power module the most.

The metallic substrates are bonded to the heatsink using a CTE-matched resin which also provides the electrical insulation. The BT resin prepreg (HL832NSF) [24] from Mitsubishi Gas Chemical is selected. This material has a very close CTE (5×10^{-6}/°C) in the x- and y-directions compared to that of SiC and the candidate metallic materials, which help further reduce the thermal stress in the entire module. More importantly, it is one of few materials suitable for high-temperature applications. Its glass transition temperature is around 270 °C, which is 1.5–2 × higher than common epoxy or polyimide materials applied in PCBs and power modules. Hou *et al.* [8], [18] used this material in a PCB embedded SiC power module and verified its advantages in thermal–mechanical performance.

In the proposed module, the SiC die is sintered to the substrate with nano-silver paste. This bonding method has been widely investigated in the literature, and it is suitable for high-temperature applications due to its high melting temperature of 961 °C. It also has 3× higher thermal conductivity and 5× higher electrical conductivity than SnAg-based solder [20]. Several studies verified that the nano-silver sintering joints have a much better reliability than conventional solders [20], [25]. The material used in this study is the nanoTach from NBE [26]. Properties and sintering process of this material can be found in the literature [19], [25], [27].

TABLE II

LAYER CONFIGURATION

The proposed module		The DBC based module	
Layers	Dimensions (mm)	Layers	Dimensions (mm)
Top lead (Mo/Mo-Cu)	5×5×0.1	Al bond-wires	d=0.38
Nano-silver paste	5×5×0.05	SiC die	5×5×0.18
SiC die	5×5×0.18	Nano-silver paste	5×5×0.05
Nano-silver paste	5×5×0.05	DBC copper top	15×15×0.2
Metal Substrate (Mo/Mo-Cu)	15×15×2	DBC ceramic (Si3N4)	15×15×0.32
Resin bonding	15×15×0.2	DBC copper bottom	15×15×0.2
Heatsink (Mo/Mo-Cu)	15×15×3	DBC solder (SnAg solder)	15×15×0.25
		Baseplate (copper)	15×15×2
		TIM	15×15×0.16
		Heatsink (copper)	15×15×3

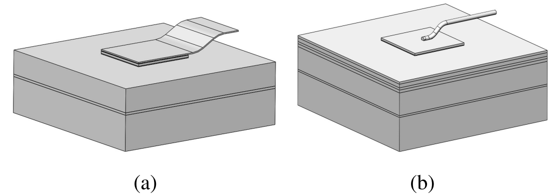


Fig. 3. Single-die modules. (a) Proposed module. (b) DBC module.

C. Design of Single-Die Modules

Single-die modules are designed for the following simulations, including one module based on the proposed concept and another one based on conventional DBC packaging, as a benchmark. For simplification, the circuit tracing on the substrate and complex interconnections are avoided in these single-die modules. A SiC MOSFET die in the size of 5 mm × 5 mm × 0.18 mm (unlisted product) is used for both modules.

The structures of these two modules are illustrated in Fig. 3. The material matrix and dimensions of layers are listed in Table II. In general, these two modules have similar footprints.

III. STEADY-STATE THERMAL–MECHANICAL EVALUATION

This section investigates how the ratio of Cu in Mo–Cu alloys affects the thermal–mechanical performance of the proposed module and guide the material selection. The proposed module will also be compared with the DBC module to verify

the expected advantages. This analysis is carried out by steady-state thermal–mechanical FEAs.

The heat transfer in a power module has been widely discussed in the literature. Generally, the heat is generated at semiconductor dies. Then, it is transferred from dies to the heatsink by conduction through solid layers. Finally, the heat is dissipated at the heatsink by convection to the ambient air or coolant. This process is elaborated in (1)–(5).

At the top of the die

$$\left.\frac{\partial T}{\partial z}\right|_{z=0} = -\frac{Q}{k_{\text{die}} A}. \tag{1}$$

Conduction within each solid layer

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0. \tag{2}$$

Conduction at the contact between the ith to the $(i+1)$th solid layers

$$k_i \left.\frac{\partial T_i}{\partial z}\right|_{z=z_i} = -k_{(i+1)} \left.\frac{\partial T_{i+1}}{\partial z}\right|_{z=z_i} \tag{3}$$

$$T_i(x, y, z_i) = T_{i+1}(x, y, z_i). \tag{4}$$

Convection at the bottom of the heatsink

$$k_{\text{heatsink}} \left.\frac{\partial T_{\text{heatsink}}}{\partial z}\right|_{z=z_{\text{heatsink}}} = -h(T_{\text{heatsink}} - T_{\text{coolant}}). \tag{5}$$

In the equations above, T is the temperature, and T_i is the temperature of the ith layer at the contact point. z_i denotes the distance from the bottom of the ith layer to the top of the die. Q represents the heat, and A is the surface area of the die. k_i is the thermal conductivity of the ith layer. h denotes the convection coefficient of the convection cooling.

In power modules, the major concern due to high temperature is the thermal stress and strain, which is critical to the lifetime of the module. When a material is subjected to thermal expansion, its ε_a (actual strain) is the difference between the ε_{uc} (unconstrained thermal strain) and the ε_c (constrained strain), as shown in (6) and (7). The ε_c will cause stress which can be expressed by (8) for elastic materials. Derived from the above theories, the stress caused by material A to another contacted material B by thermal expansion can be expressed as follows [28]:

$$\varepsilon_a = \varepsilon_{\text{uc}} - \varepsilon_c = \frac{L_T - L_{\text{ref}}}{L_{\text{ref}}} \tag{6}$$

$$\varepsilon_{\text{uc}} = \alpha(T - T_{\text{ref}}) \tag{7}$$

$$\sigma = E \cdot \varepsilon_c \tag{8}$$

$$\sigma_B = \frac{E_B \cdot E_A \cdot \Delta\text{CTE} \cdot \Delta T}{E_B + E_A} \tag{9}$$

where E means the elastic modulus of the materials. T_{ref} is the stress-free reference temperature which is typically the room temperature. L_{ref} is the length of the material at the reference temperature.

Reducing the CTE mismatch between materials helps reduce thermal stress. However, among the pure Mo and Mo–Cu alloys, the one with a closer CTE to SiC has a lower k, which leads to a higher temperature. Thus, there is a tradeoff to be made in material selection, which will be determined by the following simulations.

TABLE III
THERMAL–MECHANICAL PROPERTIES [22], [23]

Material	E (Gpa)	Poisson's ratio	k (W/m-K)	CTE ($1\times10^{-6}/^{o}$C)
SiC	420	0.14	120	4
Si_3N_3	310	0.25	30	3.3
Mo	330	0.31	138	5.3
Mo85Cu15	280	0.31	170	6.8
Mo70Cu30	230	0.31	190	7.5
Mo60Cu40	210	0.32	230	8.7
Mo40Cu60	170	0.33	290	11.5
HL832NSF	32	0.19	0.7	5.5
TIM	-	-	0.7	-
Aluminum	70	0.35	237	23
Copper	110	0.34	401	17
Nano Silver Paste	20	0.37	200	19.6
SAC405 SnAg Solder	40	0.37	50	20

A. Steady-State FEA Modeling

The simulation is conducted in ANSYS Mechanical. To simplify the problem, simulations are subject to several assumptions as follows.

1) The modules are considered symmetric. Thus, only a quarter section is applied in the FEA model.
2) As discussed above, the silicone gel is ignored.
3) The heat generation in the die is volumetrically uniform.
4) Except for the bottom of the heatsink, other surfaces are adiabatic.
5) For the DBC-based module, the bottom of the baseplate is fixed in the z-direction. Thus, the thermal grease and the heatsink have no impact on mechanical performance.
6) For the proposed module, the bottom of the heatsink is fixed in the z-direction.

According to these assumptions, boundary conditions are set for this simulation: 1) heat losses equivalent to 33 W is set on the dies; 2) the cooling boundary is a convection of 5000 W/m-K at the bottom of the heatsink with a coolant temperature of 25 °C; and 3) frictionless supports are assigned to the symmetry planes as well as the bottom surface of the DBC module's baseplate and the proposed module's heatsink.

The thermal–mechanical properties required for steady-state simulations are shown in Table III [22], [23]. The elastoplastic properties of aluminum and copper are modeled using the bilinear strain hardening curves, as shown in Fig. 4.

The solder and sintered nano-silver are visco-plastic materials. They are commonly modeled by Anand visco-plastic model in the literature [29], [30]. Anand model is usually used for large, isotropic, visco-plastic deformations, and small elastic deformations. Therefore, it is very suitable for solders and sintered nano-silvers. A single-scalar internal variable is used to construct the model, which is the deformation resistance (s). Anand model also requires no clear yield condition. The Anand model is described in (10), which shows the relationship between stress (σ) and the plastic strain rate ($\dot{\varepsilon_p}$).

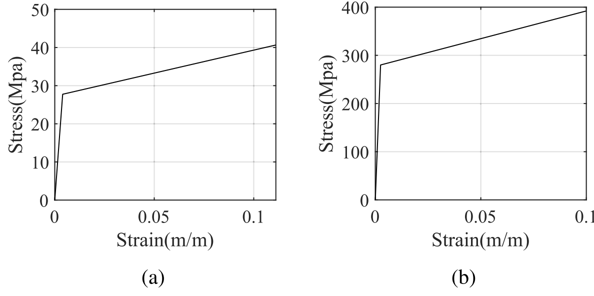


Fig. 4. Bilinear strain hardening curves. (a) Al. (b) Cu.

TABLE IV
ANAND MODEL PARAMETERS [20], [31]

Parameters	Nano Silver Paste	SAC405 SnAg Solder
Initial deformation resistance (s_o)	2.77×10^6	1.3×10^6
Activation energy (Q)	5709	9000
Pre-exponential factor (A)	9.81	500
Multiplier of stress (ξ)	11	7.1
Strain rate sensitivity of stress (m)	0.657	0.3
Hardening/softening constant (h_o)	1.58×10^{10}	5.9×10^9
Coefficient for Deformation Resistance Saturation ($\hat{s}$)	6.74×10^7	3.94×10^7
Deformation Resistance (n)	0.003	0.03
Strain Rate Sensitivity of Hardening/Softening (a)	1	1.1

Reference units (stress, temperature, time):Pa, K, s

Here, the plastic strain includes the creep strain. The evaluation of s is achieved in the following:

$$\dot{\varepsilon_p} = A \cdot e^{-\frac{Q}{TR}} \cdot \left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \tag{10}$$

$$\dot{s} = \left[h_0 \cdot |1 - \frac{s}{s^*}|^a \cdot sign\left(1 - \frac{s}{s^*}\right)\right] \cdot \dot{\varepsilon_p} \tag{11}$$

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon_p}}{A} \cdot e^{\frac{Q}{RT}}\right]^n \tag{12}$$

In these equations, R is the gas constant. T is the absolute temperature. s^* is the saturation value of s. Other involved parameters are shown in Table IV [20], [31]. The sintered nano-silver parameters are experimentally obtained by Yu *et al.* [31] based on a material with 82% relative density [32].

B. Results and Discussion

The steady-state thermal–mechanical performances of these modules are obtained from the simulations. Results are shown in Fig. 5. The junction temperature (T_j) and the thermal resistance (R_{th}) are two key values to evaluate the cooling performance of power modules. Among all the candidates, the material with the highest Cu ratio, that is, Mo40Cu60, leads to the lowest T_j and R_{th}, which is due to its highest thermal conductivity. For the DBC modules, although it has more layers, the massive application of Cu results in a better heat spreading, thus, a lower R_{th} is observed.

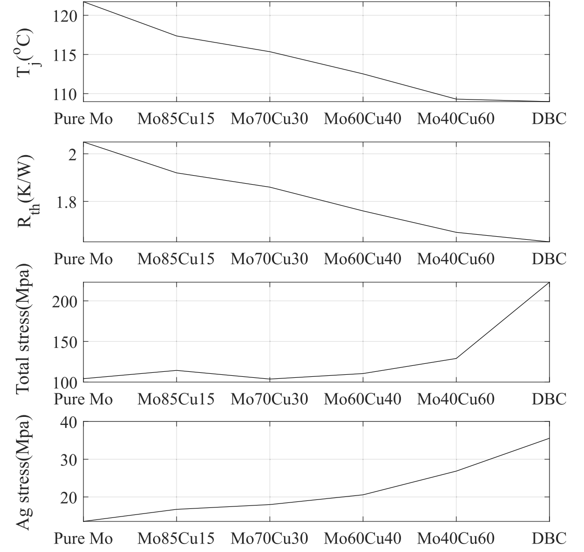


Fig. 5. Steady-state FEA results.

In our design, the critical temperature of all the materials, such as melting temperature and glass transient temperature, is greater than 220 °C, which is much higher than the typical maximum operating temperature of power modules (150 °C–175 °C). The real concern is actually the thermal stress/strain caused by thermal expansion, which is the source of major failure modes. As aforementioned, these thermal–mechanical issues are not only affected by the temperature, but also by the mechanical properties of materials, such as CTE and elastic modulus. In the other words, a proper selection of material could reduce the risk of failure despite the possible sacrifice of thermal resistance and junction temperature.

In the steady-state thermal–mechanical simulations, the thermal stress is viewed as the criteria in evaluating the performance of different materials. Lower thermal stress could prevent cracking and usually improve the resistance of fatigue [33]. From Fig. 5, it can be seen that the proposed module with pure Mo exhibits significant advantages in thermal stress. Compared with the DBC module, it reduces the total stress by a half and the critical stress (stress at the silver sintered layer) by 62%. Therefore, pure Mo is the best option.

In conclusion, this simulation is demonstrated as follows.

1) For the proposed module, the higher the Cu ratio, the better the heat transfer, but the worse the thermal stress.
2) Pure Mo results in significantly lower thermal stress. Therefore, it is selected as the material for the proposed module. And the proposed packaging concept is named the silver-sintered Mo (SSM) packaging, whose layer stack-up is shown in Fig. 6.
3) Although the DBC-based module could have better heat transfer, it has much higher thermal stress which could increase the risk of failure to a great extent.

Based on the results, the SSM module should have an improved lifetime and temperature durability than the benchmark module. Section IV will further investigate the expected advantages.

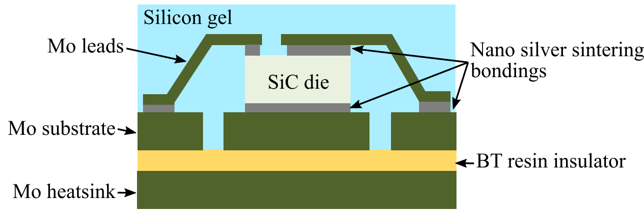


Fig. 6. Layer stack-up of the SSM packaging.

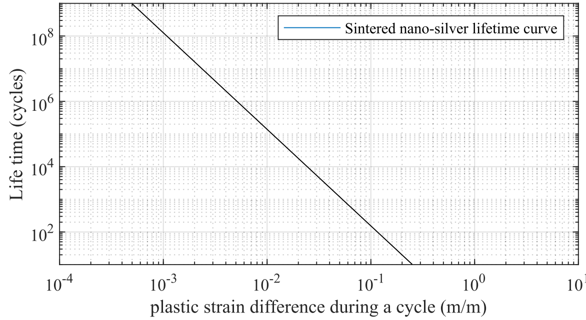


Fig. 7. Coffin–Manson lifetime characterization of nano-silver sintering bonding [19].

IV. Transient Thermal–Mechanical Evaluation

In this section, the advantage of the proposed SSM packaging in improving the lifetime and temperature range will be investigated using transient FEAs based on the JEDEC standard temperature cycling methods.

A. Lifetime Model

Power modules are subjected to multiple failures and fatigue modes, among which the fatigue at the die bonding and bond wires are viewed as the most critical ones. Since the bond wires are eliminated in the SSM packaging, the only mode discussed is the fatigue at the die bonding, the sintered silver layers.

The Coffin–Manson model [19], [20] is a widely applied method for analyzing the lifetime of metallic or solder materials under cyclic-plastic deformation. It has been used for nano-silver sintering die bonding in many studies. This model considers that the lifetime of the material has an exponential relationship with the plastic strain difference ($\Delta\varepsilon_p$) during a circle, as shown in the following:

$$N_f = C_1 \Delta\varepsilon_p^{-C_2}. \tag{13}$$

N_f denotes the lifetime (cycles), and C_1 and C_2 are material constants. The parameter characterization of the specific nano-silver materials used in this article (nanoTach from NBE) has been obtained by Knoerr *et al.* [19] through experiments, as shown in Fig. 7, in which one can obtain that C_1 equals 0.16 and C_2 is -2.96. The properties of the sintered nano-silver are largely dependent on its relative density (or porosity) [30]. The nanoTach material in Knoerr's work has a relative density of 75%–85%, which is close to the one used to construct the Anand visco-plastic model. Therefore, it is reasonable to combine all those parameters in simulations.

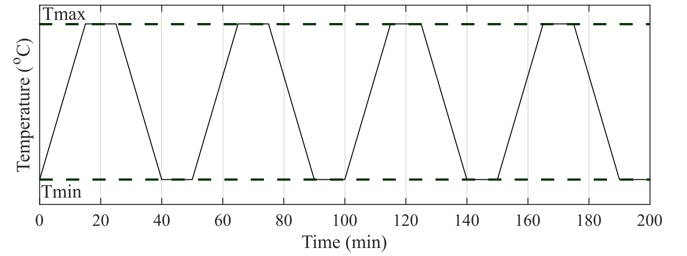


Fig. 8. JEDEC temperature cycling profiles [34].

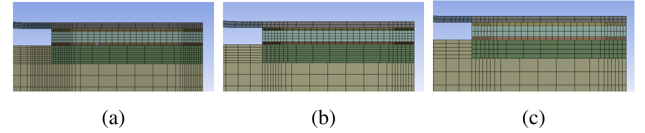


Fig. 9. Different sizes for mesh sensitive study. (a) 0.5× mesh size. (b) 0.75× mesh size. (c) 1× mesh size.

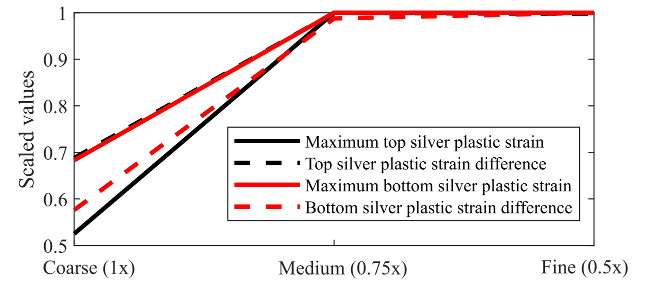


Fig. 10. Mesh sensitive study.

B. Temperature Cycling FEA Modeling

Temperature cycling is a standard approach to assess the lifetime of power modules. Several cycling profiles based on JEDEC standard [34] are applied in this analysis. The profiles of these cycling processes are shown in Fig. 8. All the cycling profiles used in this article have a $T_{\min}$ of -40 °C, while $T_{\max}$ varies.

Transient FEAs are carried out in ANSYS to implement these temperature cycling processes. The cyclic temperature is set for the entire module. Thus, the heat generation and cooling boundaries in the steady-state simulations are no longer applied. Other boundary conditions remain the same.

Transient FEAs are exceptionally time-consuming. It is not practical to apply extremely fine meshing. A mesh sensitive study is conducted to determine the suitable mesh size that guarantees reliable results with affordable simulation time. As shown in Fig. 9, three different meshings with 0.5×, 0.75×, and 1× element size at the critical regions are compared.

Fig. 10 shows that the simulation results get stabilized at 0.75× and 0.5× element size. Eventually, 0.5× element size is used for all the simulations.

The convergence plots can be used to further judge the confidence level of the transient FEA model. Fig. 11 shows the force and displacement convergence plots. It can be seen that the model converged quickly after 1–3 iterations for each sub-step, which indicates that this model is properly defined.

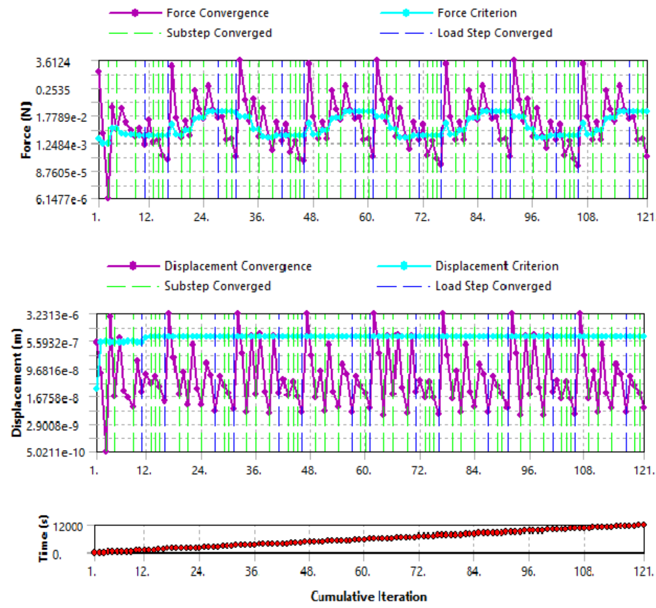


Fig. 11. Convergence analysis of transient FEAs.

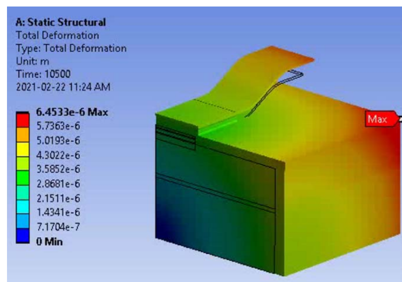


Fig. 12. Total deformation of SSM module under −40 °C to 125 °C cycling.

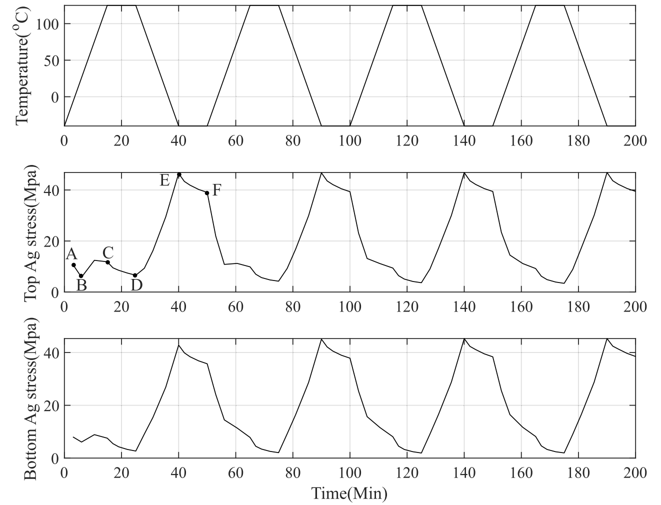
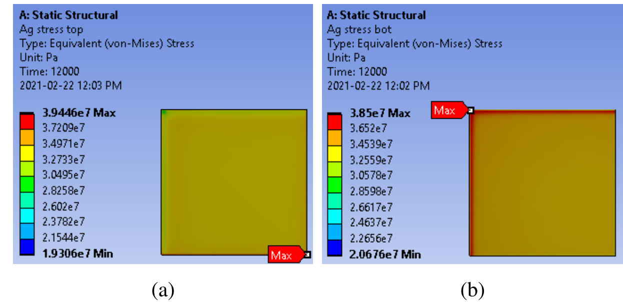


Fig. 13. Stress of SSM module under −40 °C to 125 °C cycling.



(a) (b)

Fig. 14. Stress profiles at silver layers (a) top and (b) bottom.

C. SSM Module Under −40 °C–125 °C Cycling

The temperature cycling between −40 °C and 125 °C is used as an example to explain the transient thermal–mechanical behavior of the SSM module. The total deformation of the module at the 175 min is shown in Fig. 12. Obviously, the maximum deformation appears at the farthest end.

As discussed above, the critical components are the bonding layers. For the SSM module, there are two bonding layers located at both the top and the bottom of the die. The stress fluctuation curves of these two layers during this cycling are shown in Fig. 13. In general, these two layers went through similar stress changes; however, the maximum stress at the top silver layers (46.8 MPa) is slightly higher than that of the bottom silver layer (45.3 MPa). Stress relaxation is observed during this process. Take the first cycle of the top silver layer as an example. From A to B, the stress decreases because the temperature approaches 25 °C (the stress-free temperature) from −40 °C. From B to C, the temperature continues to increase until it reaches 125 °C, however, the stress from thermal expansion is compensated by the stress relaxation, which allows the actual stress to first increase and then decrease slightly. From C to D, when the temperature load is fixed at 125 °C, the stress is brought down by stress relaxation only. During the cooling process from D and E, the stress elevates fast due to the compression. Then, the stress relaxation is dominant again during the second constant temperature region (E and F). Specifically, the stress relaxation is caused by the creep of the sintered nano-silver which has rate-dependent visco-plastic properties. The creep of the bonding layer relaxes the strain, which releases the elastic stress at the contacted layers (SiC and Mo). Consequently, the stress at the sintered nano-silver is reduced as well. Intrinsically, these creep and stress relaxation is due to mechanisms such as dislocation glide, dislocation creep, and diffusional flow (Nabarro creep) in the sintered nano-silver [30].

The stress profiles of these two layers at the end of the cycling are exhibited in Fig. 14. For both layers, the maximum stress points are located at the corners. First of all, stress concentration is always seen at sharp edges. Meanwhile, the edges and corners are subjected to the mismatch of thermal expansion by different materials. Therefore, they are typically the most critical regions. Similar stress distribution at the bonding layer obtained by FEA simulation has been reported by Zhang [20] and Cao *et al.* [35]. In fact, it is found that the corners are usually where cracks initiate [35], [36], which brings failures and fatigue.

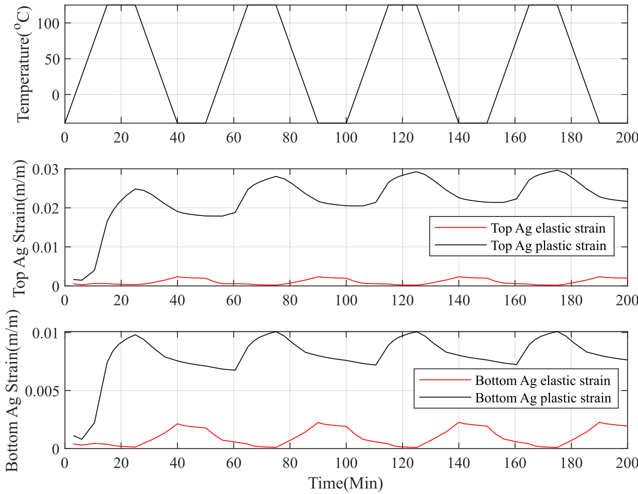
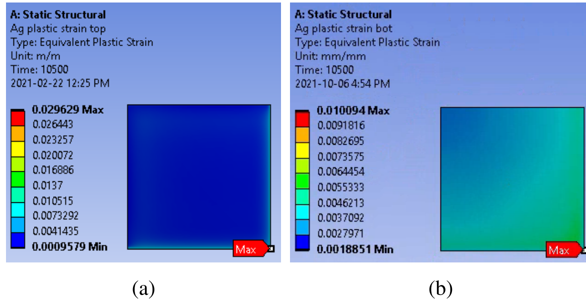


Fig. 15. Strain of the SSM module under −40 °C to 125 °C cycling.



(a) (b)

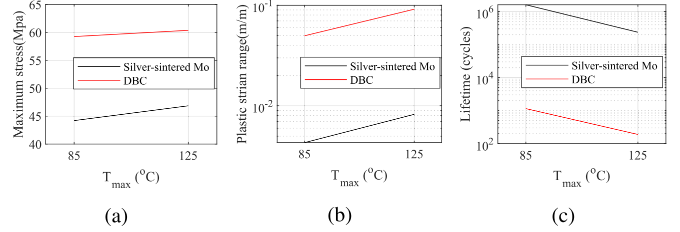
Fig. 16. ε_p profiles at silver layers: (a) top and (b) bottom.

According to the Coffin–Manson model, the strain profiles are directly related to the lifetime of these materials. Fig. 15 illustrates the fluctuation curves of the strain during the temperature cycling, including both the elastic and plastic strains. Overall, the strain curves are stabilized after two cycles. For both the top and the bottom layers, the elastic strain is much smaller than the plastic strain, which demonstrates again that this is a plastic-dominant deformation. The bottom silver layer is clamped by the SiC die and the thick Mo substrate which has a frictionless support boundary at its bottom surface. In contrast, the top silver layer is clamped by the SiC and the thin Mo lead which is free to move. Therefore, the bottom layer is better constrained. In the simulation results, the bottom layer also undergoes less deformation and during cycling. Therefore, the maximum plastic strain (0.0296 m/m) of the top silver layer is nearly 3× larger than that of the bottom layer (0.0101 m/m). More importantly, the $\Delta\varepsilon_p$ of the top layer (0.0082 m/m) is also much larger than that of the bottom layer (0.0029 m/m). Thus, the top silver layer is subjected to a higher risk of fatigue.

The plastic strain distributions of these two layers are shown in Fig. 16. Similar to the stress distribution, the maximum points are located at the corners.

D. Comparative Studies and Lifetime Analysis

A few more temperature cycling processes are simulated to compare the performance of the SSM module and the conventional DBC module. As explained above, the top silver layer is more critical in the SSM module. Thus, it is to be compared with the bonding layer in the DBC module.



(a) (b) (c)

Fig. 17. Comparative study. (a) Stress at silver bondings. (b) $\Delta\varepsilon_p$ at silver bondings. (c) Lifetime.

Two most commonly used cycling processes from JEDEC, −40 °C to 85 °C and −40 °C to 125 °C, are used for the comparison, which are shown in Fig. 17. Apparently, the higher $T_{\max}$ leads to higher stress and plastic strain difference, causing a shorter lifetime for both modules. However, the differences between the two modules are significant. Under both −40 °C to 85 °C cycling and −40 °C to 125 °C cycling, the SSM module has nearly 25% lower maximum stress at the bonding, 10× lower plastic strain difference, and over 1000× longer lifetime. The results demonstrated that the proposed SSM packaging has a significantly better performance in fatigue and lifetime than the DBC packaging.

In Table V, the results are compared with data from Knoerr's experiments [19], where the Coffin–Manson parameters used in simulations are obtained. In Knoerr's work, it is proved that the module with silver sintering bonding has a much longer lifetime than the one with conventional SnAg solders. Comparing all the DBC modules using nano-silver sintering bonding (cases C–F), the cases from this article (cases E and F) are predicted to have a slightly longer lifetime than those from the literature, which is mainly due to a smaller temperature range during thermal cycling. Also, different die sizes (Si diode versus SiC MOSFET) and DBC materials (Al_2O_3 versus Si_3N_4) could affect the results. Overall, all these lifetime values are in the same magnitudes, indicating that the simulations in this article have a decent confidence level. Cases G and H are the simulation results of nano-silver sintering with Mo substrates, which have a remarkably longer lifetime than others. This is mainly due to the low $\Delta\varepsilon_p$ during each cycle (around 4×10^{-3} and 8×10^{-3} m/m, respectively). As discussed before, the CTE difference between the SiC die and the Mo substrate is significantly smaller than between the SiC die and DBC substrate coppers. Therefore, the advantage can be expected. In fact, similar to case H, a case with a $\Delta\varepsilon_p$ of 8×10^{-3} m/m is also reported in Knoerr's work [19]. Such a case is likely to be achieved by having a short duration or a small temperature range during thermal cycling with DBC substrates. The experimental result of lifetime of this case is around 2×10^5, which agrees with case H very well. Thus, it is safe to conclude that the SSM packaging has an advantage regarding lifetime over the conventional module.

From another perspective, the SSM packaging's superior thermal–mechanical performance can elevate the maximum

TABLE V
LIFETIME COMPARISON WITH BENCHMARK FROM LITERATURE

Source	Cases	Packaging type	Bonding type	Methods	Temperature cycling profiles	Life-time (cycles)
Literature [19]	A	Si Diode with DBC (Al_2O_3) packaging	SnAg solder	Experiment/Conffin-Manson model	-5 ^{o}C to 175 ^{o}C (60 min per cycle, 7.7 ^{o}C/min ramp rate, no dwell time)	87
	B	Si Diode with DBC (Al_2O_3) packaging	SnAg solder	Experiment/Conffin-Manson model	-55 ^{o}C to 175 ^{o}C (60 min per cycle, 7.7 ^{o}C/min ramp rate, no dwell time)	51
	C	Si Diode with DBC (Al_2O_3) packaging	Nano silver sintering	Experiment/Conffin-Manson model	-5 ^{o}C to 175 ^{o}C (60 min per cycle, 7.7 ^{o}C/min ramp rate, no dwell time)	790
	D	Si Diode with DBC (Al_2O_3) packaging	Nano silver sintering	Experiment/Conffin-Manson model	-55 ^{o}C to 175 ^{o}C (60 min per cycle, 7.7 ^{o}C/min ramp rate, no dwell time)	105
This paper	E	SiC MOSFET with DBC (Si_3N_4) packaging	Nano silver sintering	Conffin-Manson model	-40 ^{o}C to 85 ^{o}C (50 min per cycle, 8.3 ^{o}C/min ramp rate; 10 min dwell time)	1152
	F	SiC MOSFET with DBC (Si_3N_4) packaging	Nano silver sintering	Conffin-Manson model	-40 ^{o}C to 125 ^{o}C (50 min per cycle, 11 C/min ramp rate; 10 min dwell time)	190
	G	SiC MOSFET with SSM packaging	Nano silver sintering	Conffin-Manson model	-40 to 85 (50 min per cycle, 8.3 C/min ramp rate; 10 min dwell time)	1609510
	H	SiC MOSFET with SSM packaging	Nano silver sintering	Conffin-Manson model	-40 ^{o}C to 125 ^{o}C (50 min per cycle, 11 ^{o}C/min ramp rate; 10 min dwell time)	236459

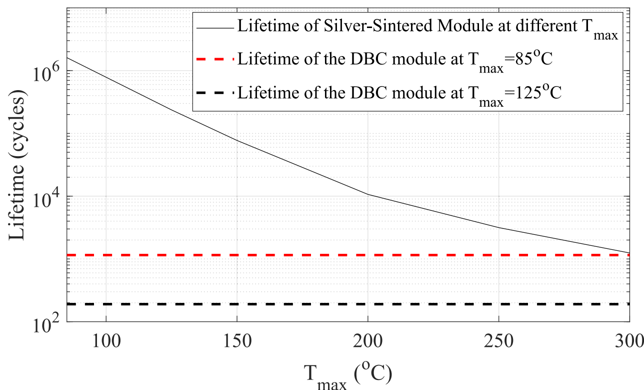


Fig. 18. Lifetime comparison between the SSM module and the DBC module at different $T_{\max}(T_{\min} = 40\ ^\circ\text{C})$.

operating temperature of power modules. More thermal cycling profiles are implemented to verify this advantage. In these profiles, $T_{\min}$ are all set to be $-40\ ^\circ$C, while $T_{\max}$ changes from 85 °C to 300 °C.

In Fig. 18, the relationship between lifetime and $T_{\max}$ for the SSM packaging can be found. Meanwhile, the lifetime values for the DBC module under temperature cycling with 85 °C $T_{\max}$ and 125 °C $T_{\max}$ are set as benchmarks. A more obvious trend of lifetime descending with temperature can be seen in this plot. More importantly, the proposed module has nearly the same lifetime at 300 °C $T_{\max}$ to that of the DBC module at 85 °C $T_{\max}$. This means that the SSM module has the potential to operate at a much higher temperature and a larger temperature range with a similar lifetime expectation to the conventional technologies.

V. SILVER SINTERING ON MO SUBSTRATES

It is important to prove that the proposed SSM packaging is manufacturable. Among all the steps, using nano-silver sintering to bond SiC dies on Mo substrates is the most challenging and uncertain one. Extensive studies on sintering dies onto DBC substrates can be found in the literature. However, applying this bonding method with Mo substrates has been rarely mentioned and needs further investigation.

A. Sintering Process

Nano-silver sintering is a solid-state atomic diffusion process driven by the reduction of total surface energy and/or interfacial energy [30]. It has been reported that nano-silver sintering could exhibit significantly better performance when the contact material has a similar atomic number and lattice structure with silver. Silver itself and gold are the most common recommendations for the contact material when it is bonded to DBC substrates. Molybdenum has a different lattice structure with silver. Also, molybdenum might form oxidized layers at the sintering temperature, which could reduce the bonding quality. Therefore, directly sintering the die on the bare molybdenum surface is unlikely to be successful. In this article, both bare Mo and coated Mo are investigated. The surface on the SiC chip has three layers of metallization, which are Ni(0.6 μm)/Pb(0.2 μm)/Au(0.1 μm). And the metallizations on the coated Mo are Ru(0.15 μm)/Ag(0.3 μm) achieved by magnetron sputtering coating. Pb, Ni, and Ru are diffusion barriers, which prevent silver from penetrating the metallization layers into SiC or Mo.

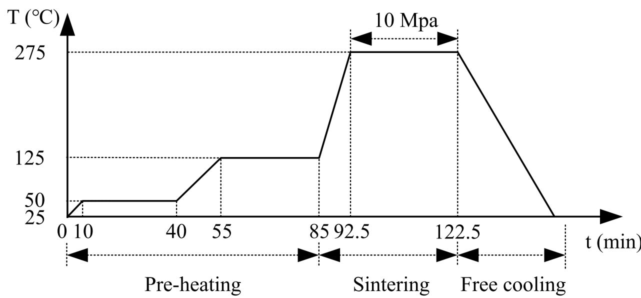


Fig. 19. Sintering profile.

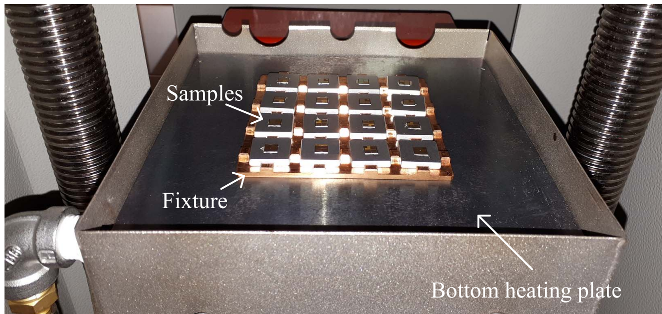


Fig. 20. Manufacturing setup.

The sintering parameters are mainly based on Knoerr's work [19] and Yu's work [31], which are also the main reference for material properties in the former simulations. However, the process is modified according to recommendations from the supplier (NBE) [26] and several other studies [27], [37]. The holding time at the sintering temperature is extended to 30 min, and the sintering pressure is set to be 10 MPa, which is likely to result in a denser bonding compared with the references. The sintering profile is shown in Fig. 19. First, the sample is pre-heated at 50 °C and 125 °C in order to completely evaporate the organic constituents in the nano-silver paste. Then, the temperature is quickly increased to 275 °C to perform sintering and achieve densification. The pressure is applied during the sintering stage. And finally, the sample is free cooled to room temperature (25 °C). The entire process is taken place in the air because oxygen is needed to evaporate the organics.

A heat-press is used to manufacture the samples, as shown in Fig. 20. The nano-silver paste of around 60 μm thickness is screen printed onto Mo substrates using a customized stencil.

B. Results and Discussion

As introduced, both bare Mo and Mo coated with Ru/Ag are studied. The sintered samples are shown in Fig. 21. As expected, the bonding with the bare Mo substrate is failed, where the SiC die falls off the substrate with a very gentle push. The surface of the bare Mo substrate is partially oxidized. However, the SiC die is successfully bonded on the Ru/Ag-coated Mo substrate. In order to further evaluate the bonding quality, a scanning electron microscope (SEM) is used to image the bonding line. As can be seen in Fig. 22,

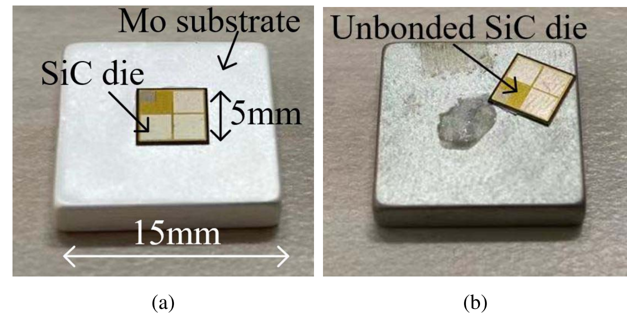


Fig. 21. Sintered samples. (a) Sample with Ru/Ag-coated Mo substrate. (b) Sample with bare Mo substrate.

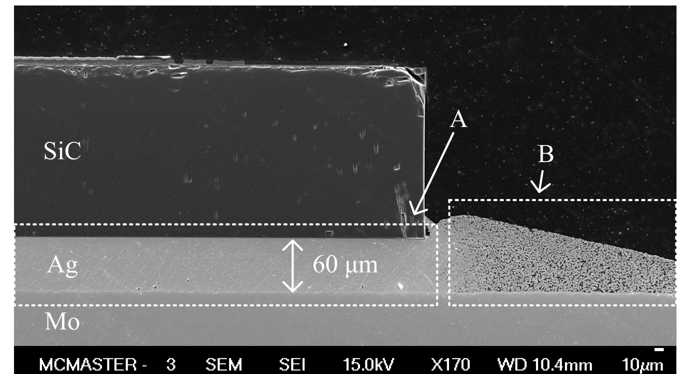


Fig. 22. SEM image of the sintered sample with Ru/Ag-coated Mo.

a sliver layer around 60 μm is formed between the SiC chip and the Mo substrate. In area A, where the pressure is applied, a very dense bonding line is achieved. No cracks or large voids can be found. And the porosity of this area is significantly smaller than what is reported in Knoerr's work [19] and Yu's work [31]. Therefore, it should exhibit an even better performance regarding strength and reliability. On the contrary, more and larger pores can be seen in area B (excessive silver materials outside of the die area) where the pressure is not applied. This demonstrates that pressure can help achieve a better bonding quality. Overall, a feasible process of sintering the die on the Mo substrate is proposed and evaluated, including the metallization, the temperature profile, and the pressure value. It demonstrates that the SSM packaging can be manufactured.

VI. Conclusion

Improving the lifetime and maximum temperature durability of power modules is necessary for the next-generation power electronic systems. In the future of large-scale applications of WBG devices, the revolution of packaging technology is the key to meet the increased performance requirements. This article proposed a new packaging, called the silver-sintered Mo packaging, which can significantly improve the power module's lifetime and increase maximum operating temperature.

In this article, the layer stack-up of the proposed packaging concept was introduced first. Several metallic materials were discussed. And Mo–Cu alloys with different copper ratios were considered as candidate materials for the metal layers.

Then, steady-state thermal–mechanical FEAs were conducted to finalize the material selection of the metal layers. It also preliminarily verified the advantage of the proposed module against the conventional DBC-based module. In the simulation, pure Mo resulted in the lowest thermal stress due to its low CTE. Thus, it was selected as the material for all the metal layers. And the proposed module was named the SSM module. Compared with the conventional DBC modules, the SSM module had 53% less total stress and 62% less stress at the bonding layers in the steady-state thermal–mechanical FEAs.

Next, the lifetime and temperature range analysis based on the Coffin–Manson model was implemented using transient temperature cycling FEAs. The results were compared with experimental data of similar works from the literature. It was found that the top silver layer was subjected to a higher risk of fatigue than the bottom silver layer. Compared with the DBC module, the SSM module exhibited over 1000× longer lifetime under various cycling conditions. On the other hand, the proposed module achieved 300 °C $T_{\max}$ while maintaining the same lifetime expectation of the DBC module with 85 °C $T_{\max}$.

Finally, the manufacturability of the proposed SSM packaging was evaluated. The key process, sintering SiC dies on the Mo substrates, was studied. A feasible sintering profile was proposed, and SEM imaging showed that a high-quality bonding was achieved on the Ru/Ag-coated Mo substrates.

In future works, the sintering process will be further optimized. And a power module implementing a half-bridge topology will be designed, which will be fully characterized experimentally to evaluate the expected advantages. Outcomes of this research will result in an innovative, efficient, and robust packaging technology for the next-generation WBG power electronic systems.

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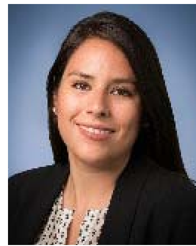

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