

# Foreword

## Special Section on “Advances in Electrical Modeling and Validation of Electronic Packaging and Systems”

**I**N A time where the demands for electronic systems and components are rising in an unprecedented fashion, the complexity for designing these components and systems is increasing at a similar pace. From wearable and handheld devices to autonomous vehicles to data centers and supercomputers, the growing amount of integration and the demand for more efficient access to ever-increasing data are pushing the state-of-art design methods to their limits. In this environment, innovative research is necessary to push the capability of electrical modeling and validation methods in order to equip the electronic design community with the most adequate tools to tackle the emerging challenges.

This Special Section presents some exciting recent developments and improvements in the area of electrical modeling and validation of electronics packaging and systems and is built from selected works initially presented at the IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS 2020) and the 2020 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS 2020) conferences. It covers a wide range of topics, including novel innovations in several familiar topics such as computational electromagnetics, model order reduction, high-frequency validation, and power delivery modeling, as well as recent developments in nascent topics such as machine learning and uncertainty quantification. The eight articles in this section, including contributions from both industry and academia, were selected after a rigorous and careful peer-review process and present new technical contents beyond the original conference articles.

In the article “High-dimensional uncertainty quantification via tensor regression with rank determination and adaptive sampling,” He and Zhang propose a novel tensor regression method to automatically determine the tensor rank and adaptively pick the informative simulation samples. Such a method is critical to efficiently determine the impact of the fabrication process variations in electronic circuits and interconnects due to a large number of parameters.

“Error-controlled static layered medium Green’s function computation via hp-adaptive spectral differential equation approximation method,” by Li *et al.*, presents a

computationally efficient approach to evaluate a set of layered-media Green’s functions needed for method of moments capacitance and inductance extractions.

In the article “Pin impedance based figure of merit with mutual coupling (PMC-FOM) for assessment of a decoupling capacitor on polygonal parallel plates,” by Erdin and Achar, the circular approximation of the effective zone of decoupling capacitors (decap) is extended to polygonal shapes that take into consideration the mutual coupling between the capacitors. The results will give package designers improved feedback on decap placement without full-wave analysis.

“Fast simulation of analog circuit blocks under nonstationary operating conditions,” by Bradde *et al.*, proposes a black-box behavioral modeling framework for analog circuit blocks operating under small-signal conditions around nonstationary operating points. The proposed framework allows for the efficient and stable construction of behavioral models for various amplifiers and voltage regulators with nonstationary bias conditions.

In the article “Comparative study of surrogate modeling methods for signal integrity and microwave circuit applications,” Nguyen *et al.* provide a comparison between machine learning models built using non-parametric Gaussian process and other methods including partial least-square regression, support vector regression, and polynomial chaos. The robustness of the proposed approach is demonstrated via application to various high-speed and microwave design examples.

“Impact of measurement uncertainty on correlation quality for high-speed interconnects,” by Geyik *et al.*, presents a new method to validate models and quantify the accuracy of high-speed package interconnect measurements while accounting for randomness and uncertainties in measurements. This work has the potential to help package engineers build better models and gain more confidence in using these models for characterizing interconnects at increasingly high speeds where uncertainties must be considered.

In “A state-space based method to model Vccin feedthrough noise in microprocessors with fully integrated voltage regulators,” Govindan *et al.* use a hybrid network parameter model to simulate the feedthrough noise between different power domains on chips with fully integrated voltage regulators. These chips can reduce the complexity and cost of power delivery components on packages and boards. With

the new technique introduced here, feedthrough noise simulations can be performed using black-box models, thus avoiding time-consuming and potentially IP-exposing circuit simulations.

“Towards fully automated high-dimensional parameterized macromodeling,” by Zanco and Grivet-Talocia, presents a fully automated algorithm for the extraction of parameterized macromodels from frequency responses. Results show that models with up to ten independent parameters can be efficiently extracted with the proposed method compared to standard approaches, which tune these parameters using time-consuming tentative model extractions following a trial-and-error strategy.

As the Guest Editors of this Special Section and the Conference Chairs of EPEPS 2020 and EDAPS 2020, we would like to thank our TRANSACTIONS Senior Area Editor, Dale Becker, and the EPS Executive Director, Denise Manning, for their extensive support to this Special Section. Our special thanks also go to all the reviewers for their significant effort and valuable time spent on reviewing the articles and providing timely feedback. We would also like to express our gratitude to all the authors for adding new contributions to their conference articles and submitting high-quality manuscripts to this Special Section.

2020 was a very challenging year not only for the scientific community but also for the whole world in dealing with the consequences of the COVID-19 pandemic. For EPEPS 2020 and EDAPS 2020 conferences, this resulted in holding virtual conferences for the first time due to all the travel and social restrictions around the world. During such trying times, it was inspiring to see our EPEPS and EDAPS communities coming together and supporting each other, while still contributing to further advancement of science with their submitted papers, presentations, tutorials, exhibitions, and interactive discussions in these virtual conferences. We hope the papers in this Special Section will inspire researchers around the world to continue to push the boundaries for scientific achievements in the exciting area of electrical modeling and validation of electronic packaging and systems.

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**Kemal Aygün** (Senior Member, IEEE) received the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2002.

In 2003, he joined Intel Corporation, Chandler, AZ, USA, where he is currently a Senior Principal Engineer and manages the Electrical Core Competency Group, High Speed I/O (HSIO) Team. He has coauthored five book chapters, more than 80 journal, and conference publications, and holds 64 U.S. patents. His current research interests include novel technologies along with electrical modeling and characterization techniques for microelectronic packaging.

Dr. Aygün was a recipient of the Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) Mahboob Khan Outstanding Mentor Award in 2008 and 2015, for his contributions in mentoring SRC GRC academic research projects. He was the General Chair of the 2020 IEEE Electrical Performance of Electronic Packaging and Systems Conference. He is a Distinguished Lecturer of the IEEE Electronics Packaging Society.



**Xu Chen** (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign (UIUC), Urbana, IL, USA, in 2005, 2014, and 2018, respectively.

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Dr. Chen was a recipient of the Best Conference Paper Award at IEEE Electrical Design of Advanced Packaging and Systems in 2017. He was also a recipient of Raj Mittra Outstanding Research Award, Mavis Future Faculty Fellowship, U.S. National Committee for the International Union of Radio Science (USNC-URSI) Fellowship Grant Award, and others.