Comments and Corrections

Corrections to "A Fully Integrated Arbitrary Power Divider on Printed Circuit Board by a Novel SMD-Resistor-Free Isolation Network"

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In the above article [1], Figs. 22 and 24 were mistakenly reproduced in Figs. 25 and 21, respectively. The correct versions of Figs. 21 and 25 are provided here.

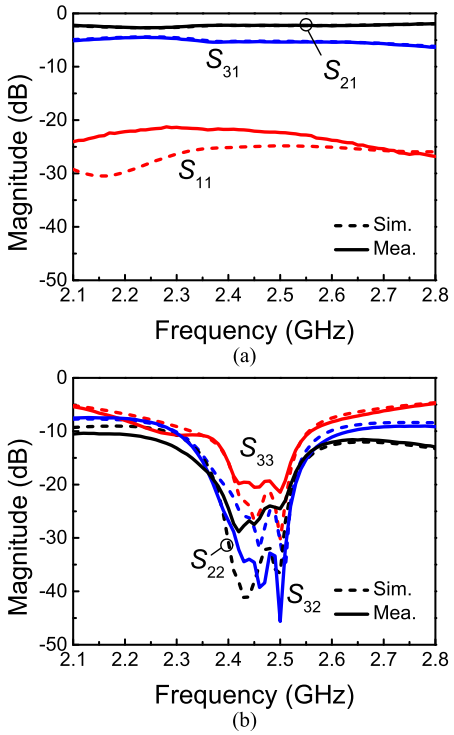

Fig. 21. Simulated and measured S-parameters of the proposed PD with a power division ratio of 2. (a) S_{11}, S_{21}, and S_{31}. (b) S_{22}, S_{32}, and S_{33}.

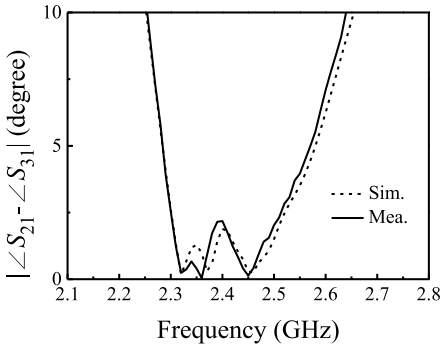

Fig. 25. Simulated and measured phase imbalance of the proposed PD with a power division ratio of 3.

In addition, (17) and (18) have been incorrectly published in [1]. The correct version should be

$$Z_{\text{in\_IDe}} = \frac{Z_{\text{in\_IUe}}}{k^2} = \infty \tag{17}$$

$$Z_{\text{in\_IDo}} = \frac{Z_{\text{in\_IUo}}}{k^2} = \frac{Z_{\text{t}}}{k}. \tag{18}$$

There is no impact of the change on further parts of the article [1].

References

[1] S. Chen and T.-L. Wu, "A fully integrated arbitrary power divider on printed circuit board by a novel SMD-resistor-free isolation network," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 10, no. 11, pp. 1889–1901, Nov. 2020, doi: 10.1109/TCPMT.2020.3029782.

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