Materials and Devices for On-Chip and Off-Chip Peltier Cooling: A Review

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(Invited Paper)

***Abstract*— The thermoelectric effect forms the basis of Peltier cooling that has attracted interest for solid-state refrigeration for more than a century. The dearth of materials level efficiency in converting between heat and electricity has limited widespread applications. With renewed focus on energy technologies in the past three decades, the thermoelectric effect has been intensely explored in new materials using state-of-the-art advances in materials fabrication, characterization techniques, and theory. This article aims to navigate the complex landscape of these studies to identify credible advances, pinpoint continuing problems, and lay out future prospects for both research and applications, with emphasis on electronics cooling.**

***Index Terms*— Electronic, optoelectronic, Peltier cooling, superlattice, thermoelectric.**

I. Introduction

By 2027, the market for thermoelectric materials is expected to reach U.S. $100M, driven by growth in the thermoelectric generators (TEGs) market, and is projected to cross U.S. $700M and more, by growth in the market for thermoelectric coolers (TECs), projected to reach U.S. $1.7B [1], [2]. The latter is a significant growth from 2019, where the market was ∼U.S. $675M. Current prominent applications of TECs include consumer electronics, communications, medical experiments, automobiles, and aerospace [3]. Lasers, charge-coupled device (CCD) cameras, automobile batteries, portable refrigerators, and car seats have all discovered use for thermoelectric cooling [4]. However, for more demanding applications such as in the thermal management of microprocessors, TECs still remain outside the realm of practicable solution. Nevertheless, TECs continue to attract interest for the perceived advantages of compactness, absence of moving parts, and fast response times. The past three decades have witnessed dramatic activity in thermoelectric materials research. Improved understanding of transport through better theoretical and experimental tools, supported by advances in nanomaterials synthesis has led to reports of breakthrough thermoelectric properties [5]–[8]. Efforts to translate these laboratory breakthroughs into commercial solutions are still nascent.

Meanwhile, the electronics industry has evolved growth strategies that deviate from traditional transistor scaling and focus increasingly on denser packaging. The current microprocessors have peak power densities in the order of several hundreds of W/cm^2 that are significantly greater than average power densities, often in the order of tens of W/cm^2 [9]. Spatial and temporal nonuniformities in power dissipation and temperatures are consequently very significant. Emerging cooling techniques such as microchannels-based heatsinks, microheat pipes, impinging jets, or magnetohydrodynamic-based cooling are still not adequate for site-specific thermal management inside the chip, hampered by the need for complex integration as well as lack of downward scaling [10]. Selective cooling near hotspots can, however, significantly reduce cooling power requirements for the whole chip. In this space, thermoelectric cooling may offer a niche thermal management solution. The historical disadvantage of TECs has been the lack of a material with a sufficiently high thermoelectric figure of merit, Z. A TEC is a heat engine whose idealized efficiency is governed by the product of Z and the average operating temperature, T. Over the past decade, extensive materials research has attempted to improve ZT by employing techniques such as alloying, nanostructuring, and band engineering. As an example, the ZT for Bi_2Te_3 alloys, the most common thermoelectric material, has been improved from ∼0.2 to 1.4 (at 373 K) [6].

Many excellent review articles on thermoelectrics have been written in the last two decades. These reviews primarily focus on material properties and methods for improving the thermoelectric figure of merit [11]–[17]. A handful of reviews consider practical details such as power supply, temperature sensing and cooling [3], [18], and cover modeling approaches used to analyze thermoelectric phenomena [19]. The objective of this article is to elucidate the current state of the art from the perspective of potential technology implementation in electronics cooling. This article thus focuses on practical issues of relevance to electronics cooling.

This article is organized as follows. Section II covers the basic physics of thermoelectricity in brief, whereas Section III focuses on materials, with emphasis on the 300–400 K temperature range. Section IV introduces devices for thermoelectric cooling and their operation. Section V summarizes past investigations into thermoelectric cooling of hotspots and integration into chips. Section VI discusses the more

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niche Peltier cooling at junctions internal to a semiconductor device. Section VII discusses the effect of parasitic losses on device performance and Section VIII discusses device reliability. Section IX provides a perspective on future applications of TECs in high-power density electronics applications. Section X concludes this article with a summary of key points and an outlook.

II. Basic Thermoelectric Phenomena and Materials Physics

As mentioned above, a temperature-dependent dimensionless figure of merit (ZT) is the material parameter governing ideal performance [20]. We note that ZT does not include the effects of thermal and electrical contact resistances, boundaries, and heatsink conductance which can each play a major role in practice. The figure of merit is given by $S^2\sigma T/(k_e + k_{ph})$, where S, σ, k_e, and k_{ph} denote the Seebeck coefficient, electrical conductivity, electronic thermal conductivity, and phonon thermal conductivity, respectively, at an average absolute temperature (T) of the device. $S^2\sigma$ is termed the thermoelectric power factor (PF). A high ZT material should thus combine a large PF with low thermal conductivity. Slack famously captured this in the term "phonon-glass/electron-crystal" (PGEC) whereby the best thermoelectric material should have the thermal properties of glassy or amorphous solids, and the electrical properties of crystalline materials [20].

The abovementioned transport coefficients can each be evaluated formally using solutions of the Boltzmann transport equation (BTE) for the nonequilibrium statistical distribution of the carriers conducting heat or charge, respectively. For bulk materials that obey parabolic dispersion relation the transport coefficients can be expressed as follows:

$$\sigma = \frac{8\sqrt{2}\pi q^2 N m_d^{3/2}\tau_0}{m^* h^3}(k_B T)^{\gamma+3/2}\left(\frac{2\gamma}{3}+1\right)F_{\gamma+1/2}(\zeta) \quad (1)$$

$$S = \frac{k_B}{q}\left[\frac{(\gamma+5/2)F_{\gamma+3/2}(\zeta)}{(\gamma+3/2)F_{\gamma+1/2}(\zeta)} - \zeta\right] \quad (2)$$

$$k_e = L\sigma T \quad (3)$$

where

$$L = \left(\frac{k_B}{q}\right)^2\left[\frac{(\gamma+7/2)F_{\gamma+5/2}(\zeta)}{(\gamma+3/2)F_{\gamma+1/2}(\zeta)} - \left(\frac{(\gamma+5/2)F_{\gamma+3/2}(\zeta)}{(\gamma+3/2)F_{\gamma+1/2}(\zeta)}\right)^2\right] \quad (4)$$

here γ is given by the power law relaxation time $\tau(E) = \tau_0(E - E_0)^\gamma$, ζ is the reduced Fermi level given by $\zeta = (E_F - E_0)/k_B T$ where E_0 is the ground state energy, E_F is the Fermi energy, k_B is the Boltzmann's constant, q is the charge, m^* is the conductivity effective mass defined along the direction of electrical conduction, m_d is the density of states (DOS) effective mass, N is the valley degeneracy, h is the Planck's constant, L is the Lorentz number, and $F_j(\zeta) = \int_0^\infty z^j/(1+\exp(z-\zeta))dz$ is the Fermi–Dirac integral of order j.

Equations (1)–(4) can be further simplified depending on whether the material is nondegenerate (ND) ($|E_F - E_{c,v}| \gg k_B T$) or strongly degenerate (D) (metal like) ($|E_F - E_{c,v}| \ll k_B T$). To be strongly degenerate, E_F must be greater than $4k_B T$ with respect to the ground state energy [20]. S is further related to σ through the Mott relationship via the carrier concentration (n) as shown in the following equation [21]:

$$S = \frac{\pi^2 k_B^2 T}{3q}\frac{d(\ln\sigma)}{dE}\bigg|_{E=E_F} = \frac{\pi^2 k_B^2 T}{3q}\left[\frac{1}{\mu}\frac{d\mu}{dE} + \frac{1}{n}\frac{dn}{dE}\right]_{E=E_F}. \quad (5)$$

In cooling applications, it is the Peltier coefficient Π rather than S that governs device performance. These coefficients are related by the Kelvin relationship, $\Pi = ST$. Following a similar approach described earlier, expressions can be derived for Π. For example, for the ND and D cases, the Peltier coefficient takes the following forms [22]:

$$\Pi_{ND} \approx \frac{1}{q}[(\gamma+5/2)k_B T - E_F] \quad (6)$$

$$\Pi_D \approx \left(\frac{\pi^2 k_B^2}{3q}\right)\left(\frac{\gamma+3/2}{E_F}\right)T^2. \quad (7)$$

An increase in ZT can result from an increase in PF, a reduction in total thermal conductivity $k = k_e + k_{ph}$, or a combination of these two. As k_e is coupled with σ, the only viable option to reduce thermal conductivity entails decreasing k_{ph}. The phonon BTE can be used to derive an expression for k_{ph}. Details of the derivation can be found in [23] which eventually leads to

$$k_{ph} = \frac{1}{3}C_v \upsilon \Lambda \quad (8)$$

where C_v is the phonon heat capacity, $\Lambda = \upsilon\tau$ is the phonon mean free path, and υ is the phonon group velocity.

Unless the operating temperature is very low (<40 K), C_v and υ are almost constant in a material. According to (8), Λ must, therefore, be reduced to lower k_{ph}. The mean free path can be reduced through scattering processes such as grain boundary scattering, defect-induced scattering, and Umklapp scattering (scattering of phonons with each other) with various levels of success [24], [25].

III. Leading Materials and Their Synthesis

This section identifies leading thermoelectric materials and summarizes their properties. We discuss the obtainable range of material properties and point out suitable materials for cooling applications. We further provide insights into methods used in materials engineering to improve material properties. Thermoelectric materials are typically classified based on their electronic properties, but here we consider the temperature of operation to emphasize applications.

A. Materials in the Range 300–400 K

The common materials used in refrigeration are alloys of bismuth (Bi) and antimony (Sb) chalcogenides (Te, Se). Among these, bulk Bi_2Te_3 is widely used in practical applications due to its high PF and low k which leads to a high ZT of ~1 at room temperature, as shown in Fig. 1. The band

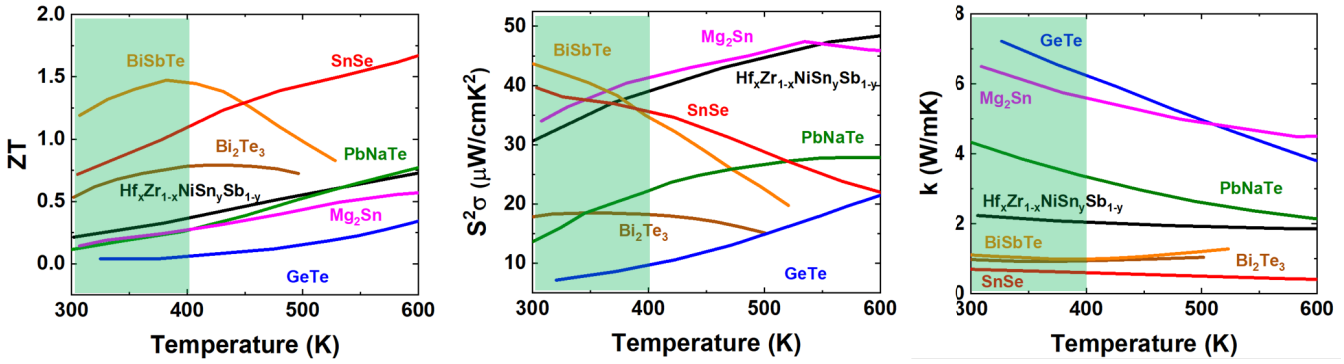

Fig. 1. (a) Thermoelectric figure of merit (ZT), (b) thermoelectric PF ($S^2\sigma$), and (c) thermal conductivity (k) as a function of temperature for various thermoelectric materials. At room temperature of 300 K, BiSbTe alloy possesses high $S^2\sigma$ where GeTe possesses high k. Since ZT is directly proportional to $S^2\sigma$ and inversely proportional to k, ZT is the highest for BiSbTe. References for the data can be found in Table I.

degeneracy of Bi_2Te_3 results in superior electronic transport properties and alloying introduces various defects leading to increased scattering of lattice phonons which reduces k [17], [26]. With increasing negative environmental effects of conventional fluorocarbon-based refrigeration methods, the Bi_2Te_3 refrigeration system has become a viable small-scale system. Recent research in Bi_2Te_3-based materials focused on improving ZT by using low-dimensional materials such as quantum wells, superlattices, quantum wires, and dots with reduced thermal conductivity. A very high ZT of 2.4 at 300 K was reported using a superlattice device made of Bi_2Te_3/Sb_2Te_3 [5]. The increase in ZT was attributed to the phonon-blocking/electron-conducting nature of superlattices. The ZT values and the physical attribution have not been validated independently. A ZT of 1.4 at 373 K was reported for nanostructured bulk alloy made of bismuth antimony telluride (BiSbTe) [6]. The increase in ZT was a result of lowering thermal conductivity due to increased scattering at grain boundaries and defects.

In the temperature range of 300–400 K, there does not appear to be much progress on materials for TEC-related applications beyond Bi_2Te_3-based materials. More recently, a study on thin-film half-Heusler alloy based on $Fe_2V_{0.8}W_{0.2}Al$ reported a very high ZT of ∼5 at ∼350 K [8]. This is attributed to a variation in DOS close to the Fermi level which leads to very high thermopower (S). The results are, however, debatable as this study involves an indirect measurement. The use of a conducting interfacial layer between the substrate and the thin film might have resulted in measurement errors while determining the temperature difference across the substrate for thermopower calculation. More work appears to be necessary to confirm these results. Another recent study investigating the thermoelectric properties of elemental Fe, Co, and Ni reported that the thermopower of these metals is highly influenced by the presence of magnons resulting in high thermoelectric PFs [27]. For Co, the peak $S^2\sigma$ was reported to be 160 $\mu W/cm \cdot K^2$ in the temperature range of 300–400 K. The authors proposed the idea of using metallic thermoelectric materials with high PF and k for active cooling of electronic devices [28]. More research is necessary in developing such metallic alloys with improved thermoelectric properties to realize active cooling in electronic devices using TECs.

B. Higher and Lower Range Materials

High temperature operation (between 600 and 800 K) is important mainly for TEG applications. Materials typically used in this temperature range are PbTe alloys. The inherently low k of PbTe has made it a leading material for high temperature TEGs. The low k value is attributed to phonon scattering due to the soft bonds between large atoms of Pb and Te [29]. Nanostructuring to reduce k_L and increasing the DOS through band structure engineering to improve S have been shown to be effective in PbTe based alloys [30]–[32]. At even higher temperatures, GeTe alloys, SiGe alloys, skutterudites, half-Heusler alloys, and silicides have emerged as leading materials, as shown in Fig. 1. Improvement of properties via nanostructuring, alloying, and band engineering has been explored in these materials [33]. To avoid the use of expensive and relatively rare Ge, improvements to the ZT of bulk Si have been explored through optimal doping and nanostructuring [34], [35]. Practical realization of thermoelectric modules using these materials requires efficient material processing and device integration techniques.

Organic thermoelectric materials such as PEDOT:PSS, and polyaniline possess low ZT values around 0.01 or lower in the temperature range of 250–400 K [15], [36]–[38]. They are good electrical conductors and can be readily patterned on large areas from commercially available organic solutions. They have been proposed as TEGs at low temperatures and explored for applications in flexible and wearable electronics since they are inexpensive and unreactive [39]–[41]. Recent research in organic thermoelectrics focused on developing nanostructured polymers, polymer/inorganic composites, and carbon nanotube-based composites to improve thermoelectric properties [42], [43]. At even lower temperatures, very few materials are known to exhibit desirable thermoelectric properties. Chung *et al.* [44] investigated thermoelectric properties of $CsBi_4Te_6$ to find peak $S^2\sigma$ and ZT at ∼225 K with values of ∼50 $\mu W/cm \cdot K^2$ and 0.8, respectively.

C. Thermoelectric Material Synthesis

The most common process of material synthesis is to mix elemental raw materials in stoichiometric proportions together and melt them under suitable conditions of temperature and pressure, followed by sintering. Methods such as melt spinning (MS) and mechanical alloying (MA) using ball milling are used to mix the individual ingredients, followed by spark plasma sintering (SPS) or hot pressing to form pellets or disks for characterization. The type of the method used is dependent on the material being synthesized, desired grain size and structure. Other material growth techniques include the Birdgman method for single crystal growth, and molecular beam epitaxy (MBE) and chemical vapor deposition (CVD) for thin film growth. A majority of the material characterization studies deal with bulk samples and use one of the above-mentioned bulk synthesis techniques. Material synthesis also includes controlling process parameters such as material content, process temperature, and the type of sintering. These affect the grain size, orientation, and the formation of nanostructures.

D. Property Optimization

Materials optimization follows from the physics of thermoelectric transport and efficiency laid out in Section II. The focus is generally on lowering k and/or increasing $S^2\sigma$. Optimizing carrier concentration and band engineering to simultaneously increase S and σ are frequently employed to improve $S^2\sigma$ [33]. Doping and alloying lower k by increasing phonon scattering [45], [46]. Another effective technique is to incorporate alloys in the material as nanoinclusions. Nanoinclusions can also increase S at high doping due to the electron scattering on band bending at nanoinclusion–semiconductor interfaces [47]. Synthesis processes such as SPS can be used to introduce charged defects in the material that serve to reduce carrier concentration [48]. The preferential scattering of electrons at charged defect sites can lead to injection of electrons into the bulk resulting in higher bulk electrical conductivity. Defect chemistry can also be used to allow appropriate doping to achieve desired thermoelectric properties [49].

Band structure engineering is a powerful technique used to alter the band gap, create resonant states through band distortion, or achieve band convergence [32], [33]. Band engineering techniques are mainly implemented in lead chalcogenides to improve S and σ. Dopants serve to increase the effective mass leading to large DOS [32]. A large DOS ensures a high S at a given carrier concentration. But dopants can also lower the electron mobility leading to lower σ. Increasing the band gap at high temperatures can reduce the effect of minority carriers degrading S and also reduce the electronic thermal conductivity. Resonant states can increase DOS through an increase in effective mass thereby increasing S [49]. Band convergence can increase S by increasing the band degeneracy of the material.

Material property optimization based on process parameters usually follows a trial-and-error approach by changing the parameters over a chosen range to identify the best combination. The repeatability and reliability of such optimization methods is, however, scarce in the literature.

Table I summarizes details on the various dopants and alloys used for each thermoelectric material and the effect on thermoelectric properties. Table I includes synthesis techniques and optimization methods, as well as general observations regarding the success of these approaches.

IV. Bulk Thermoelectric Device and Its Operation

A typical thermoelectric device consists of multiple pairs of p-type and n-type semiconductor legs shown in Fig. 2, connected in series electrically and in parallel thermally. The legs are connected to each other through metal connectors usually made of copper. As current flows through the device, one side is cooled and the other is heated. We consider a two-leg device for our theoretical analysis, as shown in Fig. 2. Based on the mode of operation, thermoelectric devices can operate as TEGs or TECs. In a TEC, heat flow is facilitated by the current flow through the device.

TECs can be used under two modes of operation: refrigeration and active cooling. Thermoelectric refrigeration, as shown in Fig. 2(a), takes place when heat flows from the cold side to the hot side (typically ambient). In this scenario, Peltier heat flow and Fourier conduction oppose each other which suggests that materials with low thermal conductivity can achieve better refrigeration. In the active cooling mode shown in Fig. 2(b), Peltier heat flow is augmented by Fourier conduction. In Sections IV-A–IV-C, we discuss the differences between the refrigeration and active cooling modes of operation, both at steady state. We then discuss the special case of transient operation.

A. Refrigeration

We consider a p-n thermoelectric module as shown in Fig. 2(a) at steady state. In the case of thermoelectric refrigeration, heat is extracted from the cold side at a constant temperature T_{C} and heat is rejected at the hot side at constant temperature T_{H}. The cooling power of the TE module defined as the heat absorbed at the cold junction, Q_{c} is given by

$$Q_{\mathrm{C}} = SIT_{\mathrm{C}} - \frac{1}{2}I^2R - K\Delta T. \tag{9}$$

Here $S = S_{\mathrm{p}} - S_{\mathrm{n}}$ is the junction Seebeck coefficient, I is the current through the TE module, L_{p} and L_{n} are the lengths, A_{p} and A_{n} are the areas of the p- and n-legs, $R = L_{\mathrm{p}}\rho_{\mathrm{p}}/A_{\mathrm{p}} + L_{\mathrm{n}}\rho_{\mathrm{n}}/A_{\mathrm{n}}$ is the series equivalent electrical resistance, $K = L_{\mathrm{p}}k_{\mathrm{p}}/A_{\mathrm{p}} + L_{\mathrm{n}}k_{\mathrm{n}}/A_{\mathrm{n}}$ is the parallel equivalent thermal conductance, and $\Delta T = T_{\mathrm{H}} - T_{\mathrm{C}}$ is the temperature difference across the TEC module. Since the TE module functions as a heat pump, the performance evaluation metric is its coefficient of performance (COP) which is the ratio of heat absorbed at the cold side to the power input. Hence, the COP is given by

$$\mathrm{COP} = \frac{SIT_{\mathrm{C}} - \frac{1}{2}I^2R - K\Delta T}{SI\Delta T + I^2R}. \tag{10}$$

Both COP and cooling power are dependent on the operating current. The performance of TE module can be optimized

TABLE I
THERMOELECTRIC MATERIAL PROPERTIES REPORTED AT 300 K

Material	Temperature range	S (μV/K)	σ (10^5S/m)	k (W/mK)	ZT	Method of synthesis	Method of improvement of ZT	General comments
Bi_2Te_3 alloys [6]	300 – 400 K	187	1.25	1.1	1.2	Zone melting Melt spinning followed by spark plasma sintering Ball milling followed by hot pressing	Nanostructuring to lower k	Highly anisotropic in nature. Can be p-type or n-type with appropriate doping.
PbTe alloys [31]	600 – 800 K	75	2.4	4.3	0.1	Direct reaction via melting followed by hot pressing Electrochemical deposition Sonochemistry Solvothermal/hydrothermal process	Nanostructuring through nanoinclusions of Ag^+, Na^+, K^+ and Sb^{3+} can lower k through phonon scattering Band engineering to maximize $S^2\sigma$	Widely used in TEGs at high temperatures Easy alloying due to fcc structure
SiGe alloys [137]	600 – 800 K	-92	1.04	4.8	0.1	Chemical vapor deposition for thin films Ball milling followed by hot pressing for bulk samples	Modulation doping to increase mobility Nanostructuring to lower k_L	High k since Si composition is ~ 80% in the alloy General application as TEG
$CoSb_3$ Skutterudites (MX_3: M = Co, Rh, Ir and X = P, As and Sb) [138]	600 - 800 K	-160	1	4.8	0.15	Melt spinning and spark plasma sintering	Increase phonon scattering using filler species such as alkali metals and other ions to reduce k_L	Cage like structure facilitates filling with other species to alter the scattering phenomena.
$Hf_{1-x}Zr_xNiSn_{1-y}Sb_y$ Half Heusler alloys [139]	600 - 1000 K	-138	1.6	1.86	2.2	Levitation melting and spark plasma sintering	Alloy scattering through intermixing of Hf and Zr to lower k_L	
Mg_2Sn Silicides Mg_2X (X = Si, Ge and Sn) [140]	600 - 800 K	-115	2.5	6.5	0.15	Melt spining and spark plasma sintering	Nanostructuring through nanoinclusions and band convergence to lower k	Composed of inexpensive and easily available compounds
SnSe [141]	300 - 700 K	500	1.5	0.7	0.7	Birdgman crystal growth	Hole doping to lower k_L Alloying with Pb, Zn and other compounds Hole doping enhances S and σ through contribution from multiple bands	Highly anisotropic and exhibits better properties preferably along axes with strong SnSe bonding Made using compounds available in abundance
PEDOT:PSS [42]	<300 K	14	0.3	0.34	0.01	Dropcasting, Ploymerization followed by spincoating onto a substrate	σ can be increased using dielectric solvents Inorganic materials such as CNTs and Bi_2Te_3 incorporated into the polymer matrix to increase σ and lower k	Properties can be altered by controlling the amount of oxidation of the polymer solution
GeTe [142]	300 - 800 K	31	7.8	7.2	0.04	Melting in a furnace followed by sintering and hot pressing	Doping/alloying with materials such as Bi_2Te_3, Ag alloyed Sb_2Te_3 to alter carrier concentration	Mainly used for thermoelectric generation at high temperatures

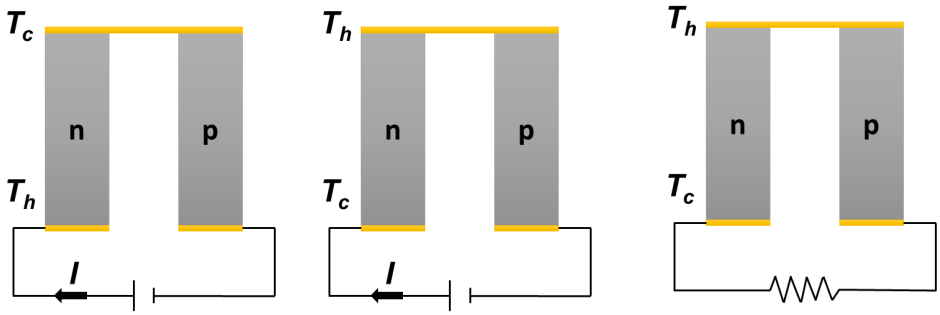

Fig. 2. (a) Thermoelectric refrigeration where the net heat flow is from the cold side and added to the hot side. Peltier heat flow is opposed by Fourier conduction. (b) Active cooling where the net heat flow is from the hot side to the cold side. Peltier heat flow is augmented by Fourier conduction. (c) Thermoelectric generation where the temperature difference results in a net current flow.

either by maximizing the cooling power or the COP depending on the type of application. The optimal current of operation for maximum cooling power is given by $I_{\text{opt}} = ST_c/R$ and the maximum cooling power $Q_{c,\max}$ is given by

$$Q_{C,\max} = \frac{S^2 T_C}{2R} - K\Delta T. \tag{11}$$

We can conclude from (11) that high $S^2\sigma$ and low k are ideal to achieve high cooling power using TEC in the refrigeration mode. Consequently, materials with high ZT at 300 K such as Bi_2Te_3 are preferred in refrigeration applications.

B. Active Cooling

In the case of active cooling, heat must be absorbed from the hot side at a temperature T_H and rejected at the cold side at a temperature T_C which is usually ambient, as shown in Fig. 2(b). The cooling power of the TEC Q_H is defined as the

heat absorbed at the hot side of the TEC and is given by

$$Q_{\mathrm{H}} = SIT_{\mathrm{H}} - \frac{1}{2}I^2R + K\Delta T. \tag{12}$$

In the above expression, $K\Delta T$ is the passive cooling and $ST_{\mathrm{h}}I - I^2R/2$ is the active cooling. We can deduce that Peltier cooling is augmented by Fourier conduction in the case of active cooling as opposed to refrigeration. The performance of the device can again be evaluated from its COP defined as

$$\mathrm{COP} = \frac{SIT_{\mathrm{C}} - \frac{1}{2}I^2R + K\Delta T}{-SI\Delta T + I^2R}. \tag{13}$$

Zebarjadi [50] discussed in detail the key differences in the heat transfer mechanisms of refrigeration and active cooling. In particular, ZT is not an appropriate metric to evaluate thermoelectric materials for active cooling. The maximum cooling power at the hot side is achieved for an operation current of $I = ST_{\mathrm{H}}/R$. By performing a similar analysis, the maximum cooling power $Q_{\mathrm{H,max}}$ and corresponding COP for TEC operating in active cooling mode are obtained as follows:

$$Q_{\mathrm{H,max}} = \frac{S^2T_{\mathrm{H}}}{2R} + K\Delta T \tag{14}$$

$$\mathrm{COP} = \frac{T_{\mathrm{C}}}{2T_{\mathrm{H}}} + \frac{\Delta T}{ZT_{\mathrm{H}}T_{\mathrm{C}}}. \tag{15}$$

From the above expressions, we can conclude that the material used in active cooling should possess high $S^2\sigma$ and high k. Hence, the thermally less conductive thermoelectric materials like Bi_2Te_3 are not ideal for active cooling. Metallic alloys such as Pd-Ag or Cu-Ni [50] or metals like Co that possess high thermopower at 300 K might be suitable for effective heat removal in active cooling [27]. To lend further credence to this idea, active cooling has been recently demonstrated experimentally using Co-$CePd_3$ TE couple where Co and $CePd_3$ are the n-type and the p-type legs, respectively [28]. They evaluated the effective thermal conductivity of the TE module defined as follows:

$$k_{\mathrm{eff}} = k + \frac{S^2\sigma T_{\mathrm{H}}}{\Delta T} \tag{16}$$

to be around 1000 W/mK for a $\Delta T \sim 0.4$ K, which is two orders of magnitude higher than the individual thermal conductivities of Co and $CePd_3$.

C. Transient Operation

Research on transient operation of the TEC mainly focused on understanding the pulse cooling of Peltier cooler using an optimized current pulse in the absence of an active heat load [51]–[55]. Pulse cooling is achieved at small timescales (∼s) when a current pulse with magnitude higher than steady-state optimal current is used, as shown in Fig. 3 [52]. The amount of pulse cooling is shown to depend on the current pulse characteristics and the time constants involved in cooling and recovery of the cold side. Numerical and theoretical models are developed to study the effect of current pulse shape on pulse cooling [54], [56]. Thonhauser *et al.* [54] concluded that having a current pulse in the shape of t^2 improves the refrigeration at the cold side by 8 K. Yang *et al.* [51] studied

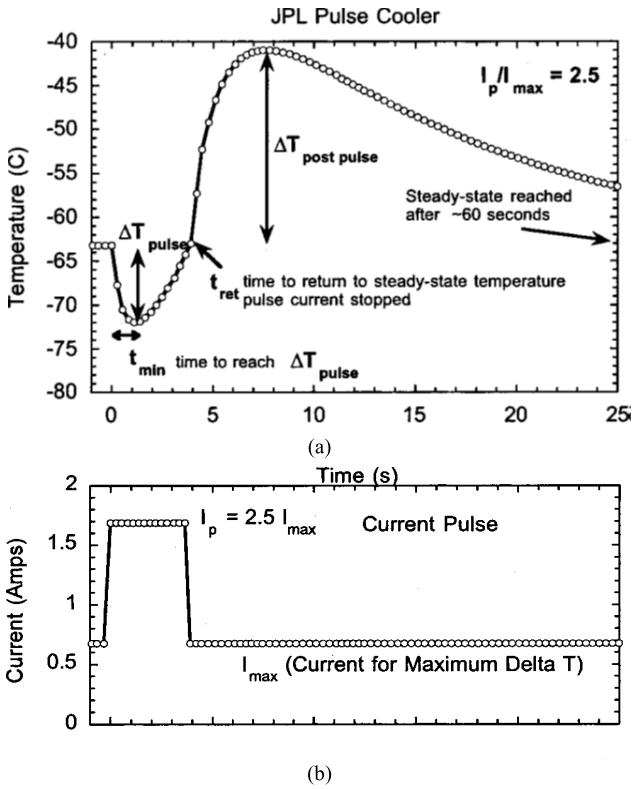

Fig. 3. (a) Pulse cooling obtained at the cold side of TEC using a current pulse with peak current whose amplitude is a multiple of optimum current. (b) Current pulse variation corresponding to the cold side temperature response of the TEC. (Images taken from [46].)

the effect of transient cooling for a TEC with an attached passive load. They determined the effect of length of the TEC, current pulse amplitude and shape, and geometry of the TE element on the cold-side temperature. The time during which pulse cooling is observed is termed as holding time and it increases with increase in TE element length and decrease in current pulse magnitude as Joule heating reduces. The thermal conductivity (k) and volumetric specific heat (C_{P}) of the passive load attached to the TE element affect the cooling observed. Having a passive load of higher k and C_{P} will increase the refrigeration. When working with TEC in transient refrigeration mode, geometric parameters and current parameters should be optimized such that the holding period of the pulse cooling is longer.

Although the abovementioned studies provide useful information about transient operation of TEC, the presence of active heat load will change the analysis in its entirety. The optimal current of TEC operation will become a transient function varying continuously as the temperature distribution across the TEC changes. A recent computational study evaluated the effectiveness of an embedded unipolar TEC for transient active cooling of a hotspot, as shown in Fig. 4(a) [57]. As established in Section IV, active cooling requires thermoelectric materials with high $S^2\sigma$ and high k. This study showed that conventional TEC materials such as Bi_2Te_3 alloys do not provide any cooling advantage due to their intrinsically low thermal conductivities ($k \approx 1.5$ W/mK) compared to that of the native

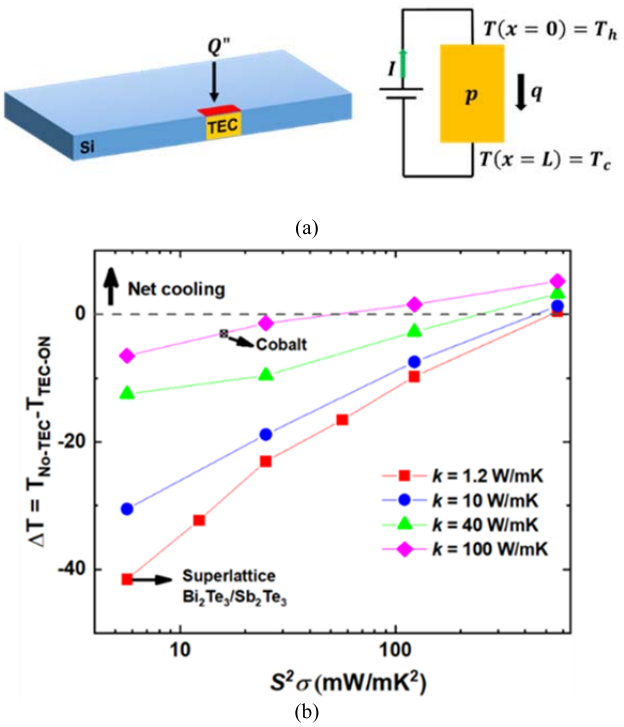

Fig. 4. (a) Geometry of the device used for computational modeling of thermoelectric cooling. TEC is embedded in the silicon chip under the hostpot. Heat flows from the hotspot to the sink. (b) Net cooling obtained at the hotspot due to TEC as a function of thermoelectric PF and thermal conductivity. (Images taken from [57].)

Si substrate ($k \approx 130$ W/mK). Instead, a combination of high $S^2\sigma$ ($\sim$35 mW/mK^2) and k ($\sim$100 W/mK) is required to obtain net cooling at the hotspot, as shown in Fig. 4(b). In order to exceed the diffusive cooling provided by the Si that the Bi_2Te_3 replaces, it would need a much higher $S^2\sigma$ than it possesses. The prospect of using a TEC for hotspot cooling appears to be more appealing in substrates of low thermal conductivity such as sapphire/GaN heterostructure.

V. Thermal Management Using TECs

In this section, we describe the efforts to explore thermoelectric devices for electronics cooling with emphasis on the past two decades, when devices in the size range of a few to a few hundred micrometers gained special prominence. Thermoelectric device cooling, initially proposed by Kraus *et al.* [58], centered around operating electronics at lower than ambient temperatures to increase reliability and switching speeds [58], [59]. Early experiments used TEC modules made of the most common thermoelectric material Bi_2Te_3 [60]–[62]. However, any cooling achieved was insufficient for the large power dissipations typical in logic circuits [62]and spoke to the need for improving material properties [63]. Fukutani and Shakouri [64], demonstrated theoretically using bulk TEC with an integrated circuit to achieve low operating chip temperature under ambient conditions. The cooling provided by the TEC proved effective for heat dissipation densities below 2 W/cm^2. Thermal resistances between the TEC and the heatsink affected the TEC performance drastically. Other factors like heat conduction in adjacent substrates and backside thermal conduction from various thermal pathways also degraded TEC performance considerably. TECs when used in conjunction with other thermal management technologies such as heatsinks showed more promise, by lowering hotspot temperature by as much as $\sim$5 K under steady-state conditions [65]–[67]. However, parasitic Joule heating remained a key bottleneck.

Evolution of semiconductor technology enabled the miniaturization of TECs to open possibilities for on-chip integration. Early work in TEC miniaturization focused on developing thin film fabrication techniques to reduce leg thickness while yielding material properties similar to the bulk. Microcoolers with leg thickness <0.2 mm were also developed using bulk manufacturing methods such as extrusion [68], [69]. Most of the work in thin film TECs (TFTECs) dealt with Bi_2Te_3 and Sb_2Te_3 alloy-based thin films developed using techniques such as coevaporation and electrochemistry [70]–[72]. Experimental studies on TFTECs reported a wide range of maximum cooling (ΔT_{max}) from 1 to 2 K for (Bi, Sb)$_2$Te$_3$ alloy-based thin film devices [71], [72] to 30 K for polycrystalline Bi_2Te_3 alloy-based thin film deposited using a two-wafer process [73]. These values are lower when compared to their bulk counter parts due to the effect of electrical and thermal contact resistances and structural defects.

With the advent of better thin film deposition techniques, usage of superlattice structures in TFTECs gained prominence. Nanostructured films and quantum dot superlattice structures with improved intrinsic ZT are used as p- and n-legs of TFTECs. Using controlled film growth techniques such as MBE and metal organic chemical vapor deposition (MOCVD) reduced contact resistances leading to improved device performance. A ΔT_{max} of $\sim$45 K was reported for a Bi_2Te_3-based superlattice thermoelectric module grown using MOCVD which is attributed to a high intrinsic ZT of $\sim$1.5 and reduced electrical contact resistance [7]. The details about materials used, fabrication methods, and device performance of TFTECs are presented in Table II.

TFTECs have been further explored as a means of reducing electrical resistance to reduce Joule heating losses. Intel reported cooling of $\sim$6 K while pumping heat fluxes in the order of 1000 W/cm^2 with a TFTEC made of p-type Bi_2Te_3/Sb_2Te_3 and n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ superlattices whose test setup is shown in Fig. 5 [74]. In another work, monolithic integration of TECs on a silicon chip offered net cooling of 4–7 K with cooling power density (CPD) ranging between 100 and 680 W/cm^2 [75]. TECs have also been explored in configurations other than the regular p-n couple. Zhang *et al.* [76] used an oversized microcooler chip made of Si/SiGe to remove heat from the hotspot on a silicon substrate. This resulted in the reduction of the hotspot temperature by 3.5 K. The oversizing of the microcooler is, however, not practical when there are multiple hotspots on the substrate. Using the substrate as a TEC and electrically biasing from the center toward the edges of the substrate was shown to reduce the hotspot temperature by $\sim$6 K at an ambient temperature of 373 K [77]. But the rest of the die also heats up due to flow

TABLE II
COOLING PERFORMANCE OF ON-CHIP TECS REPORTED AT OR NEAR ROOM TEMPERATURE

Type of TEC	Material	Device configuration	Fabrication method	Substrate	ΔT_{max} (K)	CPD_{max} (W/cm^2)
Miniaturized TECs		total 18 couples, each 200 × 410 × 410 μm^3	Electroerosion	AlN (650 μm thick)	70.6 at 30 °C 91.8 at 85 °C	80 at 30 °C 98 at 85 °C
	Bi_2Te_3 (Extruded) [68], [69]	total 18 couples, each 130 × 410 × 410 μm^3	Electrochemistry	AlN (650 μm thick)	64.2 at 30 °C 83.5 at 85 °C	110 at 30 °C 132 at 85 °C
	p-leg: bulk $(Bi/Sb)_2Te_3$; n-leg: Bi_2Te_3 NW [143]	p-leg is 130 × 250 × 250 μm^3; n-leg is 50 ×370×370 μm^3	Electrochemistry	-	14.8 at 23°C	-
Alloy based thin film TECs	n^+ GaAs [144]	100 μm thick	Micromachining	n^+ GaAs (monolithic integration)	7.5 at 30 °C	-
	p-Sb_2Te_3;	Film thickness 0.70 μm;	Co-evaporation	Glass	15.5 at 25°C	-
	n- Bi_2Te_3 [70]	diameter 7.0 μm				
	p-$Bi_{2-x}Sb_xTe_3$;	total 63 couples,	Electrochemistry	Oxidized Si (400 μm thick)	2 at 80 °C	-
	n-Bi_2Te_3 [71]	Film thickness 20 μm, diameter 60 μm				
	p-Sb_2Te_3;	total 60 couples,	Co-evaporation	Glass	1 at 25 °C	-
	n-Bi_2Te_3 [72]	Film thickness 4.5 μm, diameter 40 μm				
	p-$(Bi,Sb)_2Te_3$;	Film thickness 10-20 μm	Co-sputtering (two-wafer process)	Si (200 μm)/SiO_2 (0.1-1.0 μm)	48 at 85 °C (Vacuum) 30 at 25 °C (Vacuum)	-
	n-$Bi_2(Se,Te)_3$ [73]					
Superlattice based thin film TECs	n-InGaAs/InGaAsP [81]	Cathode: n+ InGaAs (0.3 μm) Barrier layer: InGaAsP (1 μm) Anode: n+ InGaAs (0.5 μm)	MOCVD	n+ InP (100 μm thick)	1.2 at 25 °C 2.3 at 90 °C	~ 100
	p-Bi_2Te_3/Sb_2Te_3 [5]	10 Å/50 Å p-Bi_2Te_3/Sb_2Te_3 single leg nanostructured superlattice	MOCVD	-	32 at 25 °C 40 at 80 °C	585 at 25 °C 700 at 80 °C
	SiGe/Si [117]	200×(3 nm Si/12 nm $Si_{0.75}Ge_{0.25}$) Film thickness: 3 μm Area varying from 10 × 10 to 150 × 150 μm^2	MBE	Si with a graded buffer layer	4.3 at 25 °C 7.0 at 100 °C 13.8 at 250 °C	598 at25 °C
	SiGeC/Si [79]	3 μm thick SiGeC SL grown on top of Si w/o any buffer layer; 60×60μm^2 device	MBE	Si (500 μm thick)	2.8 at 25 °C 6.9 at 100 °C	680 at 25 °C
	n-leg: n-PbSeTe/PbTe (nanostructured) p-leg: Au ribbon [145]	Film thickness: ~ 100 μm (0.1×10×5 mm^3) Au ribbon: 0.025×0.25×5 mm^3	MBE	BaF2 substrates	43.7 at 27 °C	-
	AlGaAs based SL [87]	100×$Al_{0.10}Ga_{0.90}As/Al_{0.20}Ga_{0.80}As$ with 60 × 60 μm^2 device area	LPMOCVD	n type GaAs	0.8 at 25 °C 2.0 at 100 °C	-
	$In_{0.53}Ga_{0.47}As/ In_{0.52}Al_{0.48}As$ [86]	InGaAs SL film thickness 5 nm. 25 periods, device size varying from 40 × 40 to 120 × 120 μm^2	MBE	n^+ InP (330 μm) with InGaAs buffer layer (0.3 μm)	0.8 at 25 °C	~ 135
	Si/SiGe SL [76]	200×(3 nm Si/12 nm $Si_{0.75}Ge_{0.25}$); 3 μm thick SL thin film with 1 μm SiGeC buffer layer; Device size varying from 50 × 50 μm^2 to 150 × 150 μm^2	MBE	Si chip (65 μm) on a Si substrate (500 μm)	3.5 at 25°C (bare cooler) 0.8 at 80 °C (cooler with chip)	~600 at 25 °C (bare cooler) 110 at 80°C (cooler with chip)
	p-Bi_2Te_3/Sb_2Te_3; n- $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ [74]	Film thickness: 5-8 μm Device size: 0.1 ×3.5×3.5 mm^2	MOCVD	Si Chip on Si Substrate	15 (total) 7.3 (active)	-
	p-leg: Sb_2Te_3/Bi_2Te_3 SL n-leg: n-type δ-doped $Bi_2Te_{3-x}Se_x$ [7]	Film thickness: 8.1 μm Varying contact diameters	MOCVD	-	45.6 at 25 °C	258 at 25 °C
Internal cooling in a p-n diode [94]	$Hg_{0.8}Cd_{0.2}Te$	-	-	-	30 at 25°C	-
	$In_{0.53}Ga_{0.47}As$	-	-	-	4 at 25 °C	-
	InSb	-	-	-	4 at 25°C	-
	GaAs	-	-	-	0.4 at 25 °C	-
	Si	-	-	-	0.02 at 25 °C	-

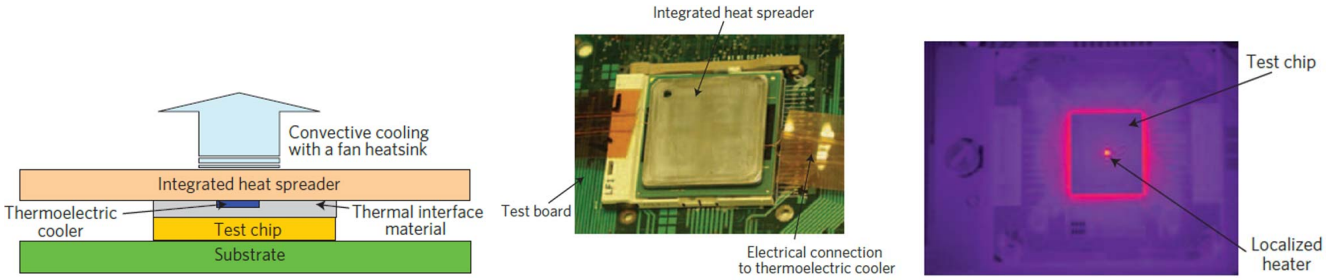

Fig. 5. (a) Cross section of the test package used by Intel to demonstrate thin film thermoelectric cooling. (b) State-of-the-art test package with heaters and temperature sensors. The TEC is attached beneath the spreader. (c) Infrared image showing the formation of a localized hotspot in the absence of a TEC. (Images taken from [68].)

of Joule heat. Thus, using TECs in lateral configuration can provide considerable cooling at the hotspot, but at the expense of creating newer hotspots elsewhere. Beyond oversizing, highly conductive contacts have been explored as a means of improving performance. Yang *et al.* [67] used a 100-μm copper mini-contact between the silicon die and the TEC made of 20-μm-thick Bi_2Te_3 to direct the heat flux from the hotspot toward the TEC. This improved the cooling obtained at the hotspot to ~17 K which is significant. But the individual contribution of the TEC versus the copper contact is not clear.

The impact of thermoelectric cooling in optoelectronic devices is different since even a temperature difference of 1–2 K may affect device performance drastically. In wavelength-division multiplexing (WDM) systems, where optical carrier signals are multiplexed using different wavelengths of laser light, 1–2 K change in temperature can result in a crosstalk between the channels [78]. Heterostructure-integrated thermionic (HIT) microrefrigerators with different superlattice periods, thicknesses, and doping concentrations are specifically studied for this

purpose [79]–[82]. HIT cooler uses thermionic emission in tandem with thermoelectric cooling to provide net cooling in devices. Thermionic emission refers to the emission of hot electrons from cathode to anode through a barrier. Typically, the superlattice structure acts as the barrier layer that allows the selective emission of hot electrons and consequently evaporative cooling at the junction [83]. Multiple studies reported cooling in the range of 0.5–3 K using microcoolers made from InGaAsP and AlGaAs superlattices [84]–[87].

Beyond these demonstrations targeting steady-state cooling, there are limited studies on transient thermoelectric cooling that mainly deal with cooling in the absence of an active heat load. These highlight the importance of short time scales in achieving pulsed cooling using a TEC [51], [52]. In summary, in hotspot cooling using TECs, attention must be paid to the complete heat flow path to ensure that the temperature field in the substrate is not adversely affected. This is particularly important in complex packages such as multichip modules. The heat flow paths in an improperly designed application can create unwanted additional hotspots elsewhere and deep within the device, eventually leading to failure.

VI. Junction-Based Cooling

Distinct from cooling using a dedicated Peltier device, internal thermoelectric cooling refers to the Peltier effect occurring during carrier transport across junctions inside a semiconductor device. For example, in a heterojunction bipolar transistor, cooling takes place when an electron is injected into the base from the emitter. The device geometry and the corresponding band diagrams describing the electron transport for a regular TEC and a junction-based cooler are shown in Fig. 6. Although internal cooling due to the thermoelectric effect is present in almost all active devices, the relative magnitudes vary significantly. A high thermal conductivity semiconductor such as Si does not benefit significantly from internal thermoelectric effects due to competition from Fourier heat conduction, but the effect can be beneficial in lower thermal conductivity semiconductors such as quarternary III–Vs. Despite extensive research for more than a decade, a full understanding of thermoelectric cooling in bipolar devices is still lacking [88]–[91]. In general, the effective $S = (S_p\sigma_p + S_n\sigma_n)/(\sigma_p + \sigma_n)$ is reduced in bipolar transport since S_p and S_n are opposite signs. However, cooling may be enhanced by optimizing the doping, applied bias, and junction width. Device-internal thermoelectric cooling in p-n-junction diodes and laser diodes have been investigated experimentally [92]–[94]. In an insightful experiment, an ultrahigh-vacuum scanning thermoelectric microscopy (SThM) probed the local thermoelectric power of a GaAs p-n-junction ($N_A = 9 \times 10^{18}$ cm^{-3}, $N_D = 1 \times 10^{19}$ cm^{-3}) [95]. For an applied temperature difference of 30 K between the SThM tip and the unbiased sample, the measured thermoelectric voltage showed about $\sim 4\times$ enhancement compared to the bulk within the 2-nm region across the junction. This suggests a higher value of the Peltier coefficient near the junction. The Peltier coefficient in a bipolar device is thus bias-dependent, and not a constant material-dependent parameter. Optimizing the bias-dependent Peltier coefficient shows that in theory, ΔT_{max} in the order of 10 K is achievable at room temperature with $In_{0.53}Ga_{0.47}As$ at a doping level of 10^{19} cm^{-3} [92]. For materials such as $Hg_{0.8}Cd_{0.2}Te$ at a similar doping, a ΔT_{max} in the order of $\sim$ 30 K is theoretically possible at room temperature. However, in materials such as GaAs or Si, ΔT_{max} is predicted to be <1 K even at degenerate doping. This is summarized in Table II. When extending this idea from short-length homojunction p-n diodes to long-length heterojunction diodes, the net effect could be either heating or cooling at the junction depending on the applied bias [96]. In devices where external cooling is not a viable or effective option, such internal cooling with proper optimization presents new opportunity.

Beyond bipolar junctions, the thermoelectric effect can also be utilized for cooling in tunneling junctions. The difference in carrier potential on either side of a thin barrier due to the gradient in temperature causes tunneling of electrons until the current driven by the electrostatic potential balances its thermally driven counterpart. A theoretical value of vacuum tunneling thermopower in the order of 10 μV/K has been reported with similar as well as dissimilar electrodes [97]. Computational predictions based on 1-D tunneling theory estimated a thermopower of 48 μV/K for a generic Al–Al_2O_3–Al junction with a 25-Å barrier thickness [98]. Experimental work on Au-1,4-benzenedithiol (BDT)–Au molecular junction demonstrated a Seebeck coefficient in the order of 10 μV/K [99] which is on the same order of magnitude as predicted theoretically for a double-barrier resonant tunneling structure with 50-Å-thick BDT barrier [100]. S is typically below 30 μV/K in molecular junctions where charge transport is mostly due to the resonant tunneling of the carriers [101], [102]. A recent experiment on molecules between gold (Au) electrodes reported that resonant tunneling increased the Seebeck coefficient beyond 200 μV/K [103]. This is an order of magnitude higher than ungated devices. Theoretical analysis shows that efficiencies close to the Carnot limit are possible near the limit of resonant tunneling. Recent work has targeted enhanced thermoelectric properties in 2-D materials through resonant tunneling [104]–[107]. It is difficult to determine the usability of such tunneling junctions since the field is mostly theoretical at present [108], [109].

VII. Influence of Parasitic Effects

In this section, we focus on parasitic losses encountered during TEC operation and discuss how changes in dimensions are often necessary to mitigate these losses. Electrical and thermal contact resistances encountered in TECs lead to parasitic effects. For example, electrical contact resistance results in additional Joule heat that needs to be removed by the TEC, reducing its cooling potential. Thermal contact resistance increases the internal temperature gradient across the TEC, leading again to reduced cooling. In case of bulk TECs, the contact resistance is usually much smaller than the internal resistance of the TE element and hence can be neglected. But for a thin film module, the magnitude of these contact resistances—both electrical and thermal—can be comparable to that of the TE element. A low contact resistivity, such

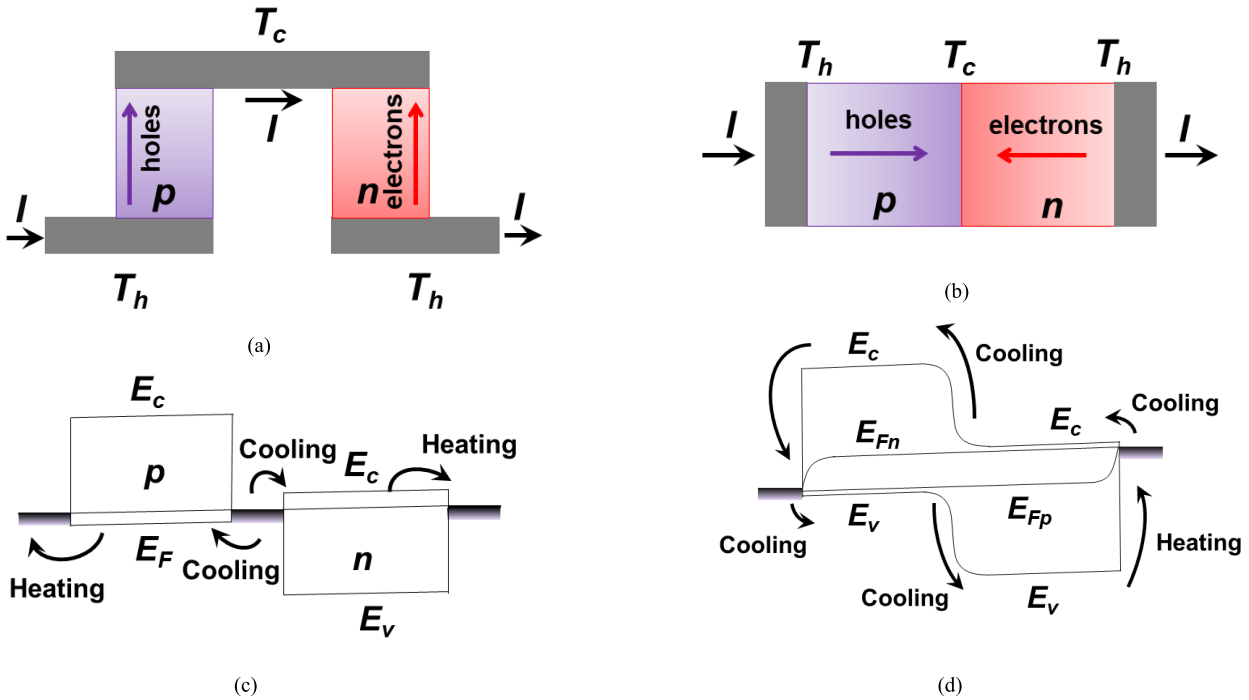

Fig. 6. Device configuration and band structure of (a) and (c) a regular thermoelectric refrigerator and (b) and (d) p-n junction diodes. (Images recreated from [92].)

as between a metal and highly doped Si, is in the order of $10^{-9}\,\Omega\cdot\text{cm}^2$ [110]. In practice, typical figures may be higher, between 10^{-7} and $10^{-5}\,\Omega\cdot\text{cm}^2$ [111]. As an example of the influence of electrical contact resistivity, the optimal film thickness of a TFTEC changes from 20 μm [83], [112] for contact resistivity in the order of $10^{-6}\,\Omega\cdot\text{cm}^2$ to <2 μm when the contact resistivity decreases to $10^{-8}\,\Omega\cdot\text{cm}^2$ [7]. For a 100×100 μm^2 Si/SiGe TEC, an increase in contact resistivity from 10^{-9} to $10^{-4}\,\Omega\cdot\text{cm}^2$ degrades performance by $\sim$85%, whereas the same device scaled to a 3000×3000 μm^2 area would face only a $\sim$5% degradation [111]. Chowdhury *et al.* [74] numerically showed the performance degradation of a nanostructured Bi_2Te_3-based thin-film superlattice cooler due to both the contact resistances. When both the contact resistances were present, almost 40% reduction in $\Delta T_{\max}$ occurred. Their work suggested that the thermal contact resistance dominates over the electrical contact resistance in their TEC. In other studies, electrical contact resistance affects performance more severely [113], [114].

In an ideal TEC, cooling is independent of the cross-sectional area [77]. But in practice, competition between the cooling offered by TEC and heat diffusion from the hotspot to the TEC results in an optimal TEC area [115]. With other factors remaining the same, the optimal current varies in proportion to the area [116]. An increase in contact resistances can be partly offset with an increase in area. The area-dependent cooling performance is prominent at larger current densities [117], [118]. When faced with increased parasitic Joule heating in TFTECs, the film thickness can be further optimized. As an example, the optimum film thickness of Si/SiGe superlattice TFTEC in a packaged IC is in the order of 10 μm [117]. A similar magnitude has been reported for TFTEC monolithically integrated into an InP substrate. With $\sim$10-μm-thick InGaAs/AlGaAs superlattice TEC and contact resistivity in the order of $10^{-8}\,\Omega\cdot\text{cm}^{-2}$, a maximum cooling of 3 K was reported with a 40×40 μm^2 device [86]. This is close to the material's theoretical limit of 4 K, obtained using $\Delta T_{\max}=0.5ZT_C^2$.

VIII. TEC Reliability

TEC modules are, in general, highly reliable components since they are solid-state devices without any moving parts. TECs working with steady-state dc power on a more-or-less continuous basis, have much higher life expectancy compared to those subjected to transient pulses. For on-chip TECs in steady-state operation, mean time to failure (MTTF) is usually greater than 200 000 h, which is considered to be an industry standard [119]. Usually, accelerated life test (ALT) is used to measure the reliability of a TE module under certain cyclic ON/OFF regimes. This method is based on the investigation of the module failure under extreme conditions like high temperatures, mechanical stress, and other effects. There are three ways to carry out the test: 1) accelerating the number of cycles; 2) accelerating the external stress; and 3) strengthening the failure criteria [120]. Depending on the test requirement, one or more ways are incorporated in typical reliability testing of a TEC. There are several parameters that affect the on-chip device reliability which is highly dependent on the device configurations and operating conditions.

A. Thermal Stress

Although thermal stresses are more prominent in TEGs, they can also significantly affect the reliability of Peltier coolers. This may eventually result in dislocations, cracks, or fatigues, and accelerate catastrophic failure of the module. The repeated

thermal cycling can lead to fatigue at the solder junctions and consequently the electric resistance may increase [121]. This unavoidable thermal stress can be minimized with design optimization and carefully choosing the thermal interface material (TIM) and soldering materials.

Interfacial thermal stress due to temperature gradients is the most critical failure mechanism of thermoelectric devices [120]. Although TECs typically do not experience the very high gradients of TEGs, repeated exposure to the temperature gradient can cause excessive thermal stress near the junction [122]. This temperature gradient can be large when the thermal budget is in the order of several hundreds of W/cm^2 and the thickness of the leg is in the order of a few micrometers, such as in TFTECs. A numerical work showed that the peak thermal stress is in the order of 500 MPa (compressive) in a bulk TEC (leg length of 1.5 mm and a thickness of 0.5 mm) at a current of 2 A [123]. With optimization, the same can be reduced to ∼50 MPa. Optimization scheme generally involves optimizing TE parameters like leg length, thicknesses of the barrier layer, metal layer, and solder layer. Studies have suggested thinner and longer legs with compliant interface materials to minimize thermally induced shear stress [124]–[126]. Numerical studies on TFTECs further highlight the impact of dimensions on thermal stresses in miniaturized devices [119]–[122]. Maximum compressive thermal stress of ∼30 MPa has been estimated in a four-layered TFTEC with $T_C = 290$ K and $T_H = 330$ K, comparable to the strength of the thin-film itself [127].

Pulsed thermal load containing high heat flux thermal energy can induce a large thermal stress in the interface of the materials by imposing a high thermal gradient [123]. Recently, Gong *et al.* [128] proposed a finite-element model to analyze transient thermal stress of a conventional TEC module made of 71 pairs of Bi_2Te_3 leg and integrated in a SiC power chip under pulsed thermal loading with varying amplitudes. This study concluded that the pulsed thermal loading drastically increased the thermal stress of the device which led to an abrupt increase in temperature, eventually reducing its cooling performance. For a 30-W pulsed load, the chip temperature fluctuation range was ∼170 °C within a pulse, while the maximum thermal-stress fluctuation range was ∼686 MPa at the chip TEC contact. Increasing the pulse amplitude and duration aggravated the amplitudes of fluctuations. Improved use of transients by controlling the pulsed thermal loading can mitigate the induced thermal stress [129]. An experiment varying a pulsed voltage demonstrated that both the maximum chip temperature and the thermal stress at the contact could be reduced simultaneously. In this case, the maximum stress appears at the cold side contact [128].

B. Mean Time to Failure

When a TEC module undergoes large thermal cycling, it exhibits a significantly lower MTTF than the industry standard minimum limit of 200 000 h [130]. A commercial single-stage ITI Ferrotec Peltier TEC module has MTTF >68 000 cycles when the thermal cycle varies from 30 °C to 100 °C which is greater than MTTF of 50 000 cycles assumed for reliability against thermal cycling [131]. Modules with higher rated operating temperatures offer better life even though the maximum temperature in the thermal cycle is well below the maximum rated temperature. For example, the commercial SuperTEC series module rated to 200 °C has an MTTF of 17 500 cycles, whereas the module rated to 150 °C has an MTTF of 8100 cycles when cycled between −55 °C and 125 °C [132]. When a TEC is powered between ON and OFF using a pulsewidth modulation controller, a significantly lower MTTF is observed compared to the industry standard minimum of 200 000 h. A test conducted with commercial ValueTEC series bulk TEC modules reported an MTTF of ∼125 000 h (3×10^7 ON/OFF cycles) with a cycle every 15 s [119].

IX. Future Prospects for TE Cooling

Fundamental materials research on thermoelectrics in the past two decades, motivated by prospects for waste heat energy conversion, has yielded several breakthroughs in understanding electron and phonon transport phenomena. In particular, increased control over the synthesis of nanostructures, novel measurement techniques, and quantitative improvements in theory have resulted in a dramatic number of reports of higher performance materials. There, however, remains a big gap in translating these laboratory findings to cooling technologies. In fact, device performance rather than cost continues to be the main concern. Since materials research has held emphasis, very little work has been carried out on perfecting electrical and thermal contacts, managing thermal cycling related stresses, and exploring nontraditional device geometries. Issues related to stability of materials, scalability of synthesis, repeatability of measurements, and details of integration remain to be explored.

On the materials side, there continues to be an emphasis on improving Z by reducing thermal conductivity, primarily because the approach has yielded success. Beyond the seminal ideas from the 1990s on altering DOS through nanostructuring, fresh fundamental ideas are needed for improving PFs. Enhancement of the PF is more consequential for cooling applications. In a recent work, we explored the concept of active cooling in managing thermal transients, where the cooling depends on the PF and not Z [57]. The 2-D electron gas (2-DEG) in heterostructures and in atomic layer materials also appears to be promising in this regard. Fundamental considerations show that the PF is intrinsically high in two versus three dimensions. For example, the theoretical PF in single layer MoS_2, for example, peaks at $\sim 2.8 \times 10^4$ μW/mK^2 [133]. Here, graphene may have an advantage due to its high thermal conductivity at room temperature. The PF of graphene can be improved significantly when deposited on a hexagonal boron nitride (hBN) substrate instead of SiO_2 due to the drastic reduction in substrate-induced random potential fluctuations. The reported Seebeck coefficient of ∼182 μV/K (∼twice that measured in graphene on SiO_2) yields a PF $\sim 3.6 \times 10^4$ μW/mK^2 on a ∼10-nm-thick hBN substrate [134]. Lower but more repeatable PFs may be achievable with 2-DEGs in III–V heterostructures [135], [136]. With continued

advances in fabrication of III–V materials for power electronics, more candidate thermoelectric materials will continue to be investigated.

Finally, beyond the conventional Peltier refrigeration, a rethinking on how thermoelectrics can be employed in chip thermal management is also necessary. Does the device need to be restricted to pi-leg bipolar thermocouples or are other configurations suitable? Can the junctions of active semiconductor devices be engineered beyond electrical (switching) performance to also provide internal thermoelectric cooling? Can thin-film integrated TECs be used in close proximity to semiconductor devices to manage peak thermal transients? Can TECs integrated within a multichip module provide cooling in areas or along directions otherwise difficult to access? These are some of the many directions ripe for future explorations.

X. Conclusion

In summary, this article covers thermoelectric cooling, starting from a description of the basic physics and going on to discuss materials and practical demonstrations of chip cooling. In discussing materials, we emphasize the temperature range of 300–400 K of specific interest to electronics cooling. In discussing modes of operation, we point out that cooling should be differentiated from refrigeration and that transient operation requires more careful optimization of the operating current than at steady state. This article also covers the many thin film devices demonstrated to date and their relative performance. Concepts for internal thermoelectric cooling within a semiconductor device either at a bipolar or a tunneling junction are relatively unexplored but are given prominence in this article due to their unique approach. Finally, we discussed reliability issues in TECs. Prospects for future integration of thermoelectric devices in demanding electronic cooling applications such as in microprocessors and high-power devices depend largely on translational work necessary on device engineering and further materials research to demonstrate laboratory gains in the real world.

Acknowledgment

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