Foreword: Special Section on "The Reliability of Advanced Microelectronic Packaging—Part II: Structure–Property Relationships"

MODERN technologies and devices ranging from smartphones, computers, cloud computing, industrial automation, automobiles, to the Internet of Things are enabled by integrated circuits (ICs) and their associated packages. The ICs have evolved from the early small-scale integration (SSI) to the later more complex very-large-scale integration (VLSI) and the subsequent ultra-large-scale integration (ULSI), in a continuous quest for improved functionality, higher performance, smaller form factors, and lower cost. The rate has generally followed Moore's law.

As the shrinking of the critical dimensions of the ICs has become more challenging, the advancement of packaging technologies that focuses on improving the package density to provide cost-effective performance improvements is gaining increased momentum. In the 1990s, a new trend in package miniaturization started. This trend was fueled by the need for "near die-size" type of packages for mobile devices, such as laptops and mobile phones, in order to reduce their form factors and costs. A concept of 3-D integrated circuits (3-D ICs) was put forth by TI researchers Robert Haisty *et al*. in 1964. It involves stacking multiple silicon dice in a single package. Most significantly, it provides the semiconductor industry a new direction to grow. The 3-D ICs have gone through demonstrations in Japan, Europe, and the USA, and have been commercialized since 2004.

The trend of high-density packaging, nonetheless, poses new package reliability issues that must be understood and addressed. The reliability of advanced microelectronic packaging has emerged as the top priority across multiple growth markets for semiconductors, including automotive, industrial, and cloud-based computing. In addition, the reliabilities of mission-critical packages, some of which are for life-saving, need to be very high.

In 3-D ICs, the current densities in microbumps for the interconnection can reach very high due to the small bump diameters. This is aggravated by current crowding at the transition from the metal line to the solder bump, where the current density can be an order of magnitude above that in the bulk of the microbump. Literature shows that a current density level of about 10^3 A/cm^2 can induce significant electromigration that exhibits a polarity effect in Sn-based solder bumps. The solder joint resistance increases due to the formation of voids and intermetallic compounds (IMCs). Excessive IMC growth can compromise the fracture toughness of the solder joint. Similarly, the differences in the coefficients of thermal expansion of materials used in the package can lead to crack initiation and propagation in the solder joint. These issues are exacerbated by Joule heat in the package. While the use of dielectric underfills between Si chips prolongs the solder joint lifetimes, problems such as delamination and corner cracking in the underfill pose additional reliability problems that are challenging.

Although the operating temperatures of most 3-D ICs need to be kept below 105 °C, electronic packages for harsh environments must work at higher temperatures from 150 °C to 500 °C and above. The transient liquid phase (TLP) bond is a solution for some of the high-temperature applications.

In addition to technological aspects of the 3-D ICs, local climate conditions, mainly humidity and particulate contamination, also influence the reliability of the package through the formation of an electrolyte layer on the surface of the printed circuit board assembly (PCBA) that is populated with conducting traces. Similarly, humidity induces a thin electrolyte layer with halogen ions from the molding compound on Cu wire bonding. Corrosion subsequently takes place along the bonding interface that can cause reliability failures. Electrochemical methods have recently been applied to study the corrosion mechanisms and the roles of Pd-addition that underlie the corrosion resistance improvement.

The notion of interconnection in 3-D ICs can be extended to electrical connections in complex electronic equipment, where the contact resistance depends on the microstructures at the contact interfaces. The microstructure evolution under mechanical and thermal stresses can lead to contact resistance increase and eventually (intermittent) failures of the equipment.

Overall, structure–property correlations have been central to materials science, product engineering, and design in general, and specifically to the reliability studies of advanced microelectronic packaging. This second half of the two-part Special Section addresses some of the reliability issues discussed above and significantly advances the state of the art. It contains the following six papers.

1) Park *et al.* present a method to improve the reliability of Cu/Ni/Sn-Ag microbumps by decreasing the solder volume.

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2) Lee *et al*. have studied the interaction between the microstructure evolution during thermal cycling and the long-term reliability of wafer-level chip-scale packages (WLCSPs) with different solder ball interconnects.
3) Nadeesh *et al*. have achieved Ag-Sn TLP bonding as a potential die-attach solution for high-temperature (250 °C) electronic applications.
4) Wu and Lee have presented an electrochemical study of the effects of temperature and Pd concentration on the corrosion behaviors of Pd-doped Cu and Cu_9Al_4 for Cu wire bonding.
5) Piotrowska and Ambat have addressed effects assisting the formation of a water layer on the PCBA surface under transient climatic conditions, which can lead to reliability failures.
6) Li *et al.* have provided a method to test for intermittent faults and assess the reliability of connections in electronic equipment.

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WENTAO QIN, *Editor*
Technology Assessment and Characterization Lab
Quality Department
ON Semiconductor
Phoenix, AZ 85008 USA
wentao.qin@onsemi.com
wentao0108@gmail.com

YAN LI, *Editor*
Corporate Quality Network
Intel Corporation
Chandler, AZ 85226 USA
yan.a.li@intel.com

Wentao Qin (Member, IEEE) received the B.Sc. degree from the University of Science and Technology of China, Hefei, China, in 1992, and the Ph.D. degree from the University of Missouri-Rolla, Rolla, MO, USA, in 2001.

After graduation, he worked as a TEM Engineer with the Semiconductor Sector, Motorola, Mesa, AZ, USA, and ON Semiconductor. For one year, he was a Post-Doctoral Research Fellow with the Center of Fuel Cells and Batteries, Georgia Institute of Technology, Atlanta, GA, USA, in 2009, during which he contributed to six papers in high-impact journals, including *Nature Communication*, *Nano Energy*, *Nano Letters*, and *Energy & Environmental Science*. He is currently a Materials Science/TEM Engineer with the Technology Assessment and Characterization Lab, ON Semiconductor, Phoenix, AZ, USA. He has published over 30 peer-reviewed journal articles and conference papers. He holds one U.S. patent on packaging. His research interests are on the structure–property correlation for materials science in the semiconductor industry, including the applications of thermodynamics and kinetics in solid-state reactions/phase transformations and electrochemistry/corrosion.

Dr. Qin has served as a Technical Committee Member for the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA). He received the Outstanding Paper Award from the International Symposium of Testing and Failure Analysis (ISTFA) in 2015, the subsequent honor of Exchange Paper between the ISTFA and the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) in 2016, and the First Place Awards in the category of False Color Images of the photo contests hosted by the Electronic Device Failure Analysis Society (EDFAS) from 2016 to 2018.

Yan Li received the B.S. and M.S. degrees in physics from Peking University, Beijing, China, in 1996 and 1999, respectively, and the Ph.D. degree in materials science and engineering from Northwestern University, Evanston, IL, USA, in 2006.

She is currently a Senior Staff Package Engineer with the Failure Analysis Lab, Assembly Test and Technology Development, Intel Corporation, Chandler, AZ, USA. As the Lead Package Failure Analysis Engineer of 3-D package technology development projects at Intel, she has been actively involved in numerous packaging-related technical solutions and focusing on the quality and reliability of electronic packages, fundamental understanding of failure modes, and failure mechanisms of electronic packages, and developing new tools and techniques for fault isolation and failure analysis of 3-D electronic packages. She has published over 20 articles and holds two patents in the microelectronic packaging area. She is the co-editor of a book titled *3D Microelectronic Packaging: From Fundamentals to Applications* (Springer), which is highly recognized in the semiconductor industry.

Dr. Li is a Senior Member and a contributor for many international professional associations, such as the Minerals Metals and Materials Society (TMS), the American Society for Metals (ASM), and the EDFAS. She received the TMS EMPMD Young Leader Professional Development Award in 2014. She has been appointed as an Organizer at the TMS and ISTFA Annual Conference since 2011. She has been serving on the Technical Committee of the IPFA since 2018.