Foreword: Special Section on "The Reliability of Advanced Microelectronic Packaging—Part I: Management of Thermal Effects"

MODERN technologies and devices ranging from smartphones, computers, cloud computing, industrial automation, and automobiles to the Internet of Things are enabled by integrated circuits (ICs) and their associated packages. The ICs have evolved from the early small-scale integration (SSI) to the later more complex very-large-scale integration (VLSI) and the subsequent ultra-large-scale integration (ULSI), in a continuous quest for improved functionality, higher performance, smaller form factors, and lower cost. The rate at which metal–oxide–semiconductor field-effect transistors (MOSFETs) counts on a chip have increased has generally followed Moore's law, which states that the transistor count per chip doubles approximately every two years.

As the shrinking of the critical dimensions of the ICs has become more challenging, the advancement of packaging technologies that focuses on improving the package density to provide cost-effective performance improvements is gaining increased momentum. In the 1990s, a new trend in package miniaturization started. This trend was fueled by the need for "near die-size" type of packages for mobile devices such as laptops and mobile phones in order to reduce the form factor and cost. A concept of 3-D integrated circuit (3-D IC) was put forth by TI researchers Robert Haisty *et al*. in 1964. It involves stacking multiple layers of circuitry in a single package. Most significantly, it provides the semiconductor industry a new direction to grow. The 3-D ICs have gone through demonstrations in Japan, Europe, and the USA and have been commercialized since 2004.

The trend of high-density packaging, nonetheless, poses new package performance and reliability issues that must be understood and addressed. The reliability of advanced microelectronic packaging has emerged as the top priority across multiple growth markets for semiconductors, including automotive, industrial, and cloud-based computing. In addition, the reliability of mission-critical packages, some of which are for life-saving, need to be very high.

The power density of Joule heating in a Si device area with 10^7 transistor/cm^2 can reach about 40 W/cm^2 and higher. The high-density characteristic of advanced microelectronic packaging, together with new materials used in the package, can compound Joule heating effects and make the management of thermal effects a formidable task. As a result, the elevation of temperature during the IC/package operation accelerates physical and chemical processes such as electromigration, thermomigration (TM), diffusion, solid-state reaction, and corrosion, all of which can cause reliability failures of the package. Grain boundary and surface scattering of conduction electrons are enhanced, which can cause the degradation of signal integrity. Nonuniform power generation on the chip and increased heat dissipation rates can lead to large temperature gradients, which can increase stresses induced by the thermal mismatch. With a temperature difference of 1 °C across a microbump with a height of 10 μm, the temperature gradient is 1000 °C/cm. The gradient can be too large to be ignored in terms of TM and makes small flip-chip solder joints particularly vulnerable to TM-induced failures. On the other hand, nonetheless, beneficial applications have been derived from the utility of thermal effects. For example, in the assembly of packages, TM has been used to achieve bonding in packaging faster than isothermal treatment. The purpose of this Special Section is to address some of these issues and advance the state of the art.

In this first part of the two-part Special Section, we present the most recent research on advanced microelectronic packaging reliability. Part one of the Special Section contains the following six papers on the thermal effects.

1) Tu and Gusak have presented a unified model of the equations of mean-time-to-failure for TM and stress migration.
2) Jung *et al*. have achieved thermal emission improvement by efficient thermal conduction and warpage mitigation by vertical symmetry and strain distribution, for fan-out package.
3) Liang *et al*. have studied the bending of fine-pitch Cu redistribution layers to improve the electromigration resistance, for fan-out package.
4) Catalano *et al.* have presented a comprehensive comparison of single-sided cooled (SSC) technology and double-sided cooled (DSC) technology that takes into account of electrical performance and mechanical reliability, in addition to heat dissipation.
5) Kumar *et al*. have addressed a matrix rational approximation (MRA) model to predict the impact

Digital Object Identifier 10.1109/TCPMT.2020.3021317

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of temperature and dielectric roughness on the signal integrity of the interconnect networks.

6) Attari and Arróyave have provided a phase-field model of TM for proactive control of the complex heat treatment processes, to speed up the bonding for low-volume solder interconnects.

We are very grateful for the encouragement and assistance provided by Dr. Ravi Mahajan, Managing Editor; Dr. K. Ramakrishna, Senior Area Editor; Denise Manning, Administrator of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY; and Prof. Xuejun Fan, Mechanical Engineering Department, Lamar University, Beaumont, TX, USA.

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Dr. Qin has served as a Technical Committee Member for the IPFA. He received the Outstanding Paper Award from the ISTFA in 2015, the subsequent honor of Exchange Paper between the ISTFA and the European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) in 2016, and the First Place Awards in the category of False Color Images of the photo contests hosted by the Electronic Device Failure Analysis Society (EDFAS) from 2016 to 2018.