

Letters

Significant Die-Shift Reduction and μ LED Integration Based on Die-First Fan-Out Wafer-Level Packaging for Flexible Hybrid Electronics

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Abstract—Typical die shift is beyond several tens micrometers or more, which is a serious problem on advanced fan-out wafer-level packaging (FOWLP), to give inevitable misalignment errors in the subsequent photolithography processes for fine-pitch redistributed wiring layer (RDL) formation. In particular, this problem is expected to grow all the more serious in chiplets and tiny dies less than 1 mm in a side. In this work, the use of an anchoring layer is proposed to fix these dies/chiplets on a double-side laminate thermo-release tape and drastically reduce the die shift. In addition, an on-nail photoplethysmogram (PPG) sensor module as a part of flexible hybrid electronics (FHE) is integrated with μ LED ($270\ \mu\text{m} \times 270\ \mu\text{m}$) based on a die-first FOWLP methodology using a biocompatible polydimethylsiloxane (PDMS) mold resin for real-time monitoring pulse wave and percutaneous oxygen saturation (SpO_2). The repeated bendability of fan-out Au wirings formed on the PDMS and the current–voltage (I – V) behavior of the μ LED before and after die embedment in the PDMS is characterized.

Index Terms—Biosensor, die shift, fan-out wafer-level packaging (FOWLP), flexible hybrid electronics (FHE), micro-LED, polydimethylsiloxane (PDMS).

I. INTRODUCTION

To address a growing demand in mobile phone market, the importance of semiconductor packages fabricated by embedded wafer-level packaging (eWLP) has been increasingly emphasized in recent year. The eWLP technology is categorized into three methodologies: die-first/face-down, die-first/face-up, and die-last [redistributed wiring layer (RDL)-first]/face-down fan-out wafer-level packaging (FOWLP). The die-first/face-down FOWLP has presented for the first time by Infineon/Nagase/Nitto/Yamada [1], [2] in 2006, whereas the RDL-first/face-down has also reported from NEC Electronics Corporation in 2006 [3]. The predecessor of the die-first/face-up

FOWLP called Integrated Fan-Out (InFO) from TSMC has published in 2012 [4].

Die-shift phenomena have been discussed in detail in the late 2000s [5], where the die shift at the outermost dies of wafers are far beyond $100\ \mu\text{m}$, and compared with 700- and 300- μm -thick dies, the die shift of the thicker dies is 8% lower than the other. The use of carrier wafers and preshift techniques diminishes the maximum die shift from 633 to $79\ \mu\text{m}$ [6]. Several groups have described that the die shift can be reduced by using dies with larger surface area [7], strengthening chip placement load and adhesion between dies and temporary adhesives/tapes [8], selecting lower viscosity molding compound materials [7], and lowering compression speed [9]. However, there is a tradeoff between the die shift and die protrusion caused by high die-placement load [10]: they achieve the die shift of $\pm 15\ \mu\text{m}$ at $10\text{-}\mu\text{m}$ die protrusion. The die shift is also dependent on wafer warpages and each process condition mainly including their temperatures [11]. Ling *et al.* [12] have mentioned that 85% of die shift is resulted from thermal and mechanical (TM) effects such as Young's moduli and coefficient of thermal expansion (CTE) mismatches between the molds and carrier wafers, whereas the rest 15% is due to fluidic forces (FF) such as a shear force. The TM-induced die shift can be lessened through increasing the die pitch/thickness [9] and decreasing the mold compound thickness [9]. In contrast, the FF-induced die shift can be lowered through decreasing the mold compound thickness [9]. In addition, the impacts of carrier CTE [13] and mold compound characteristics (granular/liquid/sheet) [14], [15] on the die shift have been studied so far, but the dominant factors are very complicated.

A structurally new flexible hybrid electronics (FHE) has been developed based on die-first/face-down FOWLP technology [16] with dielets using polydimethylsiloxane (PDMS) that has a low Young's modulus like rubber and is curable at a low temperature even at room temperature. The die-shift assessment has been given by University of California, Los Angeles (UCLA) [17] where the die shift is estimated to be $<6\ \mu\text{m}$. We believe that the curing shrinkage of mold compounds is independent on the die shift when molding with PDMS through additive polymerization because the curing shrinkage of the PDMS is approximately 1% or less. In this study, we employ a vapor-deposition polymer as an anchoring layer to fix dies/chiplets on a thermally releasable temporary tape prior to PDMS casting. The effectiveness of the anchoring layer is demonstrated, and an on-nail photoplethysmogram (PPG) sensor module is integrated by the die-first/face-down flexible FOWLP technology. Fig. 1 schematically shows the on-nail PPG sensor FHE system that is placed underneath a 3-D-printed nail chip called OpenNail (Toshiba Digital Solutions Corporation) and worn with a detachable glue on a fingernail. The

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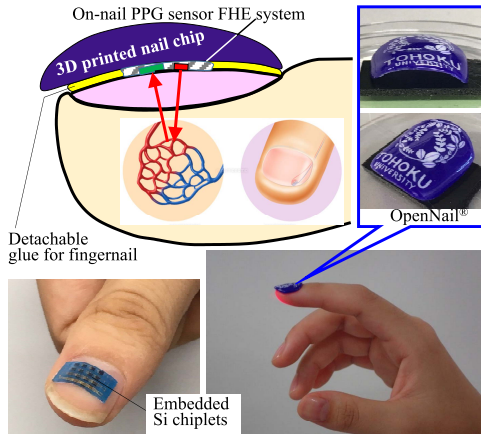


Fig. 1. Conceptual schematic of an on-nail PPG sensor FHE system with embedded μ LED and chiplets consisting of LED drivers and photodiodes.

tailor-made nail chips are designed to fit their own nail curves with various curvature radii with a 3-D scanner.

II. EXPERIMENTAL

A. Materials and Components

A biocompatible PDMS “Silastic MDX4-4210 (Dow)” was used in this work. Rivalpha 3195M and 31950E used as the first and second double-side laminate thermo-release tapes were kindly supplied from Nitto Denko Corporation. The large-scale integrated (LSI) chips (2.5-mm/2.5-mm/400- μ m width/length/height: $W/L/H$) of a PPG sensor consisting of LED drivers, photodiodes, and PPG recording circuits were fabricated using a 1-poly 5-metal 180-nm-node CMOS technology in the Rohm foundry shuttle service. A red μ LED LA DR11HP1 (270- μ m/270- μ m/270- μ m $W/L/H$) and near-infrared (IR) μ LED LA NI14HP1 (340- μ m/340- μ m/270- μ m $W/L/H$) were purchased from Light Avenue GmbH. A 0402/1005 capacitor die JMK105BJ105KV-F (1000- μ m/500- μ m/500- μ m $W/L/H$) was purchased from Taiyo Yuden Company, Ltd.

B. Measurement

The bendability of the RDL formed on the PDMS with embedded dies is evaluated with an endurance testing system: tension-free U-shape folding tester (DLDMLH-FS/Yuasa).

C. Fabrication

Fig. 2(a) shows the process flow of a PPG sensor module based on die-first/face-down FOWLP. A thermally releasable temporary tape Revalpha 3195M was laminated on the first Si carrier with the pressure sensitive side facing downward. Then, a 2.5-mm-square LSI chip, two μ LEDs (red/near-IR), and a capacitor were precisely aligned in a face-down configuration on the tape with a die-to-wafer assembly tool Fineplacer Rambda (Finetech GmbH & Company). Prior to compression molding, a thin Parylene-C as an anchoring layer with a thickness of 1 μ m was conformably vapor-deposited with a parylene coater (Specialty Coating Systems, PDS 2010). After that, a biomedical grade PDMS was poured on the die-on-wafer structure, followed by vacuum defoaming with a vacuum level of around 10 kPa from the highly viscous PDMS sandwiched with the second Si carrier for 30 min. The second carrier has another double-side thermo-release tape 31950E. The subsequent compression mold with the second carrier was performed with a compression force of 0.7 MPa. The first carrier was then thermally debonded at 130 $^{\circ}$ C for 2 min, and subsequently, these tiny dies were transferred to the second carrier. Prior to the following metallization processes, a thin stress buffer layer(s) (SBL) of Parylene-C again and a spin-on planarization

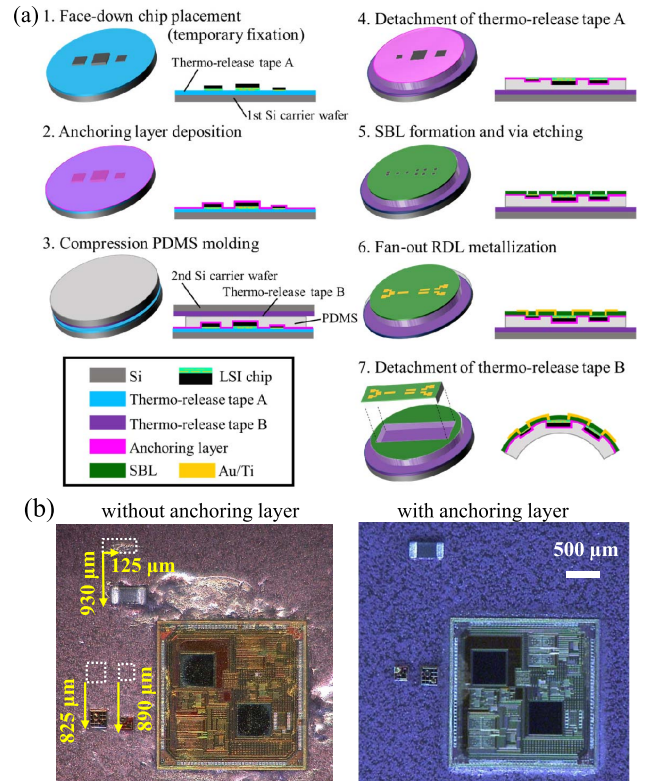


Fig. 2. (a) Process flow for die-first flexible FOWLP using an anchoring layer. (b) Die-shift measurement results from photomicrographs for two μ LEDs, a capacitor, and an LSI chip embedded in PDMS.

layer NPR-90/305B (Showa Denko K.K.) or a diluted biomedical grade flexible epoxy EPO-TEK MED-301-2FL (Epoxy Technology, Inc.) were sequentially formed on the PDMS/dies. By using standard photolithography processes with a physical vapor deposition (PVD) technique, 15-nm-thick Ti as an adhesion layer and 500-nm-thick Au were deposited on the SBL and tiny dies embedded in the PDMS at the wafer-level. The resulting Au interconnects were formed by Au wet etching with Aurum 309 (Kanto Chemical Company, Inc.) for 4 min and Ti wet etching with 1% hydrogen fluoride for 1 min. Finally, the PPG sensor module was debonded from the second carrier.

III. CHARACTERIZATION

A. Die-Shift Evaluation

The die-shift values were measured by a digital microscope VHX-900 (Keyence) after compression molding with the PDMS. Although the PDMS can be fully cured at room temperature for 24 h, the curing conditions at 90 $^{\circ}$ C for 30 min are employed in this study. The viscosity of the PDMS precursor is 60 Pa·s that is approximately two or three orders of magnitude lower than typical rigid epoxy mold compounds (EMCs). IMEC has suggested that a new temporary adhesive BrewerBOND C1301 having a low Young’s modulus similar to the PDMS can lower the die shift [18]. In addition, we measure the die-shift values with a distance of around 20 mm from the wafer center. As shown in Fig. 2(b), however, the die shift in x - and y -axes are 125 and 930 μ m, respectively, even when the capacitor (1 mm \times 500 μ m) was used. The red and near-IR μ LEDs with a side of around 300 μ m show the die shift of 800 μ m or more. This is because the adhesion strength between the tiny dies and thermo-release tape (bonding force: 0.215 N/mm) is extremely low. There would be two reasons why the large die shift is derived: one is due to the large fluidic flow, leading to large shear forces

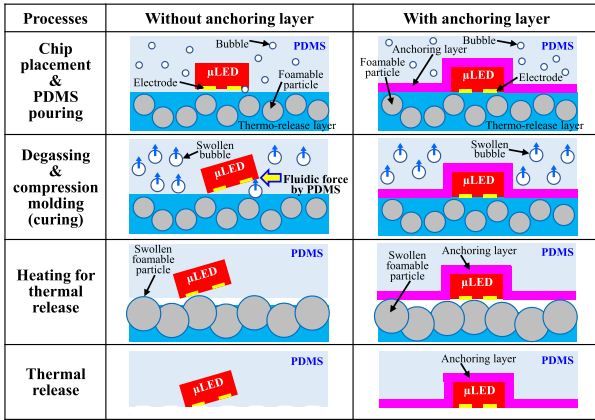


Fig. 3. Mechanism of die shift occurred in flexible FOWLP with PDMS compared to compression molding with and without an anchoring layer.

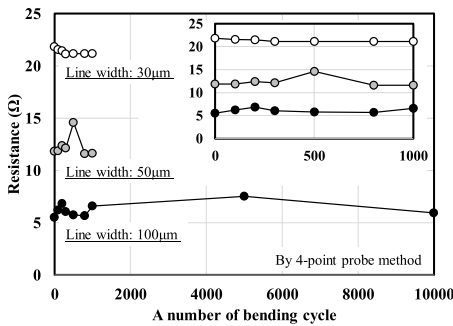


Fig. 4. Results of cyclic bendability test of fan-out RDLs with an Au wire width of 30, 50, and 100 μm (bending radius: 10 mm, bending speed: 50 r/min).

applied to the chip sidewall, especially for the thick capacitor die. Additionally, there are no bulwark surrounding the capacitor die. The two μ LEDs shift along the sidewall of the LSI chip as shown in Fig. 2(b). The other is attributed to bubbling when degassing from the viscous PDMS and the interface between the dies and tape in vacuum. The mechanism of the die-shift reduction is schematically illustrated in Fig. 3. In contrast, as shown in the right of Figs. 2(b) and 3, the parylene anchoring layer gives a significant impact on the die shift. Since the die-shift problem is drastically improved within 5 μm , the subsequent photolithography step allows the precise mask alignment process acceptable to RDL formation.

B. Bendability

In general, the curvature radii of the human fingernail are 13.2 mm for adult males and 10.4 mm for adult females [19]. Thus, the bending test was performed with a curvature radius of 10 mm in this study. We have previously suggested that the SBL contributes to high bendability because the SBL can mitigate wire stresses derived from the TM rapid/large deformation of the PDMS elastomer. Therefore, the SBL having a relatively hard Young's modulus ranging from 2 to 3 GPa exhibits higher toughness than that having a lower Young's modulus below 1 GPa [20]. Here, the spin-on hard polyurethane NPR-90/305B (2.3 GPa) is employed as a planarization layer to compensate the die protrusion of within 5 μm in addition to the Parylene-C (2.9 GPa) SBL layer. As shown in Fig. 4, the repeated bendability beyond 10 000 cycles is obtained when the thin Au wires with a width of 100 μm are used. The resistance change is found to be within 5% after 10 000-cycle bending. Au wires of 30- and 50- μm -width are still connected till 1000-cycle bending, but these wires are disconnected after 5000 cycles. On the basis of the design

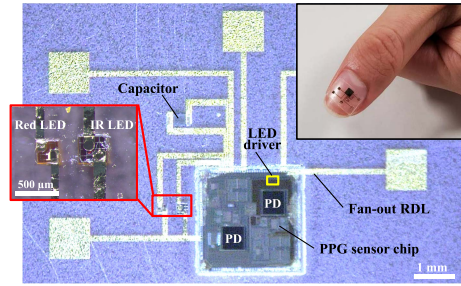


Fig. 5. Photomicrograph of an on-nail PPG sensor FHE system with an embedded red μ LEDs, near-IR μ LED, capacitor, and LSI chip interconnected with fan-out Au wires formed on SBL/PDMS.

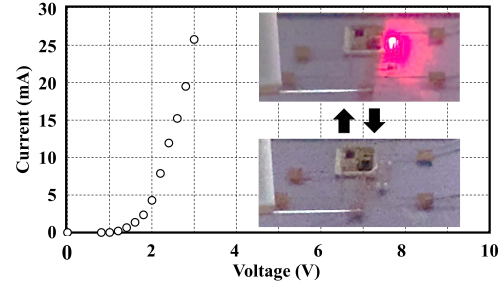


Fig. 6. I - V characteristics of the red μ LED after die embedment and RDL formation and the ON/OFF switch of red light emission driven by the LED driver integrated on the LSI chip.

concept of the on-nail PPG sensor, this FHE module does not have to endure the 10 000-cycle bending. The comprehensive study on high-reliable structural optimization including surface coverlay protection and neutral plane design is ongoing.

C. μ LED Integration

After RDL formation with parylene/MED-301-2FL (2/3- μm) as a SBL/planarization double layer, 100- μm -width fan-out Au wires are successfully interconnected between the embedded LSI chip and two μ LEDs through the capacitor die as shown in Fig. 5. As shown in the I - V characteristics (see Fig. 6), the embedded μ LED can be well operated through the fan-out RDLs. The inset photographs show that the red light emission can be controlled by the LED driver integrated in the LSI chip. This on-chip PPG sensor FHE system can be mounted on a thumbnail. However, any wearable batteries are not yet integrated in this system. The LSI chip can be driven by a voltage of 1.8 V and the maximum consumption current is 20 mA including the μ LED driver and PPG recording circuits. Since the pulse wave monitoring is turned on and off by a clock signal with 33.3% duty cycle, this system is designed to be driven only in one-third of one clock period. Thus, the wearable system can be capable of providing over 3 h of continuous operation even with the thin-film secondary battery having a nominal capacity of 20 mAh, for example. Nevertheless, pulse wave will not be monitored ceaselessly in a real scenario, which means that the system can be stably used for a longer time. Furthermore, the basic operation of the PPG recording circuits have been evaluated on a board in reflection and transmission modes to detect pulse wave from a fingernail [21]. The fully integrated on-chip PPG sensor FHE system with a rechargeable thin-film battery will be fabricated and characterized in near future.

IV. CONCLUSION

Drastic die-shift reduction with an anchoring layer of a vapor-deposited parylene was demonstrated even when 270- μm -square tiny dies were temporarily fixed on a thermo-release tape. In addition to PVD-based materials including inorganic thin films, simple

spin/spray-on anchoring layers would be applicable to this additional die-shift reduction process, depending on the mechanical film strength and adhesion to temporary adhesives although intermixing between the anchoring layers and the adhesives should be taken into account. Two red/near-IR μ LEDs and a capacitor die were embedded in a PDMS and integrated with an LSI chip mainly consisting of LED drivers and photodiodes. These functional blocks can be further divided into small chiplets, which will give more flexibility to the wearable FHE systems. The resulting fan-out Au RDLs formed on the PDMS drove the embedded red μ LED by the LED driver in the embedded LSI chip through the capacitor. This die-first/face-down FOWLP technology can realize high-density fan-out RDL formation on flexible resins and biomedical FHE fabrication without thermal compression bonding with solder microbumps.

REFERENCES

- [1] M. Brunnbauer *et al.*, "An embedded device technology based on a molded reconfigured wafer," in *Proc. 56th Electron. Compon. Technol. Conf.*, May/Jun. 2006, pp. 547–551.
- [2] T. Meyer, G. Ofner, S. Bradl, M. Brunnbauer, and R. Hagen, "Embedded wafer level ball grid array (eWLB)," in *Proc. 10th Electron. Packag. Technol. Conf.*, Dec. 2008, pp. 1–5.
- [3] Y. Kurita *et al.*, "A novel 'SMAFTI' package for inter-chip wide-band data transfer," in *Proc. 56th Electron. Compon. Technol. Conf.*, May/Jun. 2006, pp. 289–297.
- [4] C. C. Liu *et al.*, "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," in *IEDM Tech. Dig.*, Dec. 2012, pp. 323–326.
- [5] C. Houe Khong *et al.*, "A novel method to predict die shift during compression molding in embedded wafer level package," in *Proc. 59th Electron. Compon. Technol. Conf.*, May 2009, pp. 535–541.
- [6] G. Sharma, A. Kumar, V. S. Rao, S. W. Ho, and V. Kripesh, "Solutions strategies for die shift problem in wafer level compression molding," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 4, pp. 502–509, Apr. 2011.
- [7] L. Bu, S. Ho, S. D. Velez, T. Chai, and X. Zhang, "Investigation on die shift issues in the 12-in wafer-level compression molding process," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1647–1653, Oct. 2013.
- [8] J. Mazuir *et al.*, "Evaluation and optimization of die-shift in embedded wafer-level packaging by enhancing the adhesion strength of silicon chips to carrier wafer," in *Proc. IEEE 13th Electron. Packag. Technol. Conf.*, Dec. 2011, pp. 747–751.
- [9] H.-C. Cheng, C.-H. Chung, and W.-H. Chen, "Die shift assessment of reconstituted wafer for fan-out wafer-level packaging," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 1, pp. 136–145, Mar. 2020.
- [10] S. S. B. Lim, S. C. Chong, L. P. S. Sharon, W. W. Seit, and X. Zhang, "Comprehensive study on die shift and die protrusion issues during molding process of mold-1st FOWLP," in *Proc. IEEE 20th Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2018, pp. 201–205.
- [11] C.-Y. Yang, Y.-C. Liu, K.-S. Chen, T.-S. Yang, Y.-C. Wang, and S.-S. Lee, "Process emulation for predicting die shift and wafer warpage in wafer reconstitution," in *Proc. 18th Int. Conf. Electron. Packag. Technol. (ICEPT)*, Aug. 2017, pp. 215–220.
- [12] H. S. Ling, B. Lin, C. S. Choong, S. D. Velez, C. T. Chong, and X. Zhang, "Comprehensive study on the interactions of multiple die shift mechanisms during wafer level molding of multichip-embedded wafer level packages," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 6, pp. 1090–1098, Jun. 2014.
- [13] Y. Han, M. Z. Ding, B. Lin, and C. S. Choong, "Comprehensive investigation of die shift in compression molding process for 12 inch fan-out wafer level packaging," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, May 2016, pp. 1605–1610.
- [14] T. Braun *et al.*, "Panel level packaging—A view along the process chain," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 70–78.
- [15] M. Fowler, J. P. Massey, T. Braun, S. Voges, R. Gernhardt, and M. Wohrmann, "Investigation and methods using various release and thermoplastic bonding materials to reduce die shift and wafer warpage for eWLB chip-first processes," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 363–369.
- [16] T. Fukushima, A. Alam, A. Hanna, S. C. Jangam, A. A. Bajwa, and S. S. Iyer, "Flexible hybrid electronics technology using die-first FOWLP for high-performance and scalable heterogeneous system integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 10, pp. 1738–1746, Oct. 2018.
- [17] A. Hanna *et al.*, "Extremely flexible (1 mm bending radius) biocompatible heterogeneous fan-out wafer-level platform with the lowest reported die-shift ($<6 \mu\text{m}$) and reliable flexible Cu-based interconnects," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 1505–1511.
- [18] A. Podpod *et al.*, "Novel temporary bonding and debonding solutions enabling an ultrahigh interconnect density Fo-Wlp structure assembly with quasi-zero die shift," in *Proc. Int. Wafer Level Packag. Conf. (IWLPC)*, Oct. 2019, pp. 1–6.
- [19] S. Murdan, "Transverse fingernail curvature in adults: A quantitative evaluation and the influence of gender, age, and hand size and dominance," *Int. J. Cosmetic Sci.*, vol. 33, no. 6, pp. 509–513, Dec. 2011, doi: [10.1111/j.1468-2494.2011.00663.x](https://doi.org/10.1111/j.1468-2494.2011.00663.x).
- [20] Y. Susumago *et al.*, "Mechanical and electrical characterization of FOWLP-based flexible hybrid electronics (FHE) for biomedical sensor application," in *Proc. IEEE 69th Electron. Compon. Technol. Conf. (ECTC)*, May 2019, pp. 264–269.
- [21] Z. Qian *et al.*, "Development of integrated photoplethysmographic recording circuit for trans-nail pulse-wave monitoring system," *Jpn. J. Appl. Phys.*, vol. 57, no. 6, Mar. 2018, Art. no. 04FM11.