Process Modules for High-Density Interconnects in Panel-Level Packaging

Friedrich-Leonhard Schein, Ruben Kahle, Marc Kunz, Tim Kunz, Jordan Kossev, Tobias Müller, Mathias Pentz, Michael Dietterle, and Andreas Ostmann

***Abstract*— Advanced packaging technologies like wafer-level fan-out and 3-D system-in-package (3-D SIP) are rapidly penetrating the market of electronic components. For cost reduction, one approach is the migration of processes from wafer to panel format, called panel-level packaging (PLP). In a consortium of partners from industry and research, advanced technologies for PLP are developed. The project aims for an integrated process flow for 3-D SIPs with chips embedded into an organic laminate matrix. At first, 6 mm × 6 mm chips (100 μm thickness) with Cu bumps (25-μm height, 110-μm pitch) are placed into cavities of a printed circuit board (PCB) core layer. They are embedded by vacuum lamination of thin organic films. The core is equipped with fiducials for local alignment and provides handling robustness. Developments aim for a final panel size of 600 mm × 600 mm (here 227 mm × 305 mm demonstrated). Onto the contact side of embedded chips, a 25-μm dielectric film is applied. The copper bumps are subsequently opened by plasma etching. By sputtering and electroplating of Cu, electrical contacts to the chips are formed without via opening. High-aspect-ratio vias as an element for vertical interconnects are formed by UV laser drilling. At via diameters of 17 μm, a drill hole depth of 74 μm was achieved (aspect ratio 4.4:1). Using a newly developed electrolyte, microvia filling was achieved for aspect ratios up to 4:1. With a newly developed direct imaging (DI) machine, 4-μm structures in a 7-μm dry film photoresist are formed. Adaptive imaging of a redistribution layer was realized.**

***Index Terms*— Adaptive imaging, embedding, laser direct imaging (LDI), panel-level packaging (PLP).**

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F.-L. Schein was with the Felix Bloch Institute for Solid State Physics, University of Leipzig, 04109 Leipzig, Germany. He is now with the Faculty of Electrical Engineering and Computer Science, Technical University of Berlin, 13355 Berlin, Germany (e-mail: f.schein@tu-berlin.de).

R. Kahle and A. Ostmann are with the Fraunhofer Institute for Reliability and Microintegration (IZM), 13355 Berlin, Germany (e-mail: ruben.kahle@izm.fraunhofer.de; andreas.ostmann@izm.fraunhofer.de).

M. Kunz and T. Kunz are with Schmoll Maschinen GmbH, 63322 Rödermark, Germany (e-mail: marc.kunz@schmoll-maschinen.de; tim.kunz@schmoll-maschinen.de).

J. Kossev and T. Müller are with CREAVAC Creative Vakuumbeschichtung GmbH, 01159 Dresden, Germany (e-mail: kossev@creavac.de; mueller@creavac.de).

M. Pentz and M. Dietterle are with Dr.-Ing. Max Schlötter GmbH & Co. KG, 73312 Geislingen, Germany (e-mail: pentz@schloetter.de; dietterle@schloetter.de).

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I. Introduction

Advanced packaging technologies like fan-out wafer-level packaging (FOWLP) and 3-D system-in-packages (3-D SIPs) are rapidly penetrating the market of electronic components [1], [2]. Different variations of FOWLP technologies exist today like "face-up," "face-down," and "redistribution layer (RDL) first" [3]. The so-called FO panel-level packaging (FOPLP) is a recently considered approach to reduce costs by pushing the FO technologies further to large manufacturing formats [4]. Primary goal for the movement of FO technology from wafer level to panel level is cost saving by an enlarged manufacturing size. However, this upscaling from round 300 mm formats manufactured with semiconductor style materials and machines to panels of 500–600 mm^2 bears a lot of challenges, for technology as well as for yield/cost [5]. However, by merging technologies from wafer and printed circuit board (PCB) manufacturing also chances are offered to introduce new concepts and ideas.

One novel approach for PLP is investigated in a public-funded project consortium of partners from German industry and research [6], [7]. The project aims for an alternative process flow for 3-D SIPs with chips embedded into an organic laminate matrix, manufactured on large panels up to 600 × 600 mm^2 size. In the following sections, the process concept and the current status of single process step development will be described.

II. Process Concept

The flow of the PLP process is shown in Fig. 1. It has two main features given as follows.

1) A glass fiber-reinforced PCB core surrounding the embedded chips, giving excellent handling stability, and enabling additional fabrication features.
2) Tall Cu bumps (or pillars) on the chip, penetrating the RDL dielectric to avoid via formation (laser, plasma, or photo) and with that increase yield.

In terms of existing WL or PL FO technologies [8], [9], this approach can be categorized as "face-down" process. The process chain consists of the following steps.

A. Core Manufacturing

Starting point is a thin double-sided copper-clad PCB core, preferably with a low coefficient of thermal expansion (CTE) and high glass transition temperature Tg. By photolithography, the fiducial positions are defined and structured by etching the

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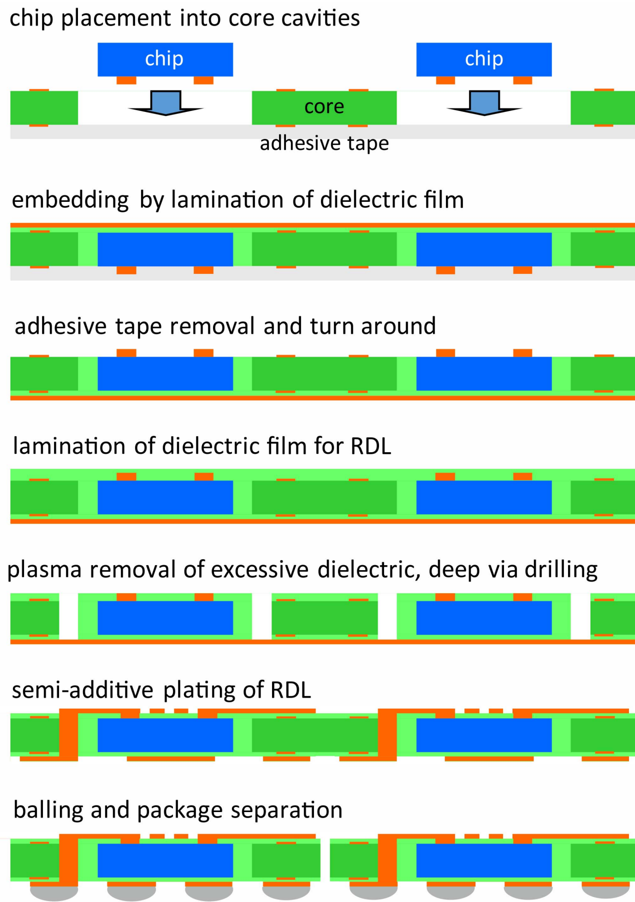


Fig. 1. Concept of process flow.

Cu of the PCB core with subsequent resist stripping. Then, with laser cutting, cavities are created for later die placement.

B. Die Placement

A single-sided adhesive tape is attached to the core backside. Thus, the cavities are equipped with a sticky bottom for die tacking and no additional carrier is needed. In a placement machine, dies with Cu bumps of 10–25 μm height (depending on RDL dielectric thickness) are placed face-down into the cavities, using core fiducials for alignment.

C. Embedding

By vacuum lamination (standard PCB process), a dielectric film is applied to the backside of the core/die construct. Here the build-up material fully fills the gap between chips and core. In the same process, a Cu foil can also be attached. Then, the adhesive tape is peeled off and the panel is turned around. Next, a dielectric is laminated onto the frontside of dies, bumps are exposed, and its positions are measured.

D. Deep via Formation

Optionally (for stackable packages) through-module vias around the chips can be formed by laser drilling. These deep vias with high aspect ratio will be filled with Cu during the following process action.

E. RDL Processing

The RDL is formed in a semiadditive process (SAP). At first, a barrier and seed metal are deposited by sputtering Ti or TiW (typically 100 nm) and Cu (100–300 nm). Then, a dry film photoresist (thickness of 7–25 μm) is applied in a vacuum applicator. The RDL pattern is then exposed to the resist by laser direct imaging (LDI). The LDI technique enables local shrink and stretch of the images by adaptation to local fiducials. Then, the resist is developed and Cu structures are plated. Finally, the resist is stripped, and barrier metal and Cu seed layer are etched.

F. Backend Processing

For the required number of layers, the RDL processing can be repeated. Eventually, a solder mask is applied and contact pads are coated with a surface finish, and solder balls (in case of a ball grid array (BGA)-type package) are applied. The individual packages are then separated by laser or dicing saw. The advantages of this approach are as follows.

1) Local fiducials on any location of the core can be used for die placement and adaptive imaging of the RDL pattern.
2) Since the PCB polymer is already cured before die embedding, it will only have a limited shrinkage.
3) The core cavities limit local die shift and rotation after placement.
4) The PCB core gives significant robustness in handling.

In future developments, further features can be included, such as the following.

1) Premanufactured through-vias and conductors in the core.
2) Adaption of physical properties (such as CTE, stiffness, thermal conductivity, and dielectric constant) by using alternative materials than PCB-laminates (such as metal, glass, and thermoplastics).
3) The PCB core can be equipped with (pre-)embedded components like thin blocking capacitors.

III. Process Steps

In the current phase of the project, the complete process flow and single process steps are developed and optimized separately and in parallel. Since not every machinery or equipment is available at one place, some of the single process steps are developed beyond the actual application case. This section will describe parts of this work. All evaluations were performed on an experimental panel size of 305 mm $\times$ 227 mm. The process until chip embedding was also carried out with a format of 510 mm $\times$ 515 mm.

A. Embedding

For the embedding evaluations, test chips with 6 $\times$ 6 mm^2 size and 100 μm thickness were used. They had peripheral Cu bumps of 60-μm diameter and 110-μm pitch and a thickness of 25 μm. Package and chip design are depicted in Fig. 2. The dummy chips were manufactured with inhouse equipment (semiadditive processing of Cu bumps and no

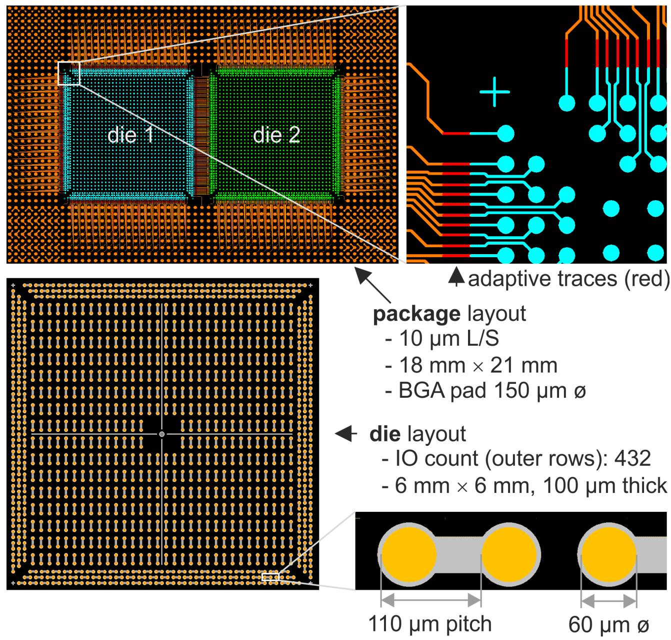


Fig. 2. Package and chip design.

back end of line). Dicing and grinding were carried out by an external company. As PCB core, a low CTE material with 100-μm thickness and double-sided Cu from Hitachi Chemicals was used (E770G). It has Tg $>$ 260 °C, a CTE xy of 4–6 ppm/K, and a CTE z of 8–13 ppm/K. Next, fiducials for die placement and RDL formation were defined by LDI and subtractive etching of the Cu layers. Since the core extents after Cu etching, linear compensation factors were used for resist exposure.

Then, holes for the chips were cut by IR laser (wavelength 1060 nm). The size of holes varied, leaving gaps of 45 or 75 μm between chips and cavity walls. Tests have shown a reproducibility of hole geometries of $\pm$10 μm at 3σ. A temperature-stable adhesive film was attached to the core bottom side. It is important to choose a relatively thick adhesive layer in order to allow bumps to penetrate into and to seal chip edges, avoiding resin flow onto the die surface during embedding. In the present study, a back-grinding tape ELEP Holder UB3102D from Nitto Denko was used. It has a UV-curable adhesive layer of 50-μm thickness.

The chips were placed face-down into the cavities by an automated placement machine. For an evaluation panel size of 305 mm × 227 mm, a Datacon 2200 evo bonder was used. Chip assembly for larger panels of 510 mm × 515 mm size was carried out in an ASM SiPlace CA3. Fig. 3 shows such a panel during assembly.

Next, an Ajinomoto build-up film (ABF) dielectric with 25-μm thickness (GX-T61) was applied onto the now tape-less backside of the panel using a Dynachem VA-7224-HP7 vacuum laminator. During lamination, gaps between chips and core were completely filled by the dielectric. Then, the adhesive film was illuminated with UV light and peeled off. Due to robustness and flexibility of the core, the film can easily be removed without the need for a thermal release adhesive. The panel was flipped and a further ABF film

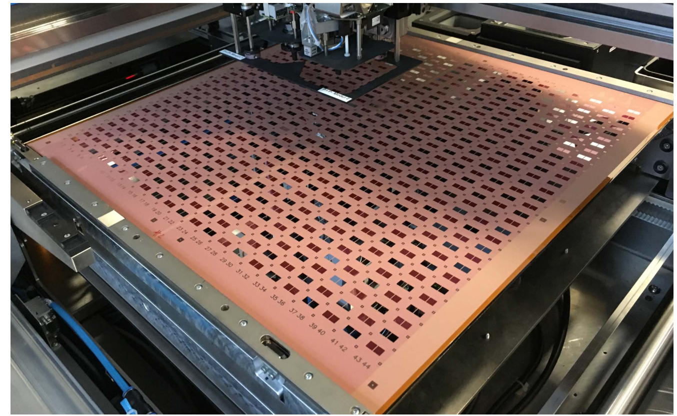
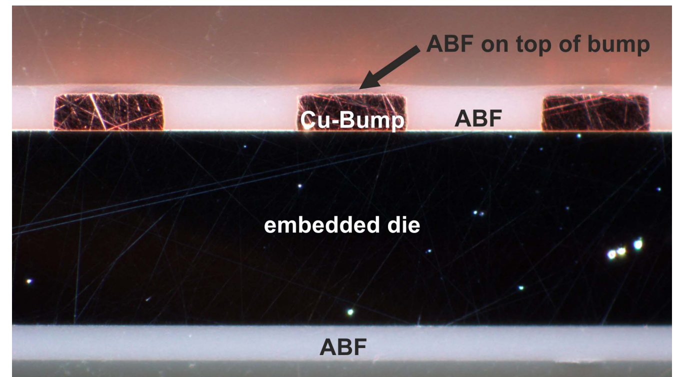
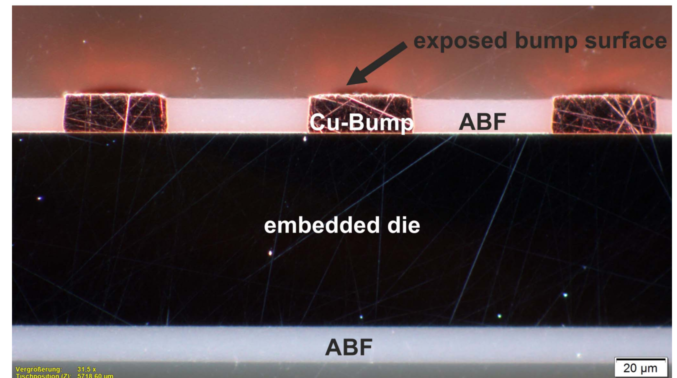


Fig. 3. Chip placement into cavities of a core panel (510 mm × 515 mm) with adhesive tape sticking to panel backside.



(a)



(b)

Fig. 4. Cross section of a chip with 15-μm Cu bumps embedded into an ABF dielectric. (a) After lamination with dielectric over bumps. (b) After plasma etching with exposed Cu surface.

(25-μm thickness) was laminated to the top side, serving as RDL dielectric. The low viscosity of the dielectric during hot lamination allowed the Cu bumps to penetrate into the layer. The result was a planar dielectric layer over the chips with bumps inside [see Fig. 4(a)].

The excessive dielectric over the bumps is removed in an O_2/CF_4 plasma to lay open the Cu bump top surface [see Fig. 4(b)]. The process was carried out in a Nordson MARCH PCB-800 plasma system (40-kHz RF power generator). First, a warmup step to 90 °C with the following parameters was done: power 3.5 kW, pressure 280 mTorr, and N2 flow 2.0 slm. Finally, ABF was etched at a rate of about 1 μm/min with

Fig. 5. Cross section of dies embedded in an organic laminate matrix with Cu RDL on top fabricated by semiadditive processing and adaptive direct imaging (DI).

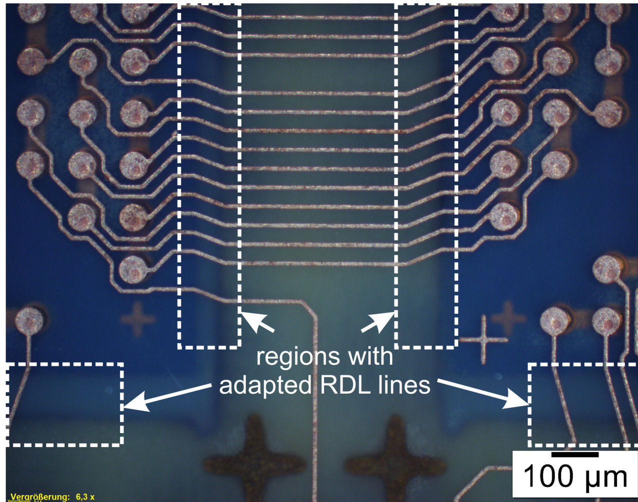


Fig. 6. Microscopic image of dies embedded in an organic laminate matrix with Cu RDL on top fabricated by semiadditive processing and adaptive DI.

3.5 kW, 200 mTorr, 2.0 slm O2, and 0.2 slm CF4 flow. However, while most of the bumps were completely exposed, there were few bumps still covered with residual dielectric. The inhomogeneity can be attributed to the plasma and/or the thickness variation of the dielectric over chips. At this point, further optimizations are needed. For a via-less process, mechanical polishing is also an alternative. To continue the process chain, conventional laser drilling with adapted drill positions was also used.

Before RDL formation, chip position and rotation angle of each chip were measured with a Rudolph Firefly S1200 inspection system. Subsequently, an individual RDL image with adapted connection traces based on measured data is calculated using an internally developed software. The software allows adapting lines in a limited region between chip edge and FO (like an elastic band). The RDL is then formed in an SAP as described in Section II, using a CREAMET 600 Cl2 S3 sputtering system and an Orbotech Ultra 200 LDI. In the depicted package comprising two chips, it is possible to contact both—despite individual die shift. One can also see the proper working of the adaptive imaging in the cross section of such a package in Fig. 5 (Figs. 5 and 6 are from different samples). Here, the chip on the left-hand side is placed close to the core (10-μm distance), whereas the chip on the right-hand side is shifted to about 81-μm distance. However, the RDL layer is following that die shift accordingly. Moreover, no voids or cracks are visible. Note that the RDL-to-bump interconnects are only observed here for the chip on the right-hand side due to the position of the cross-sectional plane.

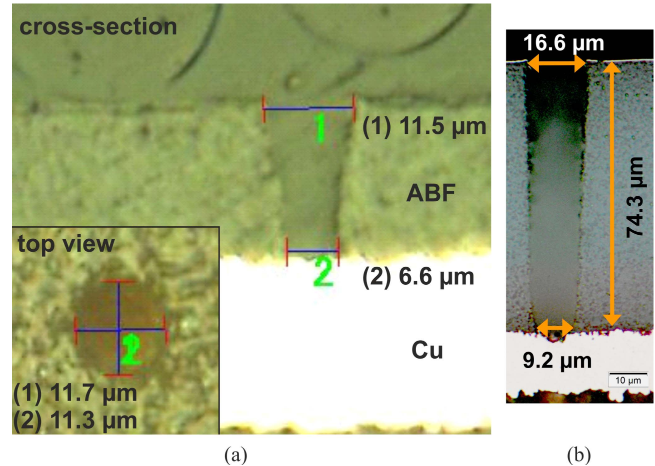


Fig. 7. Cross sections of laser-drilled microvia in ABF with (a) hole opining diameter of 11.5- and 20-μm depth and (b) aspect ratio of 4.4:1.0.

B. Laser Drilling

The motivation to develop deep microvia drilling and filling toward an aspect ratio 5:1 is to form vias around the embedded chips, allowing interconnects between RDL layers below and above. Since laser drilling through the glass fiber-reinforced core material is very slow, only drilling through the ABF encapsulation surrounding the chips in the PCB cavities is considered. Here, we aim for vias of 70-μm depth and 10–15-μm diameter to be adequate for chips of 50-μm thickness embedded in 10-μm RDL dielectric below and above. Fig. 7(b) shows a deep via in a 74-μm ABF dielectric with a hole diameter of 16.6 μm at the top beam entrance, yielding to a value of 4.4:1 for the aspect ratio. It was drilled by a Schmoll PicoDrill machine with 355-nm wavelength, 10-ps pulselength (picosecond laser), and 1-MHz pulse repetition rate. The conical shape of the hole is intended in order to improve sidewall metal coverage during sputtering and electrolyte flow during Cu filling. In the current project stage, smaller via diameters of 11.5 μm have also been realized. Fig. 7(a) depicts a via drilled by a Schmoll PicoDrill machine with 355-nm wavelength, 25-ns pulselength (nanosecond laser), and 100-kHz repetition rate.

C. Direct Imaging

The exposure of photoresist was performed in a prototype machine from the project partner Schmoll. The system is based on digital mirror devices (DMDs) with more than a million micromirrors at a pitch of 7.6 μm. The switchable mirrors are reflecting light of a 405-nm laser diode. By an optical system, the light is focused at the substrate surface, projecting

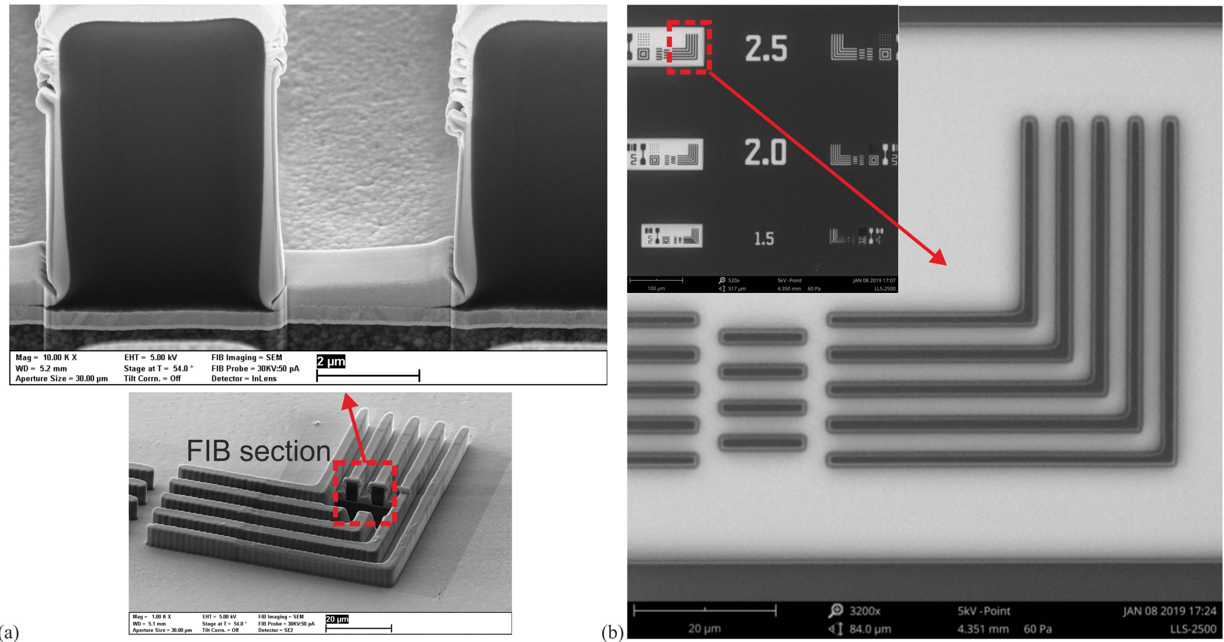


Fig. 8. (a) Photoresist exposed with DI machine with 4-μm linewidth at 7-μm height: FIB section of a 4-μm resist line (top left) and SEM view on test structures (bottom left). (b) SEM images of photoresist exposed with prototype exposure head of DI machine showing printing capability of 2.5-μm lines and spaces.

a demagnified image of the mirror array onto the photoresist. The optical system is designed for a lateral resolution of structures down to 4 μm. The exposure heads, containing laser diode, DMD, and optics, are moved over the substrate surface, exposing the resist in a scan mode. Substrates of up to 610 mm $\times$ 615 mm size and larger can be processed in the machine. The total exposure time for a panel depends on the number of exposure heads (up to 6) and the required exposure dose of the resist. By measuring fiducials on the substrate, a local scaling of the exposed pattern is possible, allowing the compensation of nonlinear substrate deformations.

For the exposure tests, a high-resolution photoresist from Hitachi Chemicals with a thickness of 7 μm was used (RY5107UT). Application of the very thin film by hot roll lamination did not lead to satisfactory results. Therefore, it was attached to the substrate by a Dynachem vacuum applicator.

For exposure tests, a pattern with structures down to 4-μm width and spaces were initially investigated. Fig. 8(a) shows a 4-μm test pattern after exposure and development. At 405-nm wavelength, the required energy dose was 600 mJ/cm^2. A focused ion beam (FIB) section of this resist lines is also depicted. Sidewalls are well defined and vertical, showing only a small resist foot at the bottom.

Further developments toward 2-μm lines and spaces are shown in Fig. 8(b). Here, a liquid resist on the wafer was exposed by a prototype exposure head. With this, line and space structures of 2.5-μm size were printed.

D. Deep Microvia Filling

For the experiments on Cu filling of high-aspect-ratio microvias, at first, an electrically conducting layer (usually Cu) within the drill hole sidewalls is necessary. The Cu seed layer of the microvias was sputtered in a high-power impulse magnetron sputtering (HiPIMS) process by project partner CreaVac. Here, NiCr (10-nm thickness) was used as a barrier layer between ABF and the Cu layer of about 7-μm thickness. Currently, a limit for aspect ratios greater than 4:1 seems to be insufficient sidewall coverage of the Cu seed layer. Therefore, further work will be done on improvement of the sputtering process.

In order to fully fill high-aspect-ratio microvias with Cu, a new plating chemistry of the project partner Schlötter was used. Here, the electrolyte is denoted as “E-via.” The filling effect is based on the interaction of additives in the Cu electrolyte. Suppressors and levelers with a high molecular weight are decreasing the plating rate, while it is enhanced by lightweight molecules [10].

Fig. 9 shows a Cu-filled microvia in a 79-μm dielectric and a top diameter of 20 μm, corresponding to an aspect ratio of 4:1. Filling was done in the dc plating mode at 0.25 A/dm^2 for 180 min.

After the solder dip test (five times at 288 °C, each dip 10 s), no delamination or damage has been observed in visual inspection.

E. RDL Plating

For plating tests, plain PCB cores were used. A Cu foil of 2-μm thickness was applied by lamination in a Lauffer lamination press. Subsequently, the Cu surface was treated with MECetchBOND CZ 2001 in a horizontal MECetch line to obtain a roughened surface for resist adhesion. A dry film resist of 25-μm thickness (Hitachi RD1225) was applied in a conventional hot roll laminator. Test structures of 12-μm linewidth and space were exposed in an Orbotech Ultra 200 LDI system at a wavelength of 355 nm and 50 mJ/cm^2. Resist development was performed in a horizontal developer system (Schmid CombiLine) in a carbonate solution. Cu plating is currently performed in a standard vertical PCB plater.

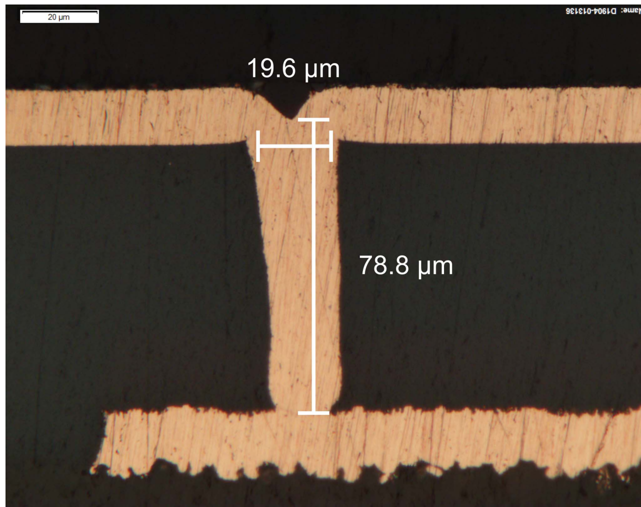
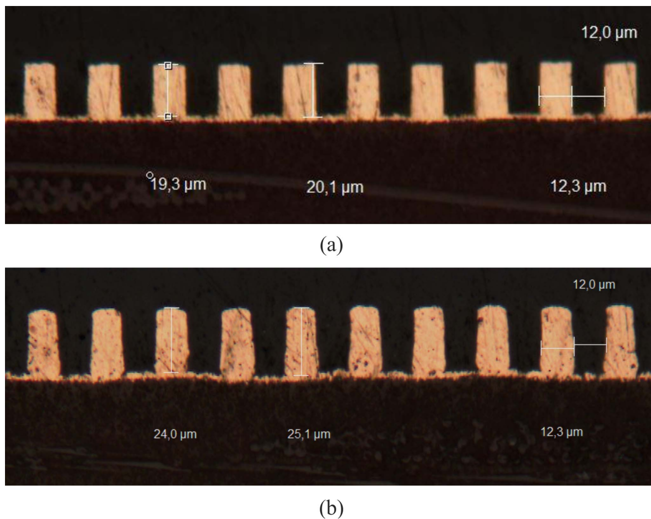


Fig. 9. Cross section of Cu-filled blind microvia with aspect ratio of 4:1.



(a)

(b)

Fig. 10. Cross section of electroplated Cu lines with 12-μm width. (a) Reverse pulse plating with 2 A/dm^2, 60 min, electrolyte "E-line." (b) DC-plating, 2 A/dm^2, 45 min, electrolyte "E-via."

The electrolyte used was an adapted bath from Schlötter, denoted here as "E-line." Plating was done at 2.0 A/dm^2 in a reverse pulse plating mode for 60 min. The result is shown in Fig. 10(a). The Cu line thickness is 20 μm corresponding to a plating rate of about 0.67 μm/min. The line cross-sectional profile is of the well-defined rectangular shape.

One goal within the project is to combine deep via filling and RDL plating at the same time in one plating machine using the same electrolyte. Therefore, in a further experiment, the electrolyte "E-via"—which was already applied for deep via filling (Fig. 9 in Section III-D)—was now used for RDL plating. Doing so, one can obtain the result shown in Fig. 10(b). Thus, the same electrolyte and plating mode (dc) were used for deep via filling and RDL plating. The corresponding cross-sectional profile is of appropriate rectangular shape. It is comparable to the lines in Fig. 10(a) plated with the designated "E-line" electrolyte. The slight curvature at the top of Cu lines [Fig. 10(b)] is assumed to become negligible for decreasing linewidth toward 4 μm. The RDL line uniformity will be investigated later when a dedicated panel-level plater is available.

In short, for deep via filling and RDL plating, the same electrolyte is suitable. The remaining difference in process parameters is the current density and time with 0.25 A/dm^2 and 180 min (via) or 2.0 A/dm^2 and 45 min RDL.

IV. Conclusion

In a public-funded research project, a novel approach for panel-level packaging technology was investigated. The main features are: 1) use of a PCB laminate core for embedding and 2) avoiding of via formation to the chip by tall bumps. In the current phase project, single-process steps have been evaluated. The feasibility of the embedding concept has been shown using small panels of 305 mm $\times$ 227 mm size initially. Formation and Cu filling of high-aspect-ratio (4:1) vias for vertical interconnects around the embedded chips were demonstrated. With a new LDI system, a resolution of 4 μm in a 7-μm dry film resist was achieved. An adaptive DI process utilizing measured chip positions after embedding was realized for a multichip package. Currently, the formation of RDL wiring has been demonstrated for 12-μm lines and spaces and a plated Cu thickness of 20–25 μm.

The goal of the next phase of the project is to demonstrate a complete process flow for manufacturing of 3-D SIPs on 600 mm $\times$ 600 mm panels.

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