Foreword: Special Section on Packaging and Interconnects: Cutting-Edge Solutions in Modeling, Design, and Characterization—Part I

IN A world of digitally native citizens, processors and memory are common topics of conversation, no longer restricted to the engineering community. It is only natural. After all, one does not need to be an architect to appreciate the skyline of a modern metropolis. But behind this postcard image is a complex world of substrates and interconnects and buffers and packages. Smartphones and self-driving vehicles require advanced printed circuit board (PCB) and IC design. Advanced design relies on specialized computer-aided design (CAD) tools. CAD requires modeling and an entire field of mathematical know-how. But technology exists in the physical realm. Progress is also driven by the advance of materials and manufacturing techniques. Prototyping requires accurate measurements and precise characterization. Layers upon layers of knowledge and expertise make the intricate infrastructure of modern electronics possible. We seek to give an overview of the recent innovations across these layers. This special section is built from selected work initially presented at the SPI 2018, EPEPS 2018, and EDAPS 2018, conferences that are co-sponsored by the IEEE Electronics Packaging Society (EPS).

Current fluctuations and power consumption are crucial issues in microprocessor systems. In "A Multicore Chip Load Model for PDN Analysis Considering Voltage–Current-Timing Interdependency and Operation Mode Transitions," Chen *et al.* come up with an elegant novel solution for the chip load model with the aim of avoiding oversimplifications that may strongly impact the design.

In "A Novel Desensitization Using Resonance Suppressors in Metallic Shielding," Chan and Wu use their previous experience in both circuit design and electromagnetics to come up with a novel solution for resonance suppression.

"Nonperiodic Flipped EBG for Dual-Band SSN Mitigation in Two-Layer PCB" is coauthored by researchers from National Taiwan University and Realtek Semiconductor Corporation. Hsieh *et al.* propose a novel design of 2×2 nonperiodic flipped-EBG structure that supports dual-band simultaneous switching noise mitigation in WLAN. The authors present a systematic design procedure resulting in an ideal dual-band electromagnetic bandgap in only two metal layers.

"An Adaptive Sampling Process for Automated Multivariate Macromodeling Based on Hamiltonian-Based Passivity Metrics" is authored by members of the EMC Group, Politecnico di Torino, Turin, Italy, known for their game-changing contributions to the field of macromodeling. The article builds on previous work related to parametric macromodeling and manages to find a good compromise between mathematical rigor and computational efficiency.

"Machine-Learning-Based Error Detection and Design Optimization in Signal Integrity Applications" incorporates the latest research in machine learning in an automated design optimization framework. Signal integrity is, naturally, the main focus.

"Efficient Time-Domain Sensitivity Analysis of Active Networks" extends Nouri's and Nakhla's previous work on an efficient model order reduction incorporating sensitivity analysis. The technique may successfully be used for a wide class of active systems; several illustrative examples are available in the article.

The IEEE EPS conferences offer ideal opportunities for experts working on packaging, interconnects, and all the related fields to meet, present their work, and establish collaborations. This special section seeks to provide an overview of the latest and the most daring topics that emerged from these conferences in 2018. It spans over two issues of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY, with a second part scheduled to appear in October 2019.

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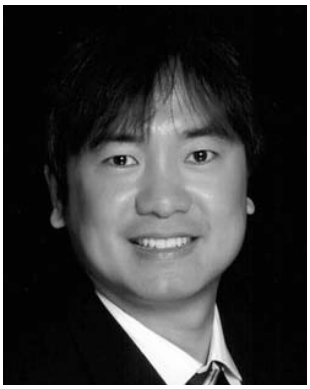
From 2008 to 2009, he was a Post-Doctoral Researcher with the EMC Group, Politecnico di Torino, Turin, Italy. He has been an Associate Professor with the University of Brest. His current research interests include linear and nonlinear macromodeling, model order reduction, system identification, computer-aided design (CAD), and related topics. Since 2015, he has been also conducting research in telecommunications with a focus on the design of nonlinear predistorters.

Dr. Telescu chaired the 22nd and the 23rd editions of the IEEE Workshop on Signal and Power Integrity in Brest and Chambery, France, respectively. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY.



Xiaoxiong Gu (S'00–M'07–SM'12) received the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2006.

He joined IBM Research, Yorktown Heights, NY, USA, as a Research Staff Member in January 2007. He has recently worked on antenna-in-package design and integration for millimeter (mm)-wave imaging and communication systems including Ka-band, V-band, and W-band phased-array modules. He has also worked on electrical packaging and signal/power integrity for high-speed I/O subsystems including on-chip and off-chip interconnects. He has coauthored more than 80 peer-reviewed publications and holds 9 issued patents. His current research interests include 5G radio access technologies, optoelectronic and mm-wave packaging, electrical designs, modeling and characterization of communication, imaging radar, and computation systems.

Dr. Gu has been serving on program committees for MTT-S, EPEPS, ECTC, EDAPS, and DesignCon. He was a recipient of the Best Session Paper Award at IEEE ECTC in 2007, the Best Interactive Session Paper Award at IEEE DATE in 2008, the IEC DesignCon Paper Awards in 2008 and 2010, the Best Conference Paper Award at IEEE EPEPS in 2011, the two SRC Mahboob Khan Outstanding Industry Liaison Awards in 2012 and 2014, the four IBM Plateau Invention Awards from 2012 to 2016, the IEEE EMC Symposium Best Paper Award in 2013, and the IBM Outstanding Technical Achievement Award in 2016. He was a co-recipient of the IEEE ISSCC 2017 Lewis Winner Award for Outstanding Paper, the IEEE JSSC 2017 Best Paper Award, and the 2017 Pat Goldberg Memorial Award to the best paper in computer science, electrical engineering, and mathematics published by IBM Research. He is the Co-Chair of the Professional Interest Community (PIC) on Computer System Designs at IBM. He was the General Chair of IEEE EPEPS 2018 in San Jose, CA, USA. He is also a Distinguished Lecturer of the IEEE EMC Society from 2019 to 2020.

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In 2010, he was a Brain Korea Post-Doctoral Fellow with the Design Automation Lab, Seoul National University, Seoul, South Korea. From 2011 to 2012, he was an Indo–U.S. Research Fellow with the Interconnect Focus Center, Georgia Institute of Technology, Atlanta, GA, USA. He joined the Electrical Engineering Department, IIT Ropar, Rupnagar, India, in 2012, where he is currently an Associate Professor. All along his tenure, he has initiated activities in the broader area of electronics. He is also the Coordinator of the Microelectronics and VLSI Design Research Group, Rupnagar. His current research interests include exploring signal integrity issues in high-speed chip-chip, on-chip and 3-D interconnects, 3-D IC design, and graphene-based nanoelectronic devices and interconnects.