Impact of Local Stress Distribution in a Silicon Chip Mounted by Area-Arrayed Copper Pillar Wafer-Level Packaging Technology on Analog-Circuit Performance

Naohiro Ueda, *Member, IEEE*, and Hirobumi Watanabe, *Senior Member, IEEE*

***Abstract*— The local stress distribution in a silicon chip encapsulated in an area-arrayed copper pillar-type flip-chip package was evaluated using specially designed test chips. Stress is sensed using piezoelectric resistors, which are p-type and n-type diffusion resistors embedded in a silicon chip measuring 7.8 mm × 7.8 mm. Each piezoelectric resistor measures approximately 0.03 mm in length and 0.002 mm in width, which is sufficiently small to measure the local stress distribution near each copper pillar. As a result of this study, it is revealed that the copper pillars have an impact on the local stress distribution in silicon chips, in particular producing a large stress gradient near the copper pillar edge, compared to the conventional wire-bonded packages. Since large stress gradients disturb pair characteristics of analog circuits, in order to design a high-precision integrated circuit employing a copper pillar-type flip-chip package, a specific regulation method to avoid overlap with the copper pillars is needed to maintain the accuracy of the analog circuits.**

***Index Terms*— Circuit, copper pillars, distribution, flip chip, piezoelectric, resistor, stress.**

I. Introduction

FLIP-CHIP packages are widely used in sophisticated portable electronic devices to satisfy the demand for smaller structure and higher density [1]. In flip-chip technology, an integrated circuit (IC) is connected vertically to a substrate through conductive bumps, such as copper pillars. Compared to the conventional wire-bonded packages, the flip-chip packages have fewer modules for stress relaxation, such as lead frame or bonding wires (Fig. 1). In addition, copper pillars, which are larger than typical metal–oxide–semiconductor field-effect transistor (MOSFET) structures, are located immediately above the circuitry (Fig. 2). A copper pillar has a thermal expansion coefficient larger than that of other materials in ICs, including solder (Table I). As a result, local deformation of the silicon chip is caused by the mismatch between different thermal expansion coefficients of the silicon chip and copper pillar. The structural signature of flip-chip packages could generate high localized stress and might cause not only deterioration of bonding reliability, such as delamination or cracking [2]–[8], but also circuit performance fluctuation due to the piezoelectric effect of active circuits [9]–[15].

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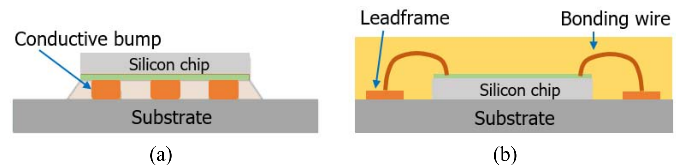

Fig. 1. Comparison of flip chip and wire bonding. (a) Flip-chip package. (b) Wire-bonded package.

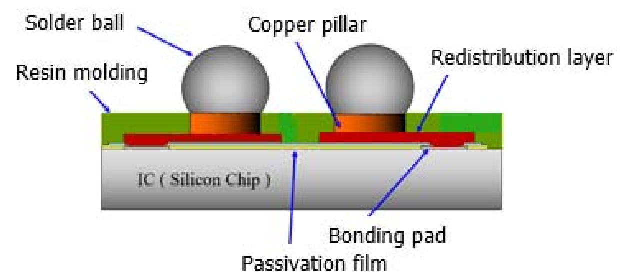

Fig. 2. Structure of the flip-chip package used in this paper.

In response to those concerns, we have designed a new test vehicle to evaluate local stress distribution in a flip-chip package. Measurement results for the local stress distribution near the area-arrayed copper pillars are reported in this paper. In addition, the impact of the local stress distribution on circuit components of the flip-chip and conventional wire-bonded packages is compared.

II. Experiment

In the test chip, the stress is sensed using piezoelectric resistors [16]–[21], which are p-type and n-type diffusion resistors embedded in a silicon chip measuring 7.8 mm × 7.8 mm (Fig. 3). Each piezoelectric resistor measures approximately 0.03 mm in length and 0.002 mm in width (Fig. 4).

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TABLE I
PHYSICAL PROPERTY VALUES

Material	Young's modulus (Pa)	Poisson ratio	Thermal expansion coefficient (1/K)
Si	1.3×10^{11}	0.28	3.0×10^{-6}
SiO_2	7.3×10^{10}	0.16	5.4×10^{-7}
Resin	1.6×10^{10}	0.24	9.0×10^{-6}
Copper pillar	1.3×10^{11}	0.34	1.7×10^{-5}
Solder ball	2.2×10^{10}	0.37	2.4×10^{-5}

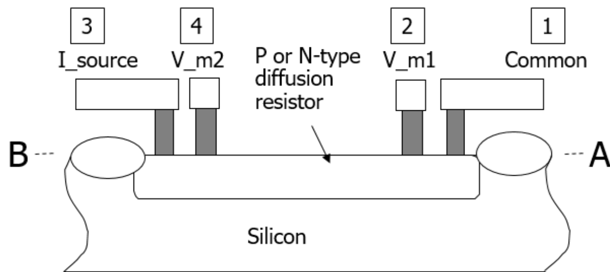

Fig. 3. Cross section of the piezoelectric resistor.

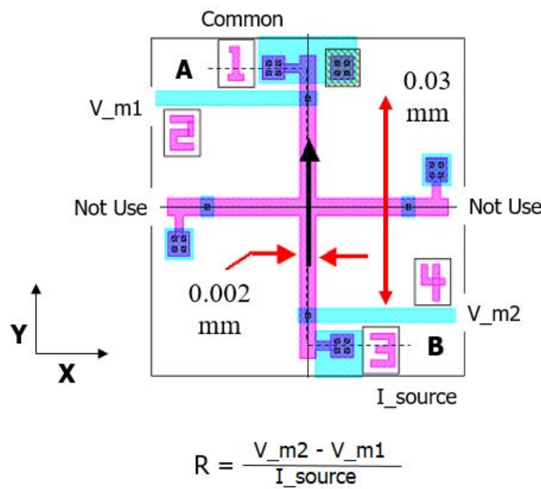

Fig. 4. Plan view of the piezoelectric resistor.

In order to avoid other disturbance factors, the sensor of this study was designed to work with four-point Kelvin resistance measurements [22].

The terminal numbers 1–4 in Fig. 3 correspond to the terminal numbers 1–4 in Fig. 4, respectively. The piezoelectric resistor is sufficiently small and sensitive to measure the local stress distribution near each copper pillar.

To measure the stress distribution near a copper pillar having a circular cross section, two kinds of samples were prepared, as shown in Fig. 5.

Sample A was used to measure the stress distribution when copper pillars are placed in the x-direction, as shown in area A, that is, 17 piezoelectric resistors were placed in the x-direction to the three copper pillars.

Meanwhile, sample B was used to measure the stress distribution when copper pillars are placed in the y-direction, as shown in area B, that is, five piezoelectric resistors were placed in the y-direction to the two copper pillars.

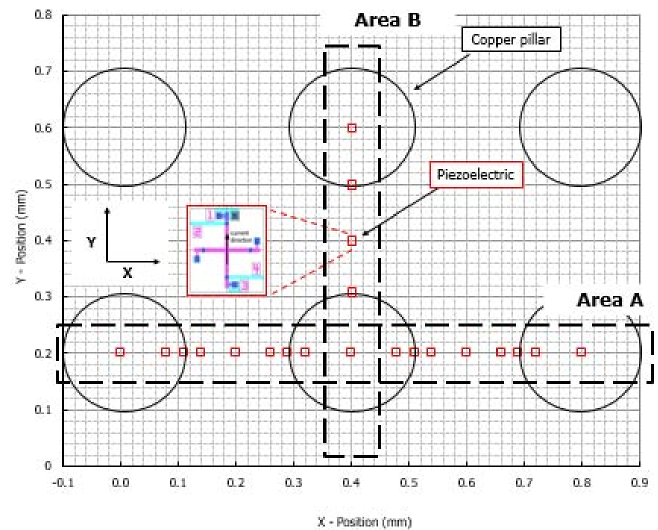

Fig. 5. Arrangement of piezoelectric resistors and copper pillars in samples A and B.

Also, it is noted that the current flows through the piezoelectric resistor in the y-direction.

As a result, the local stress distribution near a copper pillar can be visualized by combining the measurement results for both sample types.

The test chip was manufactured in a conventional complementary metal–oxide–semiconductor wafer process. Following completion of bonding pad windows, commercially available wafer-level chip size packaging (WL-CSP) technology was employed.

The WL-CSP steps included dielectric film coating, redistribution layer formation to build routing circuitry, formation of copper pillar electrodes, resin molding, and solder ball terminal formation (Fig. 6).

Next, each test chip was diced to the same size as the silicon chip. The test chip has area-arrayed copper pillars distributed over the entire chip surface with a 0.4-mm pitch. The pillar diameter and its height are approximately 0.22 and 0.09 mm, respectively. A scanning electron microscopy (SEM) image of the actual device in this paper is shown in Fig. 7.

The cantilever technique was applied to calibrate the response of the piezoelectric resistors (Fig. 8). The load stress was controlled by the intensity of the load cell. By pushing down or pushing up the silicon beam, it is possible to apply tensile stress or compressive stress to the target device under test, as shown in Fig. 9.

Each piezoelectric resistance coefficient π_{ij} for the p-type and n-type piezoelectric resistors was experimentally extracted through the controlled application of a uniaxial loading [23]. Calibration results for the p-type and n-type piezoelectric resistors in this paper are shown in Fig. 10.

R^{n} and R^{p} show the resistance value of n-type and p-type piezoelectric resistors, respectively. ΔR is the variation between the resistance values measured in the wafer condition and resistance value measured in the package condition. Measurements were carried out at room temperature.

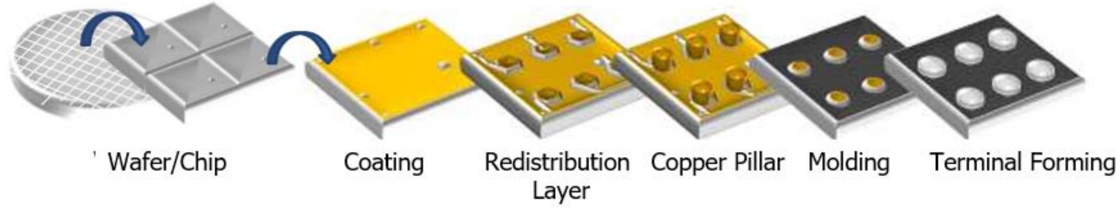

Fig. 6. WL-CSP technology.

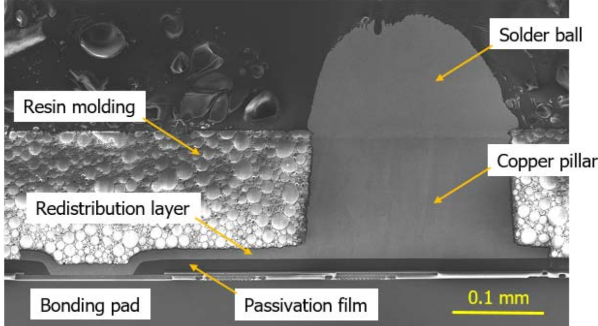

Fig. 7. SEM image of the actual device.

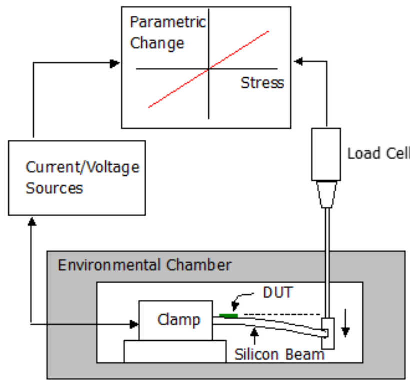

Fig. 8. Cantilever bending calibration system.

Then, x- and y-direction stress components (S_x and S_y, respectively) could be calculated by algebraic manipulation using the following equations [23], [24]:

$$\frac{\Delta R^{\mathrm{n}}}{R^{\mathrm{n}}} = \left(\frac{\pi_{11}^{\mathrm{n}}+\pi_{12}^{\mathrm{n}}-\pi_{44}^{\mathrm{n}}}{2}\right) S_x + \left(\frac{\pi_{11}^{\mathrm{n}}+\pi_{12}^{\mathrm{n}}+\pi_{44}^{\mathrm{n}}}{2}\right) S_y \quad (1)$$

$$\frac{\Delta R^{\mathrm{p}}}{R^{\mathrm{p}}} = \left(\frac{\pi_{11}^{\mathrm{p}}+\pi_{12}^{\mathrm{p}}-\pi_{44}^{\mathrm{p}}}{2}\right) S_x + \left(\frac{\pi_{11}^{\mathrm{p}}+\pi_{12}^{\mathrm{p}}+\pi_{44}^{\mathrm{p}}}{2}\right) S_y. \quad (2)$$

III. Results and Discussion

A. Measurement Results of Sample A

Measured results for Sample A are shown in Fig. 11. Both the stress values S_x and S_y changed periodically with peaks corresponding to the position of the copper pillars. The maximum compressive stress for the S_y component of around 20 MPa was generated at the copper pillar edge, and it gradually decreased toward the center of the copper pillar to approximately 7 MPa on average. The stress between copper pillars was almost zero or small tensile value.

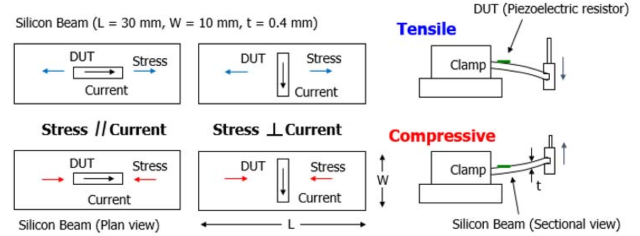

Fig. 9. Cantilever technique for extraction of piezoelectric resistance coefficient.

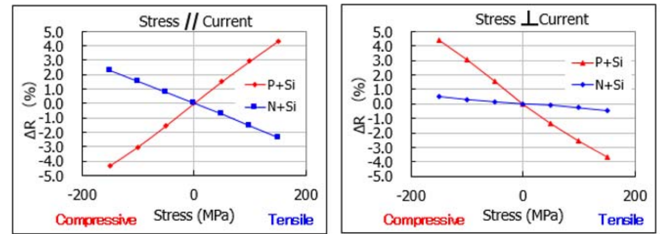

Fig. 10. Calibration results of p-type and n-type piezoelectric resistors.

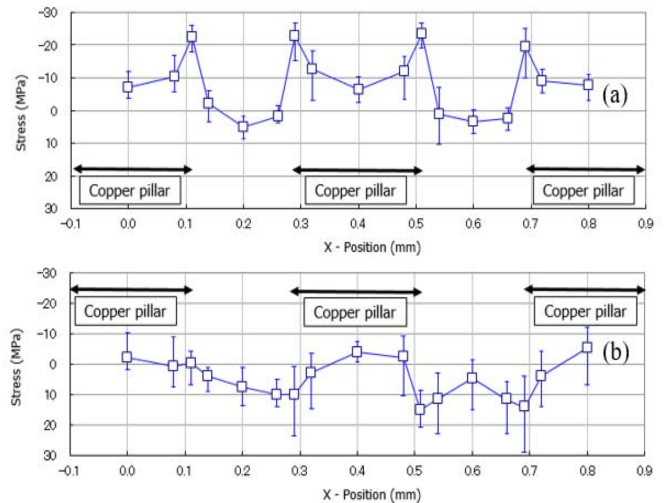

Fig. 11. Measured stress components in sample A. (a) S_y: y-direction stress. (b) S_x: x-direction stress.

Meanwhile, S_x exhibited similar values as S_y near the center of the copper pillar and the region between copper pillars. Compressive stress was less than 10 MPa at the center of the copper pillar, and small tensile stress was observed between copper pillars.

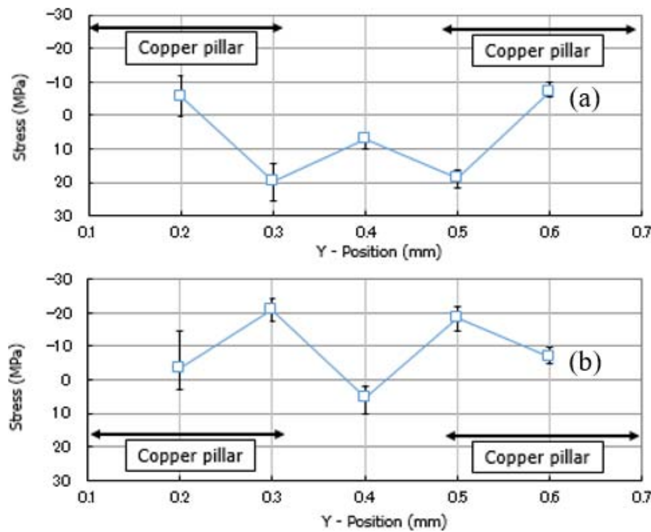

Fig. 12. Measured stress components in sample B. (a) S_y: y-direction stress. (b) S_x: x-direction stress.

It is reasonable that S_x and S_y exhibit almost the same values in these areas due to the chip's structural symmetry. Note that S_x exhibited approximately 10 MPa or larger tensile stress at the copper pillar edge, whereas S_y exhibited compressive stress larger than 20 MPa, on average, in this location.

B. Measurement Results of Sample B

Measurement results for sample B are shown in Fig. 12. Both S_x and S_y changed periodically with S_x peaks of around 20 MPa corresponding to the copper pillar edges. Thus, S_x in sample B exhibited the same response as S_y in sample A.

Regarding the copper pillar edge, S_y exhibited tensile stress larger than 10 MPa, which is the same behavior as S_x in sample A. The center of the copper pillar in sample B exhibited small compressive stress for both S_x and S_y, and the region between copper pillars exhibited small tensile stress for both S_x and S_y. These results are similar to those of sample A.

In this paper, evaluation was performed by using piezoelectric sensors with unidirectional (y-direction) current with respect to area A in the x-direction and area B in the y-direction in the arrangement of the copper pillars. For area-arrayed copper pillars arranged at equal intervals in the x- and y-directions, since equivalent results were obtained with samples A and B, it was confirmed that the x- and y-direction stress components can be quantitatively and accurately measured by using the piezoelectric sensor with a unidirectional current.

C. Local Stress Distribution Close to the Copper Pillar

Figs. 13 and 14 show stress distributions in samples A and B, respectively, where red arrows are compressive stress and blue arrows are tensile stress. The magnitude of the stress is roughly indicated by the length of the arrow shaft. Based on the results of the two samples, the local stress distribution near the copper pillar can be finally visualized, as shown in Fig. 15.

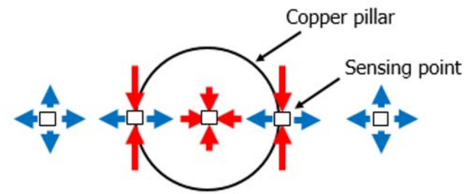

Fig. 13. Stress distribution resulting from sample A.

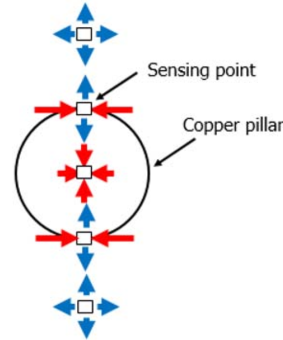

Fig. 14. Stress distribution resulting from sample B.

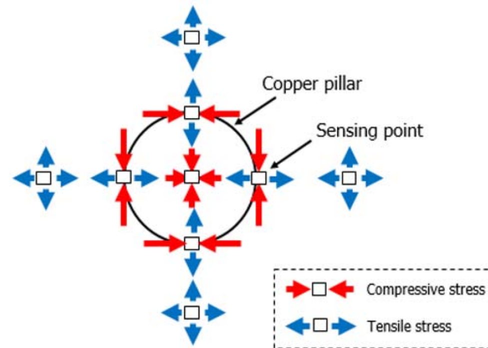

Fig. 15. Stress distribution near copper pillar.

Figs. 13–15 show that distinctive stress components occurred near the copper pillar. The compressive stress in the circumferential direction and tensile stress in the radial direction were generated at the copper pillar edge. Also, in the central area of the copper pillar, compressive stresses were generated in both the transverse and longitudinal directions.

The measurement results that compressive stress in the circumferential direction and tensile stress in the radial direction were generated at the copper pillar edge can be understood as follows.

Copper pillar having large thermal expansion coefficient undergoes volume shrinkage, whereby local deformation which directs toward the center of the copper pillar occurs in the silicon chip. An image chart of stress that generates in the silicon chip is shown in Fig. 16.

Focusing on the sensing point, it is understood that the tensile stress is generated in the x-direction due to local deformation that directs toward the center of the copper pillar. Meanwhile, the piezoelectric resistors that are placed

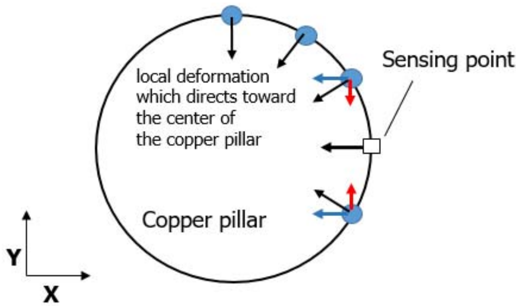

Fig. 16. Image chart of the stress generation.

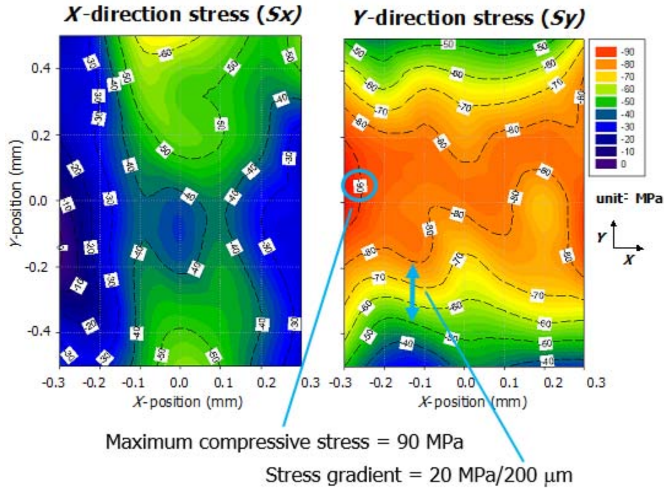

Fig. 17. Stress distribution for 0.8-mm × 1.2-mm silicon chip molded by the conventional SON packaging.

at the copper pillar edge is affected by the curvature of the copper pillar since the piezoelectric resistors used in the study measures 0.03 mm in length. As a result, the compressive stress in the y-direction is detected due to the y-direction components.

D. Comparison Between Two Kinds of Packages and Impact on a Circuitry

Next, we compared the stress distributions of WL-CSP and conventional wire-bonded packaging and evaluated the impact of stress distribution on a circuit.

Fig. 17 shows the stress distribution about a 0.8-mm × 1.2-mm silicon chip formed by small outline on (SON) lead packaging [25]. The maximum compressive stresses for both S_y and S_x were generated in the central area of the chip, and they gradually decreased toward the chip edge. With respect to S_y, maximum compressive stress was approximately 90 MPa, almost five times larger than the stress generated at the copper pillar edge in WL-CSP.

We evaluated the stress gradient, the amount of change in stress over a distance. The SON chip exhibited a difference of 20 MPa over a distance of 200 μm, giving a stress gradient of 0.1 MPa/μm. In contrast, the WL-CSP chip exhibited a difference of 25 MPa over a distance of 25 μm, giving a stress gradient of 1.0 MPa/μm. Thus, WL-CSP has a stress gradient that is ten times larger than that of the SON packaging (Table II).

TABLE II
COMPARISON BETWEEN PACKAGE TYPE AND THE IMPACT OF STRESS

Package type	Maximum compressive stress (MPa)	Maximum stress gradient (MPa/μm)
WL-CSP	20	1.0
SON	90	0.1

Large stress can cause a large performance change due to the piezoelectric effect, and circuit designers need to account for this fluctuation. This effect is not reflected in the Simulation Program with Integrated Circuit Emphasis (SPICE) model parameters extracted from the condition of the wafer, which is generally used in chip design. This is more important for the SON packaging than for the copper pillar-type WL-CSP [26]–[29].

A large stress gradient has a great impact on circuit components that require paired operation. For example, pairs of transistors in input circuits for amplifiers and resistor ladder networks with divided output voltage are required to have closely matched characteristics [30]. Therefore, for WL-CSP, specific consideration, such as keeping such elements away from the copper pillars, is necessary because characteristics can become mismatched where the stress gradient is large.

IV. CONCLUSION

Local stress distribution in a silicon chip encapsulated in the area-arrayed copper pillar-type flip-chip package was evaluated using a specially designed test chip. It was revealed that periodically placed copper pillars have an impact on the local stress distribution in silicon chips, in particular producing a large stress gradient near the copper pillar edge. A regulation method that designs high-precision ICs to avoid overlap with the copper pillars is needed to maintain the accuracy of analog circuits when applying the copper pillar WF packaging.

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