Flexible Hybrid Electronics Technology Using Die-First FOWLP for High-Performance and Scalable Heterogeneous System Integration

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***Abstract*— A technological platform is established for scalable flexible hybrid electronics based on a novel fan-out wafer-level packaging (FOWLP) methodology. Small dielets are embedded in flexible substrates we call FlexTrate. These dielets can be interconnected through high-density wirings formed in wafer-level processing. We demonstrate homogeneous integration of 625 (25 by 25) 1-mm^2 Si dielets and heterogeneous integration of GaAs and Si dielets with various thicknesses in a biocompatible polydimethylsiloxane (PDMS). In this paper, 8-μm-pitch die-to-die interconnections are successfully implemented over a stress buffer layer formed on the PDMS. In addition, coplanarity between the PDMS and embedded dielets, die shift concerned in typical die-first FOWLP, and the bendability of the resulting FlexTrate are characterized.**

***Index Terms*— Fan-out wafer-level packaging (FOWLP), flexible hybrid electronics (FHE), flexible substrate, heterogeneous integration, high-density interconnect, polydimethylsiloxane (PDMS).**

I. Introduction

In THE past decades, flexible device works can be mainly divided into three categories: the first one is the use of organic semiconductors that are deposited on flexible substrates in sheet-level processing or roll-to-roll processing [1]–[3]. The second strategy utilizes thin-film transistor fabrication on flexible substrates [4], [5]. The third approaches rely on transfer technologies that can allow the integration of an extremely thin monocrystalline inorganic semiconductor layer on flexible substrates such as silicon-on-insulator and III–V semiconductors on Si [6], [7]. Although the performance of the organic semiconductors has relatively improved recently [8], [9], the performance of inorganic monocrystalline semiconductors represented by Si and III–V compounds will not be achieved by the organic semiconductors.

On the other hand, flexible hybrid electronics (FHE) combine the flexibility of flexible substrates with the performance of inorganic monocrystalline semiconductor devices to create a new category of electronics [10], [11]. Traditional rigid/flex packages enable us to integrate thick Si dies on flexible substrates [12], [13]. However, these technologies are not based on wafer-level packaging (WLP), and in addition, the flexibility is limited by their rigid substrates. More recently, in order to enhance the flexibility of the rigid monocrystalline semiconductors, ultrathin dies are mounted on flexible substrates [14], [15]. This is because such thinned dies can be more flexible and follow curved profiles. However, ultrathin dies are very sensitive to applied stresses [14] by which both the performance degradation and property deviation would be induced with small bending radii. Lee *et al.* [16] have reported that the retention time of thinned dynamic random access memory having planar capacitors is shortened when the die thickness is less than 50 μm.

We have been working on holistic heterogeneous system integration using silicon interconnect-fabric (Si-IF) that can eliminate the organic laminates and achieve the drastic reduction of interconnect length between hardened intellectual property dies "dielets" integrated on Si wafers at small interdie spaces [17], [18]. In our FHE approach, the rigid dielets are embedded in flexible polymeric substrates we call FlexTrate that is fabricated at the wafer level using an advanced die-first fan-out WLP (FOWLP) technology. Classical FOWLP is expected to reduce package sizes, shorten interchip wirings by eliminating laminates, and integrate dies in rigid epoxy mold compounds (EMCs) [19], [20]. Several redistributed wiring layers (RDL)-first approaches with and without wafer-level processing have been reported for rigid [21] or flexible [22], [23] device system integration. Compared to RDL-first FOWLP with die/flip-chip bonding processes, die-first FOWLP is cost effective [24]. If the die shift issues in die-first FOWLP are mitigated, the production yield would be further increased, leading to drastic cost reduction. The biggest advantage of the die-first FOWLP is that wire bonding, printable wiring, and solder bumping are not required for connecting the neighboring dies and there are no additional

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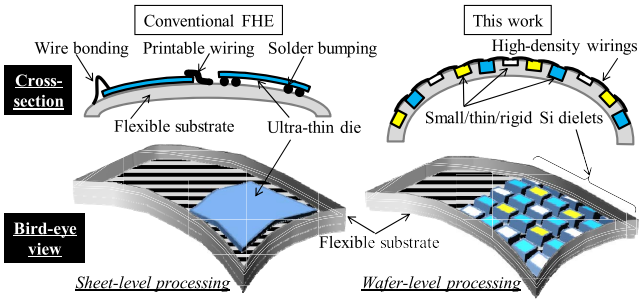


Fig. 1. Schematic comparison of die integration for FHE. Ultra-thin/large die bonded on flexible substrate (left). Small/thin/rigid dielets embedded in flexible substrate "FlexTrate" (right).

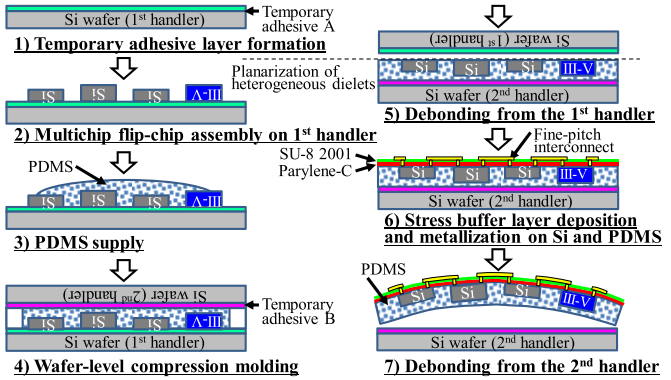


Fig. 2. Process flow of FlexTrate fabrication.

packaging processes due to the embedded structure [25], [26]. In our embodiment of this approach, the high flexibility is achieved by the unique structure of FlexTrate consisting of the hard and soft segments analogous to how a bicycle chain is flexible in spite of rigid chain components. As depicted schematically in Fig. 1, the dielets themselves are not expected to bend, whereas the polymer regions are bent in between the dielets which act like the joints in the bicycle chain. Heterogeneous dielets are embedded in a flexible substrate, and then electrically connected with high-density interconnects formed in wafer-level processing. Similar structures using rigid device islands interconnected with horseshoe wirings have been developed for stretchable electronics [13], [22], [23], but the fabrication concept of these systems is considerably different from FlexTrate based on scalable WLP using embedded Si dielets that are assembled in a face-down configuration. Landesberger *et al.* [27] have presented a quite similar approach to our FOWLP-based FlexTrate although they employ ultrathin Si dies having equalized die thicknesses and the dies are bonded in a face-up configuration [27]. Due to our advanced die-first FOWLP, the FlexTrate allows scalable integration of heterogeneous dielets with various thicknesses and much tighter interconnect formation than the conventional rigid/flex packages fabricated in sheet-level or roll-to-roll processing. In addition, fine-pitch interconnects can be formed at the wafer level. Nowadays, inkjet printing can draw very fine wirings in parallel, but the wire thicknesses are limited [28]. FlexTrate with inorganic monocrystalline semiconductor dielets can realize highly integrated flexible device systems without using low-performance organic semiconductors, ultrathin devices/dies, and colloid-/paste-based wirings.

In this paper, we demonstrate fine-pitch (<10 μm) interconnect formation on a biocompatible polydimethylsiloxane (PDMS) in which Si dielets are embedded by using the advanced die-first FOWLP technology. In addition, coplanarity between PDMS and dielets and die shift concerned in typical die-first FOWLP are characterized to implement the new flexible device system integration processes. High-density interconnect formation on the elastically deformable/stretchable PDMS rubber without cracks is very challenging compared with that on rigid EMCs. From a reliability point of view, the bendability of the FlexTrate is also evaluated by cyclic bending test.

II. Experiments

A. Materials

A biocompatible PDMS "Silastic MDX4-4210 (Dow)" was used in this paper. The biocompatible PDMS consisting of a base resin and a curing agent was uniformly mixed and defoamed with a planetary centrifugal mixer (THINKY, ARE-310) prior to compression soft molding.

Rivalpha 3195M and 3195V (Nitto denko) were used as the first and second temporary adhesives, respectively. The mechanically peelable layer was typically laminated at room temperature on the first Si handler. The other thermally removable layer was attached on the PDMS and dielets.

B. Measurement

The surface profile was measured with noncontact white light interferometer (cyberTECHNOLOGIES, CT100) and a contact-type stylus (Veeco, DEKTAK 150). The water contact angles were determined with the goniometer (VCA3000S, AST Products, Inc., Billerica, MA, USA). Resistances were measured with the probe station with probes (model: 7T-J3/20$\times$1.25," taper: 200–220," radius: 2 μm, overall length: 1.25," American Probe & Technologies, Merced, CA, USA) and probers (Model 350, The Micromanipulator Co., Inc., Carson City, NV, USA) equipped with a count multimeter (5491B, BK PRECISION, Yorba Linda, CA, USA) and a dc power supply (E3644A, Agilent).

C. Fabrication

The 100-μm-thick 1-mm-sqaure Si dielets were fabricated by plasma dicing in GINTI, Tohoku University, Sendai, Japan. Fig. 2 shows the total process of FlexTrate fabrication. A temporary adhesive 3195M was laminated on the first Si handler. Then, the Si dielets were precisely aligned in a face-down configuration on the adhesive formed on the first handler using a K&S APAMA die to wafer assembly tool. A biomedical grade PDMS was applied on the die-on-wafer structure, followed by vacuum defoaming with a vacuum level of <133 Pa from the high-viscous PDMS sandwiched with the second Si handler for 30 min or more. The second handler has another temporary adhesive 3195V. The subsequent compression mold with the second handler

is done with a wafer bonder (SUSS Micro Tec, SB6) with a compression force of 600 N. The first handler was then thermally debonded at 130 °C for 2 min, and subsequently, the hundreds of the Si dielets were transferred to the second handler. Prior to the following metallization processes, a thin stress buffer layer (SBL) of Parylene-C and a photosensitive planarization layer SU-8 2001 (Microchem) were sequentially formed with a parylene coater (Specialty Coating Systems, PDS 2010,) and simple spin coating on the PDMS/dielets, respectively. By using standard photolithography processes with a vacuum evaporation technique, fine-pitch Au wirings (10-nm-thick Ti as an adhesion/barier layer and 200-nm-thick Au) were deposited on the SU-8/Parylene-C/Si dielet array and the surrounding PDMS at the wafer level. Au interconnects were formed by wet etching with chemicals of an iodine complex/potassium iodine/wafer 1/4.2/294.8 (wt%) mixture for Au and a buffered fluoric acid (hydrogen fluoride/ammonium fluoride 1/6 wt%) for Ti. On the other hand, Cu wirings were formed by PVD and wet etching with a mixture of acetic acid/35% hydrogen peroxide/wafer 1/1/18 by weight. Finally, the FlexTrate was thermally debonded at 180 °C for 1 min from the second handler. The flexible, tough, and less stretchable properties of the Parylene-C can prevent the wires from being elongated, following thermal and mechanical deformation of the PDMS. However, since the nonphotosensitive Parylene-C is conformably deposited on the small steps formed at the interface between the PDMS and embedded dielets, the additional photosensitive spin-on layer SU-8 is required to planarize the step and electrically contact to the dielets through the Parylene-C.

III. Results and Discussion

A. Coplanarity Evaluation

High coplanarity between PDMS and embedded dielets after wafer-level compression molding is needed to integrate fine-pitch interconnects on FlexTrate. If the coplanarity is low, defocusing when using steppers and large proximity gaps when using mask aligners lower their lithographic resolution for patterning. As shown in Fig. 3, 625 (25 by 25) pieces of Si dielets are successfully transferred from the first handler to the second one. The 3-D surface profiles are measured with a surface metrology system (cyberTECHNOLOGIES, CT100) equipped with confocal white light. These data are analyzed and the average coplanarity between molded PDMS and transferred dielets in addition to the intradielets are summarized in Fig. 4. The PDMS is cured at room temperature. From the coplanarity of the intradielets, almost all dielets shows the die tilt with the height gaps of within 1 μm. Concerning coplanarity among the PDMS and embedded dielets, the high frequencies are obtained from 1 to 4 μm and the maximum height gap is below 6 μm. These height gaps including die tilt are attributed to die placement and PDMS curing conditions: the die placement force is 5 N/chip (=5 MPa).

Fig. 5 shows the effect of PDMS curing temperature and adhesive thickness (10 or 50 μm) on these height gaps. Here, die placement force of 2 N/chip is employed. The minimum die tilt of the intradielets is obtained by room-temperature

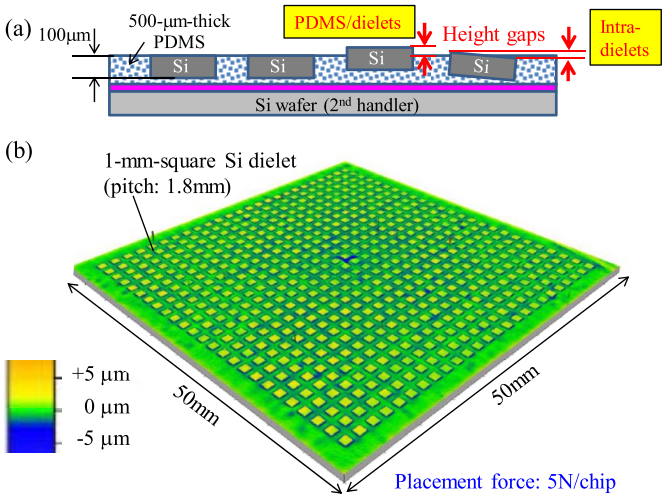


Fig. 3. (a) Cross-sectional schematic and (b) 3-D surface profile of Si dielets embedded in molded PDMS after transfer to the second handler.

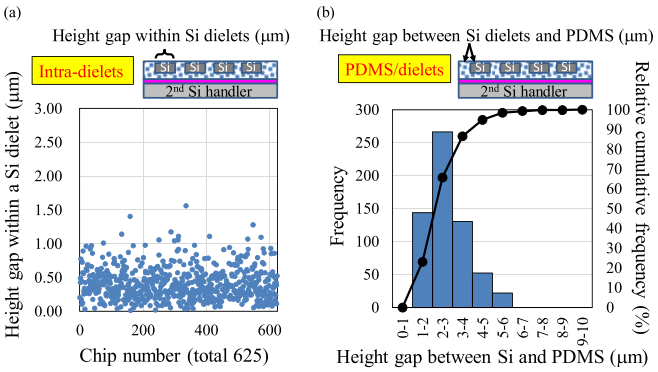


Fig. 4. Coplanarity between (a) intradielets and (b) PDMS and dielets.

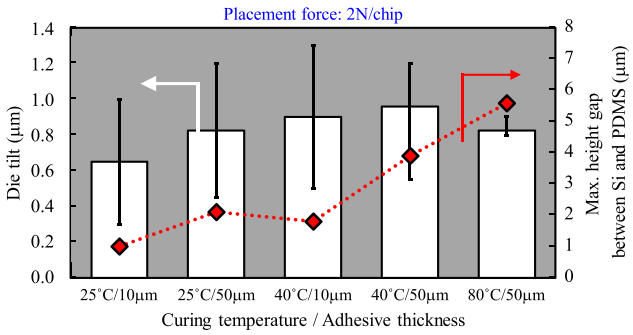


Fig. 5. Impact of PDMS curing temperature and adhesive thickness on height gaps of intradielets and between PDMS/dielet.

PDMS curing and the 10-μm-thick temporary adhesive. However, the die tilt is not significantly affected by these conditions. On the other hand, the impact of these conditions on the height gap between the PDMS and Si dielets is high. The height gaps can be reduced down to 1 μm when we employ the 10-μm-thick temporary adhesives and room-temperature PDMS curing. These results indicate that elevated curing temperature of PDMS softens the adhesive layer, resulting in dielet sinking down into the layer during compression

TABLE I

PROPERTIES OF A BIOCOMPATIBLE PDMS FOR FLEXTRATE AND A NONBIOCOMPATIBLE RIGID EPOXY USED IN TYPICAL FOWLP

Properties	PDMS (MDX4-4210 / Dow)	EMC [30]
Elongation at break	~500%	< 1%
CTE	~300 ppm/K	7.5 ppm/K
Young's modulus	0.5 MPa	22 GPa
T_g	-120˚C	165˚C
Curing temp.	25˚C - 80˚C	125˚C
Biocompatibility (screening test)	Passed up to 29 days for implantation in the human body.	None

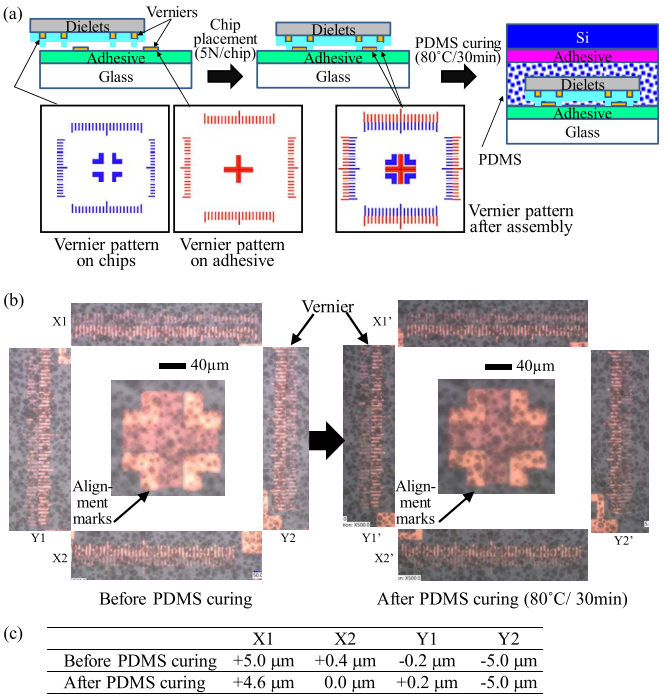
molding. We assume the differences given by the adhesive thickness would be resulted from their softening behavior at elevated temperature between the two adhesives: one is a thicker thermally removable layer and the other is a thinner mechanically peelable layer. Several micrometers in the height gap between the PDMS and dielets can be mitigated by the subsequent planarization process with SU-8 to be formed on a conformably deposited Parylene-C layer.

B. Die Shift Challenges

Die shift is a serious problem in current die-first FOWLP using rigid EMCs. In [19], the average die shift is beyond 40 μm and maximum die shift is nearly 80 μm. This large die shift would be given by thermal cure shrinkage, low adhesion strength between temporary adhesives and dies, and CTE mismatch between EMCs and dies. The EMCs including silica fillers have relatively low CTE that is one-order magnitude lower than typical epoxies. However, the die shift cannot be restricted, and thus, the die shift issues are solved by die preshift that makes deliberate misplacement of dies in their pick-and-place process to account for drift [19]. The prediction can compensate for the die shift, but that is not perfect. Nowadays, lithography tools are dedicated to FOWLP applications, and for instance, steppers can accurately follow the large die shift in a die-by-die alignment mode [29]. Although the allowable values for die shift depend on lithographic tools, large die shift definitely reduces WLP density and production yield/throughput for patterning.

In this paper, a biocompatible PDMS elastomer is employed as a flexible substrate. The thermomechanical characteristics of the biocompatible PDMS "Silastic MDX4-4210 (Dow)" and a rigid EMC including silica fillers used in a typical FOWLP research [30] are summarized in Table I for comparison. The elongation at break of the PDMS is quite high, compared with the EMC. The PDMS has high CTE with respect to both Si and Cu, 300 versus 3 and 17 ppm/K, respectively. The glass transition temperature T_g of the PDMS is much lower than room temperature. The huge difference from the rigid epoxy is the 0.5 MPa of Young's modulus that is four orders of magnitude lower than the EMC.

The PDMS has large $\alpha 1$ showing a CTE at below T_g. However, the T_g is much lower than room temperature, which means thermal stress accumulated with Young's modulus and CTE ($\alpha 1$) mismatch in the temperature regions ranging



(c)

	X1	X2	Y1	Y2
Before PDMS curing	+5.0 μm	+0.4 μm	-0.2 μm	-5.0 μm
After PDMS curing	+4.6 μm	0.0 μm	+0.2 μm	-5.0 μm

Fig. 6. Die shift evaluation: a flow of sample fabrication and Vernier patterns formed on (a) dielets and adhesives and (b) photographs of the Vernier patterns and (c) die shift values obtained before and after PDMS curing at 80 °C for 30 min.

from room temperature to T_g is experimentally zero [31]. According to the Stoney equation [32] simply calculated with the following PDMS/EMC/Si parameters: Young's modulus: 0.5 MPa/22 GPa/190 GPa, CTE: 300/7.5/2.6, PDMS/EMC curing temperature: 80 °C/125 °C, and 0.272 for Si Poisson ratio, the 300-mm-diameter Si wafer warpages of the PDMS and EMC with a thickness of 500 μm are 1.8 μm and 2.4 mm, respectively. The biggest difference is due to the low Young's modulus of the PDMS. Although the Stoney's equation can well assume the film thickness to be less than 1/20 of the substrate thickness and is effective for smaller substrate [33], [34], general elastomers represented by PDMS will be estimated to apply extremely low stresses so as not to drift embedded dies.

To accurately evaluate die shift between before and after PDMS curing, Vernier scale patterns are formed on the temporary adhesive. The process flow is shown in Fig. 6(a), where a 50-nm-thin Cu layer is deposited on the thermally releasable temporary adhesive (Rivalpha 3195M) laminated on a 500-μm-thick glass wafer by PVD, followed by wet etching to make the Vernier patterns. The dielets having the corresponding Vernier patterns were fabricated in GINTI, Tohoku University, by using Cu wet etch and plasma dicing processes. The resolution of the Vernier patterns is 0.2 μm and we can evaluate the die shift within 5 μm with the Verniers. These dielets are gently placed upside-down on the temporary adhesive with the flip-chip bonder (K&S, APAMA): placement force is 5 N/mm^2 at bottom stage temperature is 60 °C. The adhesion strengths of the temporary adhesive before and after Cu PVD and patterning are 0.75 and 0.60 MPa. The shear

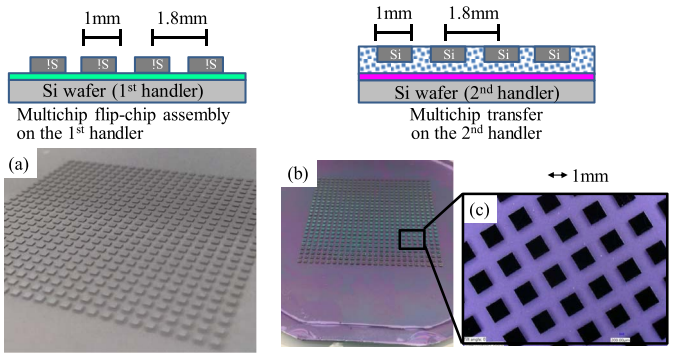


Fig. 7. Photomicrographs of 1-mm^2 multidielets placed on the first Si handler (die pitch: 1.8 mm): (a) bird-eye view. Photomicrographs of 1-mm^2 multidielets transferred to the second Si handler: (b) top view and (c) magnified top view.

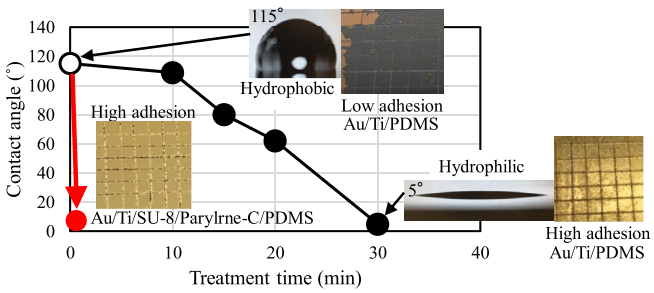


Fig. 8. Water contact angle shift as a function of PDMS surface modification time with UV/O_3 (black) or O_2 plasma (red) and images after Scotch tape test for adhesion strength evaluation.

bonding strengths are measured with a multipurpose bond tester (Dage Co., 4000Plus). We evaluate the die shift before and after PDMS curing at 80 °C for 30 min by wafer-level compression mold with the second Si handler.

The typical images before and after PDMS curing is shown in Fig. 6(b). As compared with these images, the die shift is hardly observed after PDMS curing. The initial die placement errors are nearly 5 μm or more because the alignment marks formed at the center of the die placement position on the temporary adhesive is unclear due to the roughened surfaces of black particles as a thermal bubbling component in the thermally removable layer. Surprisingly, the die shift can be compensated by using the PDMS even though the shear bonding strength between the Rivalpha surface and dielets is not high. The reason why the extremely low die shift is obtained is probably due to the excellent thermomechanical properties of the PDMS such as very low Young's modulus, low curing temperature, and low T_g much lower than room temperature. Also, we cannot ignore the use of middle-sized wafers with a diameter of 100 mm in this paper. The images are captured in the position 30 mm away from the center of the wafers with a high-resolution digital microscope (Keyence, VHX-6000). The die shift works are still going to well know the mechanism and further investigate the die shift in the subsequent PDMS transfer and metallization processes.

C. Process Integration With High-Density Interconnect

As shown in Fig. 7, 625^2 1 mm $\times$ 1 mm dielets were assembled on the first Si handler, and were successfully transferred to the second handler at 130 °C. Then, the metallization with evaporated Ti/Au is performed on the PDMS and embedded Si dielets covered with a 1-μm-thick oxide layer on the top. However, adhesion between the metals and the PDMS is quite low. Therefore, a surface modification step was inserted into the process to enhance the adhesion between the metal and PDMS. By using an UV/O_3 treatment, the water contact angle is dramatically decreased, and consequently, the PDMS surface is rendered highly hydrophilic, as shown in Fig. 8. These hydrophilic surfaces can increase the adhesion strength between the metal and PDMS as seen from pictures insets in Fig. 8. The Scotch tape adhesion test was based on ASTM D 3359-87 method B. Another surface modification with oxygen plasma (power: 65 W, O_2 flow: 100 sccm, and etching time: 30 s) can further reduce process time.

In the metallization process, photoresists are used for the metal patterning as a mask material for photolithography processes. However, cracks were generated in the use of a standard positive photoresists (Microchemicals, AZ5214E) in the cooling step after spin coating and the subsequent prebaking. Thus, we propose the use of an SBL between the metals and PDMS. Parylene-C was employed as an SBL. In addition, the surface of the PDMS after transferring it on the second handler is not perfectly smooth because of the small steps at the interface between the PDMS and Si dielets. SU-8 is employed as a planarization layer by spin coating. The spin-on photosensitive material also helps to open contact holes down to dielets through their top passivation in the future works. Generally, Parylene-C has low adhesion to various polymeric materials and Si/glass substrates [35]. Although several surface modification techniques have been reported [36], [37], the adhesion enhancement between the PDMS and parylenes is still a big concern. To enhance the Parylene-C/PDMS adhesion, we newly utilize vinyl triacetoxy silane (AP3000, Dow) that is well known to be an adhesion promotor for BCB (benzo cyclobutene resin) to Si substrates [38]. After PDMS surface modification with oxygen plasma, AP3000 was spin coated on the treated PDMS. The vinyl functional groups would react with free radicals generated in $CH_2 = C<$ double bonds of di-para-xylylene resulted from the pyrolysis of the Parylene monomers in the next step. Then, the Parylene-C surface is treated with the oxygen plasma in the same conditions again, SU-8 2001 was coated and cured, followed by Ti/Au deposition with an EB evaporator (CHA, solution). After deposition of the metals, the adhesion strength is evaluated by the Scotch tape test. As seen in the image inserted into the bottom left in Fig. 8, the adhesion at the interfaces of Au/Ti, Ti/SU-8, SU-8/modified Parylene-C, and Parylene-C/modified PDMS is very high.

Photoresists can be coated on the metal deposited on the SBL without cracks and dewetting. In addition, the SBL formation can allow the metal deposition without microcracks reported in [39] by mitigating the CTE/elongation/modulus mismatches between the PDMS and metals. As a result, Ti/Au wirings with the SBL are electrically connected between

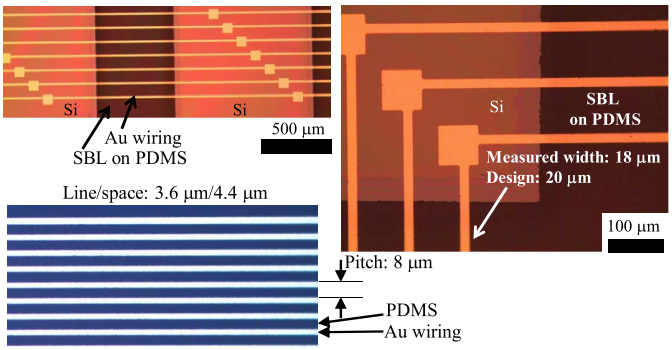


Fig. 9. Optical images of intradielet/fine-pitch wirings formed on Si/PDMS in wafer-level processing.

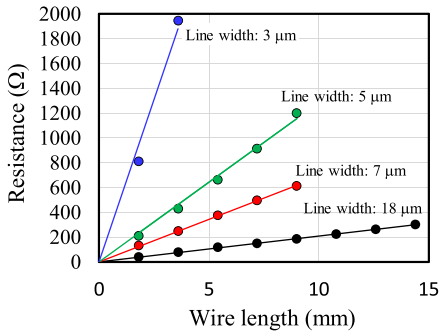


Fig. 10. Relationship between the resistances and wire lengths formed on a PDMS before removal from the second handler.

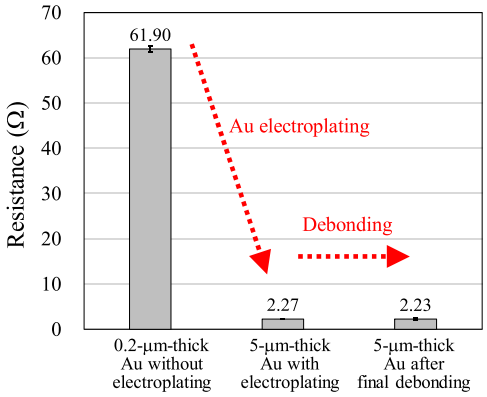


Fig. 11. Resistances formed on FlexTrate: 200-nm-thick Au wires and 5-μm-thick Au wires before/after debonding.

the adjacent dielets. 8-μm-pitch Au wirings (line/space 3.4/4.6 μm) are successfully formed on the array of Si dielets and the surrounding PDMS, as shown in Fig. 9. Fig. 10 shows that excellent linear relationships are obtained by I–V measurement of the fine Au wirings with the minimum wire width of 3 μm.

In this paper, since wafer-level processing is employed, metal layers can be readily thickened by using wafer-level electroplating. Au electroplating was supported by Electroplating Engineers of Japan Ltd., Kanagawa, Japan. As shown in Fig. 11, the 200-nm-thick Au wire resistances are significantly decreased down to nearly 1/30 when thick Au wires with a

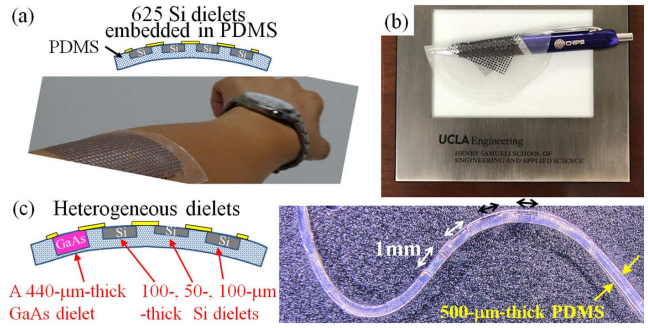


Fig. 12. Photographs of FlexTrate demonstrators. (a) Wearable and (b) rollable 100-μm-thick/1-mm-sqaure 625 Si dielets embedded in PDMS, and a cross-sectional image of PDMS embedding heterogeneous dielets composed of (c) GaAs and Si with various thicknesses.

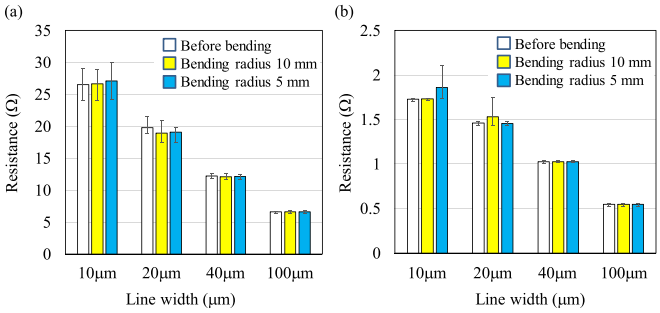


Fig. 13. Resistance comparison between before and after 1000-cycle bending with curvature radius of 10 and 5 mm for 100-, 40-, 20-, and 10-μm-width Cu wirings formed on Si dielets embedded in PDMS: Cu thicknesses are (a) 600 nm and (b) 5 μm.

thickness of approximately 5 μm are used. The low resistances are kept even after final PDMS removal from the second handler, as shown in Fig. 11.

The FlexTrate embedding large numbers of the 1-mm-sqaure Si dielets in the PDMS can be attached on the curved profiles such as the human arm, Fig. 12(a), and a pen, Fig. 12(b). Fig. 12(c) shows the cross section of a FlexTrate embedding heterogeneous dielets composed of a 440-μm-thick GaAs dielets and three 1-mm-sqaure Si dielets with various thicknesses of 50 and 100 μm. As seen from Fig. 12(a)–(c), rigid dielets can be bent in any chosen direction by the flexible PDMS between the dielets. These FlexTrate with the heterogeneous dielets embedded in the biocompatible PDMS can be implanted into the human body including the brain.

D. Bendability

The bendability of the FlexTrate having embedded dielets is evaluated with an endurance testing system: tension-free U-shaped folding tester (DLDMLH-FS/Yuasa). Fig. 13 shows the resistances of FlexTrate test vehicles having 600-nm- and 5-μm-thick Cu wirings formed on the PDMS embedding 1-mm^2 Si dielets with a thickness of 100 μm. Cu wirings are required for FHE desiring low-resistance applications such as wearable sensors, whereas Au/Ti wirings are desirable for implantable use due to their high biocompatibility. Four-point probe patterns are used for the resistance evaluation. The

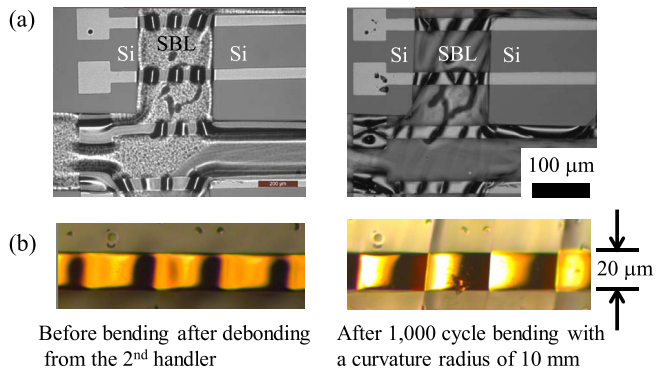


Fig. 14. (a) SEM images and (b) enlarged photomicrographs of 600-nm-thick Cu wirings formed on FlexTrate with dielets embedded in PDMS before and after bending.

Cu interconnections are 15 mm long and 100, 40, 20, and 10 μm in width. The resistances are compared before and after 1000 bending with a curvature radius of 10 mm and the subsequent additional 1000 bending with the radius of 5 mm. As a result, both the Cu interconnects between the neighboring dielets embedded in the PDMS are still connected without delamination. The resistance changes are within 2% on average after the sequential bending. In contrast, 200-nm-thick Cu wirings hardly survive the thermal debonding process. From these results, the wide ranges of Cu thicknesses are turned out to be applicable for the FlexTrate.

Comparison of some of state-of-the-art FHE under stress is summarized in [40]. The 20-μm-thick Si fabricated by dicing before grinding and 15-μm-thick Si fabricated by controlled spalling techniques exhibit the reliable curvature radii of 20 mm [40] and 6.3 mm [41]. These studies show good CMOS characteristics under the bending conditions; however, repeated bending is not evaluated. Our new FHE "FlexTrate" achieves high durability of 2000 cycle bending in total with curvature radii of 10 and 5 mm as mentioned above.

Fig. 14(a) and (b) shows the SEM images and photomicrographs of the test vehicles before and after bending with the radius of 10 mm. The left image is captured just after debonding from the second handler at 180 °C. Several wrinkles are observed between the dielets even before bending when the 600-nm-thick Cu wirings are employed. The cracks resulted from the wrinkles are probably formed in the brittle SU-8 on the SBL Parylene-C that is plastically deformed. However, the two polymers SU-8/ Parylene-C formed on the PDMS mitigate the stresses applied when thermal debonding and mechanical repeated bending. On the other hand, compared to 600-nm-thick Cu wirings, half of the 10- and 20-μm-wide Cu wirings with the thickness of 5 μm are working after additional bending of the curvature radius of 2.5 mm. In addition, the 40- and 100-μm-wide Cu wirings exhibit almost the same resistances as the initial values when the wire is thickened. It should be stressed that FlexTrate fabrication process has a wide margin for wire thickness.

From simulation results using ANSYS, it is found that larger interdielet spaces and thicker dielets give smaller stresses to the PDMS underneath metal wires without SBL. We are still on going the stress mapping research of FlexTrate and working on the stress simulation analyses of the embedded dielets and wirings formed on SBL.

IV. Conclusion

We have integrated FlexTrate using the new technology platform based on advanced die-first FOWLP for next-generation FHE. The 3-μm-feature Au wirings are successfully formed on the PDMS in which Si dielets are embedded and planarized. High coplanarity, low die shift, and high repeated bendability are achieved by FlexTrate. The fabrication process of FlexTrate with 10-μm-feature Cu interconnects exhibits a wide margin for wire thickness in 1000 cycle repeated bending with a curvature radius of 5 mm or less. This heterogeneous integration using monocrystalline Si dielets embedded in flexible substrates enables high-performance and scalable flexible device systems with high-density interconnects to create highly integrated wearable and implantable electronics.

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