IEEE-CPMT Special Topic: Advances in Tools/Techniques for Microelectronic Package Failure Analysis

RECENT advances in microelectronic package technologies such as 2.5-D, 3-D, and wafer-level packaging have delivered rapid breakthroughs in the semiconductor industry by providing better device performance, power efficiency, and cost reduction. Reduction of feature sizes for these technologies has also required advancements in tools and techniques necessary to observe and investigate failures seen in these complex devices. The complexity of these devices has challenged researchers to modify conventional tools and invent smart methods for enhanced fault isolation (FI) and failure analysis (FA) capabilities. This Special Topics Section is a collection of various fault isolation and failure analysis advances made by research groups active in this area. Dissemination of all this research in one Special Topics Issue will greatly benefit the researchers working in the area of failure analysis of semiconductor devices. We capture the highlights of this Special Topic below.

The first two articles focus on a general review in the area of fault isolation and failure analysis pertinent to 2.5-D/3-D packaging architecture. De Wolf and her colleagues at IMEC provide a focused review of challenges in failure analysis of 3-D devices. In their paper, they start with a general introduction of different TSV processing options in current use in the industry and lay out the challenges that these options bring with them. This paper provides an overview of failures that can be expected in 3-D technology and lists the potential failure analysis techniques that can be applied to find these failures, along with the related challenges. Boit and Scholz at Technische Universität Berlin, Berlin, Germany, provide a complementary perspective to the first article by discussing the readiness of contactless fault isolation and discuss the challenges for fault isolation that come with heterogeneous integration. The subsequent articles take a deeper dive in FI-FA challenges and capture specific areas in more detail.

Viswanath Ravi and colleagues at Intel Corporation present details about advances in lock-in tomography (LIT) and its use in performing noncontact, nondestructive fault isolation. They discuss the details of fault isolation using the LIT technique on 3-D packages and cover the challenges of obtaining depth accuracy in devices with multiple defects. They also present real cases that utilize LIT and details of their understanding using numerical analysis. Brand and Altmann from Fraunhofer Institute, Germany, also touch upon LIT along with photoemission and time-resolved gigahertz acoustic microscopy as fault isolation tools for nondestructive defect localization in TSVs. They present their work utilizing thermal imaging by thermography in combination with photoemission microscopy to precisely locate the defect creating electrical shorts in the 3-D stack. They also discuss the important area of filling defects of TSV and present their acoustic gigahertz-microscopy work for inspection and integrity of TSVs. This approach has helped them characterize voids in TSV region with better sensitivity compared to conventional acoustic imaging.

Schmidt from Carl Zeiss, Oberkochen, Germany, discusses the importance of utilizing 3-D X-ray imaging for failure analysis of semiconductor packaging. He discusses the recent advancements in X-ray technology utilizing Fresnel zone plate objectives to demonstrate the capability to image Cu layers in silicon back end with nanometer resolution. As the complexities in packaging increase with wide adoption of 2.5-D and 3-D packaging, it is important to explore options that can provide alternate approaches to understand reliability risks; Prisacaru and colleagues at Bosch share their work where piezoelectric sensors are implemented in the devices to understand *in situ* failures. They also discuss an algorithm to effectively handle the data obtained from these sensors. Wu and Han from the University of Maryland, College Park, MD, USA, discuss the advancements in the analysis of thermal deformation of fan-out wafer-level packaging (FO-WLP) using real-time Moiré interferometry. These advancements have enabled them to document the global and local behavior of an FO-WLP while it is subjected to a controlled thermal excursion.

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