Interposer Power Distribution Network (PDN) Modeling Using a Segmentation Method for 3-D ICs With TSVs

Kiyeong Kim, Jong Min Yook, Junchul Kim, Heegon Kim, Junho Lee, Kunwoo Park, and Joungho Kim, *Member, IEEE*

***Abstract*— In this paper, we propose models for large-sized silicon interposer power distribution networks (PDNs) and through silicon via (TSV)-based stacked grid-type PDNs using a segmentation method. We model the PDNs as distributed scalable resistance (R), inductance (L), conductance (G), and capacitance (C)-lumped models for an accurate estimation of the PDN impedance, including PDN inductance and wave phenomena such as the mode resonance at the high end of the frequency range. For this estimation, it is necessary to accurately model all transmission line (TL) sections that form the PDNs using a conformal mapping method and a phenomenological loss equivalence method (PEM). After modeling the individual TL sections, all the TL sections are connected based on a segmentation method, which is a matrix calculation method. The segmentation method accelerates the calculation speed for the PDN impedance estimation. The proposed models are successfully validated by simulations and measurements in the frequency range 0.1–20 GHz. Using the proposed models, we estimate and analyze the impedance curves of the interposer PDN and TSV-based stacked grid-type PDN with respect to the variations in the horizontal area of the interposer PDN and the number of power/ground TSVs in TSV-based stacked grid-type PDNs, respectively.**

***Index Terms*— Conformal mapping method, interposer power distribution network (PDN), phenomenological loss equivalence method (PEM), segmentation method, through silicon via (TSV)-based stacked grid-type PDN.**

I. Introduction

CURRENTLY, the realization of high-speed integrated-circuit (IC) systems with wider bandwidths, multifunctionality, and better electrical performance has been a continual challenge. Three-dimensional ICS based on through silicon via (TSV) connections and silicon interposers have attracted substantial attention as an ultimate solution for achieving this end goal [1]–[4]. The demand for wider bandwidths and multifunctionality has fueled the considerable increase in the number of I/O drivers in ICs. Therefore, to make the I/O signals transferable to other ICs, TSVs and silicon interposers are used [5]. TSV is a vertical interconnection passing through a silicon substrate. Because of the merit of the vertical interconnection, many I/O signals escape through TSVs, penetrating the silicon substrate of ICs. A silicon interposer is a newly developed package device for interconnection and power transfer. It includes TSVs and metal layers fabricated during the chip fabrication process. Compared with a TSV, a silicon interposer can support not only the vertical interconnections through the TSV but also the horizontal interconnections with the fine metal pitch realized during the chip fabrication. Because of its significant merits in terms of interconnection, the interposer has attracted much attention in 3-D-ICs that have difficulties with escaping I/O signals. Another important function of TSVs and silicon interposers is the supply of power to ICs in 3-D-ICs.

When power is supplied to ICs in 3-D-ICs with the circuit activation, a switching current passes through the power distribution networks (PDNs), including the power/ground (P/G) TSVs and the interposer PDN in the silicon interposer. At this time, the current encounters the impedance of the PDNs. Because of the encounter, simultaneous switching noise (SSN) is generated on the PDNs [6]–[9]. Because SSNs can critically degrade the performance and reliability of ICs, it is important to estimate the PDN impedance as the main criterion to approximate SSNs on the PDNs [6], [7]. When estimating the impedance of PDNs hierarchically stacked in 3-D-ICs based on 3-D electromigration (EM) simulators, it is difficult to estimate the impedance because of the long simulation time and the use of many computational resources, which are necessary because of the high aspect ratio of the PDN structures [9], [12]. Because of the limitations of 3-D EM simulators, the model-based impedance estimation has been used as an effective method to estimate the impedance of PDNs in 3-D-ICs [10]–[12].

In this paper, we focus on the modeling method for the large-sized interposer PDNs in 3-D-ICs. In 3-D-ICs, several on-chip PDNs are stacked on the interposer PDN through P/G TSVs, as shown in Fig. 1. Through the TSV connection, the

Manuscript received January 15, 2013; revised May 29, 2013; accepted July 5, 2013. Date of publication August 29, 2013; date of current version October 28, 2013. This work was supported in part by the IT R&D program of MKE/KEIT under Grant KI001472, Wafer Level 3D IC Design and Integration, in part by the IT R&D program of MKE/KEIT under Grant 10039232, Core Process Development of the 3D Integration for System IC, and in part by the Smart IT Convergence System Research Center funded by the Ministry of Education, Science and Technology as Global Frontier Project under Grant STRC-2011-0031863. Recommended for publication by Associate Editor A. Maffucci upon evaluation of reviewers' comments.

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Digital Object Identifier 10.1109/TCPMT.2013.2276050

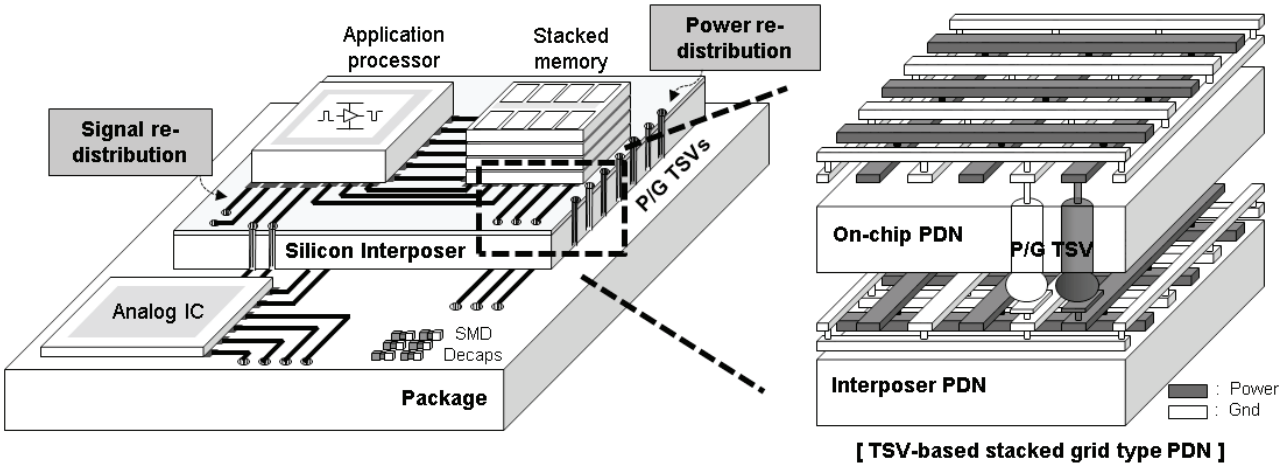

Fig. 1. Interposer for a 3-D-IC with TSVs. The interposers play important roles in signal and power distribution to the circuits within 3-D-ICs through TSVs and a redistribution layer in the interposers. Because of the 3-D stacking through the TSV connection, two grid-type PDNs, an on-chip PDN, and an interposer PDN are hierarchically connected and become a TSV-based stacked grid-type PDN.

on-chip PDNs and interposer PDN, which are the grid-type PDNs, are hierarchically connected and become a TSV-based stacked grid-type PDN. We also address the modeling method for the TSV-based stacked grid-type PDN in 3-D-ICs.

Because of the metal density rule of the chip fabrication process, interposer PDNs in silicon interposers are formed as grid-type PDNs with entangled P/G lines. For the same reason, the on-chip PDNs are also formed as grid-type PDNs. The difference between the on-chip PDN and interposer PDN is their PDN size. Because the interposer functions as a stanchion and power supplier for stacked ICs, the horizontal area of the interposer PDN is larger than that of the on-chip PDN.

Because of the larger PDN size, the different impedance characteristics are revealed in the impedance of the interposer PDN. To examine the impedance of the interposer PDN, we simulate a 2 × 2 mm interposer PDN using a 3-D EM simulator CST Microwave Studio (CST MWS). The biggest differences revealed in the simulated impedance curve of the interposer PDN shown in Fig. 2 are the remarkable increase in PDN inductance and the generation of the mode resonance peak compared with the impedance characteristic of the on-chip PDN conventionally represented with its resistance (R) and capacitance (C). In particular, the mode resonance at 14.6 GHz is a distinct feature of the large-sized interposer PDN. We focus on this parallel resonance because the critical SSN at high frequencies can be generated through this high impedance peak caused by the mode resonance.

To accurately estimate the impedance of the interposer PDN based on the PDN model, the model should include distributed resistance, inductance (L), conductance (G), and capacitance (RLGC)-lumped components according to the variation in PDN structure. Additionally, the model for large-sized interposer PDNs should be able to estimate the PDN inductance and mode resonance at arbitrary port positions.

Several papers have been published that propose a RLGC-lumped model for grid-type PDNs [10], [11]. One particular study [10] has proposed a distributed scalable RLGC-lumped model. The model, however, consists of

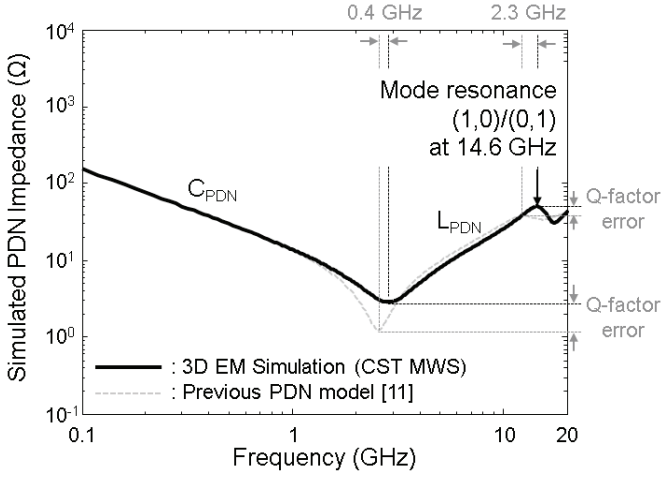

Fig. 2. Impedance curves of a 2 × 2 mm interposer PDN on the silicon substrateare represented. The solid line is obtained from CST MWS. The gray dashed line is obtained from the previous PDN model [11].

frequency-independent resistance and inductance (R and L). Additionally, it does not include the silicon substrate, which is a substantial weakness when modeling interposer PDNs because of the proximity between the metal and silicon substrate in the silicon interposer. Kim *et al.* [11] proposed a distributed scalable RLGC-lumped model based on a segmentation method. However, there are several limitations in the RLGC-lumped model. When the capacitance (C) of the grid-type PDN is estimated, the equations for the capacitance did not consider the boundary condition because the equations are derived under the assumption that the ground is infinite. This results in a capacitance error when the model is applied to the PDN structure, which is critically affected by the boundary condition, such as the case in which the power line is close to the ground line. The R and L in the model are also frequency-independent. Using this frequency-independent model, the PDN inductance and mode resonance on large-sized interposer PDNs cannot be accurately modeled. In Fig. 2,

the PDN impedance curves are obtained from the 3-D EM simulation by CST MWS (black solid line) and the previous model (gray dashed line) [11], and the two curves have similar characteristics. However, the previous model has a difficult time accurately estimating the PDN inductance, mode resonance, and Q-factor at the resonance frequency of the large-sized interposer PDN.

In this paper, we proposed distributed scalable RLGC-lumped models for the large-sized interposer and TSV-based stacked grid-type PDN based on a segmentation method. First, to model the interposer PDN, the PDN is split into several transmission line (TL) sections [11]. We model these TL sections as RLGC-lumped models. In the models, the capacitance and conductance (C and G) is calculated using a conformal mapping method [13] and considering the boundary condition. In the C and G modeling, to consider the silicon substrate effect, which is important, the capacitance caused by the silicon substrate is calculated by applying the conformal mapping method to the silicon substrate. The frequency-dependent calculation of the R and L is performed using a phenomenological loss equivalence method (PEM) [14]. After the lumped modeling of the TL sections, the interposer PDN is consequentially modeled through the connections between all the TL sections using a segmentation method [11]. Additionally, we model the TSV-based stacked grid-type PDN by connecting the proposed models for the interposer PDNs with the RLGC-lumped models of P/G TSV pairs [11] in a hierarchical order with a segmentation method. The proposed models for the interposer and TSV-based stacked grid-type PDN are based on a matrix calculation using a segmentation method without any circuit simulator. Therefore, we can achieve a fast calculation speed and save the computational resources required for the estimation of the PDN impedance.

To verify the proposed models for the interposer PDN and TSV-based stacked grid-type PDN, we simulated an interposer PDN on the silicon substrate with sizes of 2 mm $\times$ 2 mm and measured the fabricated double-stacked grid-type PDN, respectively. The proposed models for the interposer PDN and TSV-based stacked grid-type PDN have been successfully verified by the 3-D EM simulations using CST MWS and the measurement of the fabricated TSV-based stacked grid-type PDN in the frequency range of 0.1–20 GHz. Additionally, we have confirmed the efficiency of the proposed PDN models by comparing their simulation times with 3-D EM simulations with CST MWS. Therefore, we can conclude that the proposed models are accurate and efficient models for predesigning the PDNs.

Using these verified models, we estimated and analyzed the impedance curve of the interposer PDN with respect to the variations in the horizontal area of the interposer PDN. Additionally, we estimated and analyzed the impedance curve of the TSV-based stacked grid-type PDN with respect to the variation in the number of P/G TSVs in the double-stacked grid-type PDN, which are the main design issues of the PDN in 3-D-ICs. Through these estimations and analyses, we suggested the design guide of the interposer PDN and TSV-based stacked grid-type PDN in 3-D-ICs.

II. Proposal of Models for Interposer PDNs and TSV-Based Stacked Grid Type PDNs

In this section, the models for the interposer PDN and TSV-based stacked grid-type PDN are proposed based on a segmentation method, a conformal mapping method, and a PEM. The key is to accurately model those PDNs as distributed RLGC-lumped models to include the accurate capacitances and frequency-dependent resistances and inductances, which are obtained from a conformal mapping method and a PEM, respectively. If done correctly, the impedances of the interposer PDN and TSV-based stacked grid-type PDN can be accurately modeled up to a high frequency range. The proposed models have the advantage of being based on the scalable equations with structural and material parameters. The use of scalable equations provides physical insights into the effects of varying those parameters. Additionally, the matrix-based impedance calculation using a segmentation method accelerates the calculation speed for the efficient impedance estimation.

A. Modeling Method of Grid-Type PDNs

The on-chip and interposer PDN are grid-type PDNs because of the metal density rule, as shown in the right side of Fig. 1. In particular, in the interposer, the PDN is located directly above the substrate because only a few metallic layers can be fabricated. Therefore, we set up the target interposer PDN with two metal layers over a silicon substrate. Additionally, we assume that the metal width and the pitch between a power line and an adjacent ground line are fixed. Under these assumptions, the interposer PDN can be decomposed into certain repetitive PDN structures with a perfect magnetic conductor (PMC) on all four horizontal boundaries, called unit cells [12]. By including PMC boundaries, we can include the effect from the other adjacent unit cells.

Once we have a model of the unit cell, the whole interposer PDN can be modeled through the connection between the face-to-face ports of the adjacent unit cell models based on a segmentation method [11]. To model the unit cell, the cell is split into several TL sections in the x- and y-directions, as shown in Fig. 3.

In the next step, the TL sections are modeled as RLGC-lumped models. It is important to accurately model these sections because PDN impedance is directly determined by the connection between these section models. This modeling method, which is based on structural decomposition, has the advantage that we can model the PDN seen by the wave while it moves in the PDN. Thus, the bandwidth and accuracy of the distributed RLGC-model is greater than other simple lumped models. Additionally, the mode resonance on the interposer PDN can be estimated by this model. However, to model the interposer PDN, thousands of TL sections should be connected to each other. Thus, when each TL section model contains a small modeling error, the modeling of the whole interposer PDN can contain substantial errors. Therefore, accurate modeling of TL sections is most important. Thus, a conformal mapping method and a PEM are mainly used to extract the C and G and R and L of the TL sections, respectively.

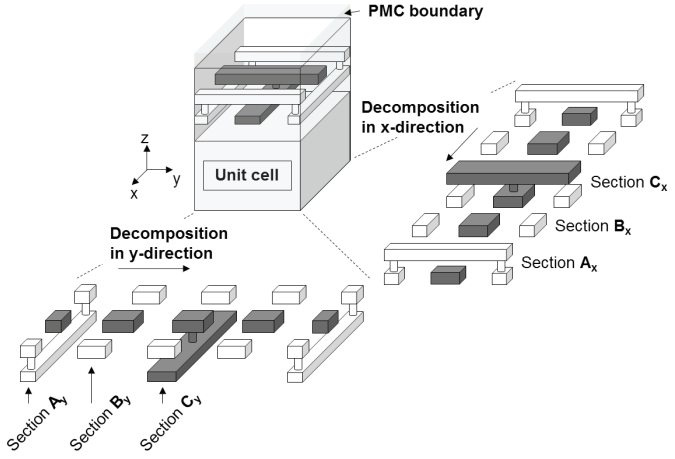

Fig. 3. Decomposition of a unit cell in the x- and y-directions into the decomposed TL sections, such as sections A_x, B_x, and C_x.

A conformal mapping method is an angle-preserving method. For the capacitance estimation, the Schwarz–Christoffel transformation, which is a conformal transformation to transform the upper half-plane onto the interior of a simple polygon [15], is used. Through the Schwarz–Christoffel transformation, we can estimate the capacitance of the TL sections given their PMC boundary condition by transforming the partitions of the TL sections into the parallel plate [15]. Then, we can easily estimate their capacitance by the capacitance equation for two parallel plates, including a dielectric material between them.

Electromagnetic fields penetrate into the imperfect conductors while they move along TL sections. The field penetrations result in resistance (R) and internal inductance (L_{int}). Because of the shallow penetration caused by the skin effect, the R and L are increased and decreased, respectively, as the frequency increases [14]. The internal impedance variation, which is represented as the variation in the resistance and internal inductance, changes the transmission characteristics, such as the characteristic impedance and complex propagation constant. The impedance of the interposer PDN is intrinsically determined by these transmission characteristics of the TL sections that form the interposer PDN. The mode resonance on the interposer PDN is directly associated with the propagation constants of the TL sections because the wavelength that determines the mode generation is determined by the propagation constants [20]. Therefore, it is important to include the frequency-dependent variation in the R and L in the section models. Accordingly, a PEM is used to model the frequency-dependent R and L of the TL sections.

To calculate the internal impedance of the TL sections, the current distribution must be known throughout the entire conductor. The purpose of the PEM is to phenomenologically transform the TL sections into single equivalent strips and then analyze the equivalent strips using the surface impedance for a finite conductor thickness [14]. The internal impedance can be calculated using the equivalent strip width ($W_e = 1/G$), equivalent thickness (t_e = AG), and the surface impedance of a flat-plane conductor with finite thickness, as represented

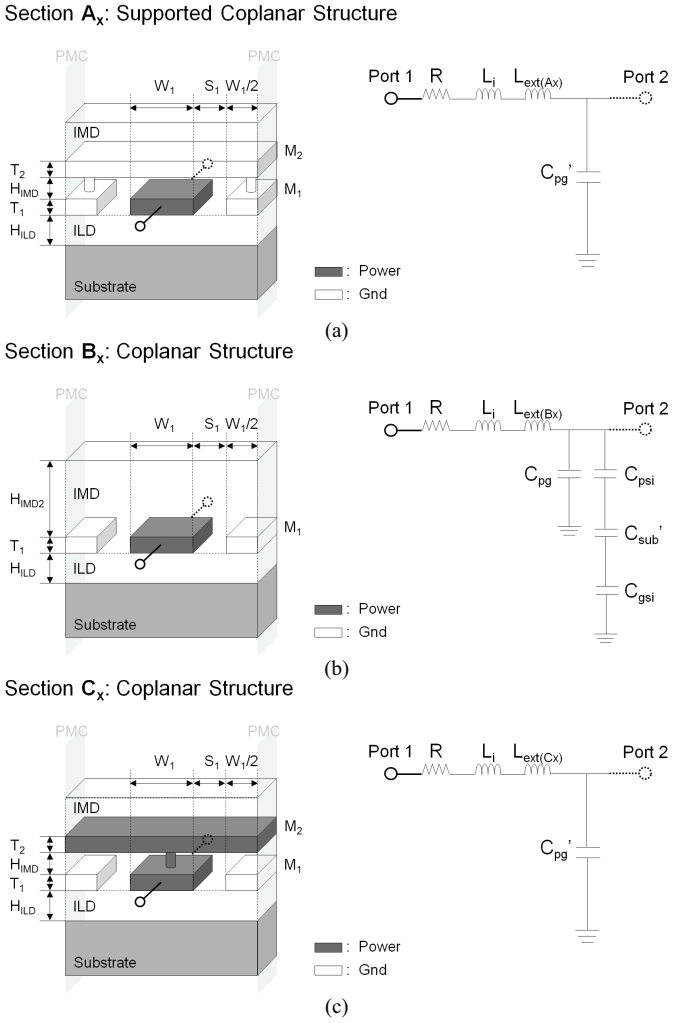

Fig. 4. (a) Structure and RLGC-lumped model of section A_x. (b) Structure and RLGC-lumped model of section B_x. (c) Structure and RLGC-lumped model of section C_x.

in (1) [14]

$$Z_i = R + j\omega L_i = Z_s / W_e \coth\left(\frac{1+j}{\delta} t_e\right) = Z_s G \coth\left(\frac{1+j}{\delta} AG\right). \quad (1)$$

In (1), Z_s is the surface impedance of the conductor medium. G and A are the geometric factor and cross-sectional area of a TL section, respectively. The usefulness of a PEM is due to its simple calculation of Z_s, G, and A. With the internal impedance (Z_i) obtained from a PEM, we can calculate the frequency-dependent resistance (R) and internal inductance (L_i) caused by the current distribution in the metal of the TL sections.

By applying a conformal mapping method and a PEM to extract the RLGC components of the TL sections, all the TL sections shown in Fig. 3 can be modeled as RLGC-lumped models. In this paper, because of the similarity in the modeling method for the TL sections, we only focus on the modeling of sections such as A_x, B_x, and C_x, as shown in Fig. 4.

The structure of section A_x shown in Fig. 4 (a) is a supported coplanar waveguide. All RLGC values obtained from

TABLE I
MODEL PARAMETERS WITH THEIR SYMBOLS FOR A PROPOSED SCALABLE ELECTRICAL MODEL OF AN INTERPOSER PDN, WHICH INCLUDES STRUCTURAL AND MATERIAL PARAMETERS

	Parameter	*Description*
On-chip PDN	W_1	Metal width of M_1 metal
	W_2	Metal width of M_2 metal
	S_1	Space between the power line and ground line on the M1 metal
	S_2	Space between the power line and ground line on the M2 metal
	P_1	Pitch between the power line and ground line on the M1 metal
	P_2	Pitch between the power line and ground line on the M2 metal
	H_{ILD}	Height of the ILD layer between the M1 metal and silicon substrate
	H_{IMD}	Height of partition 3 between the M2 metal and M1 metal
	T_1	Thickness of the M1 metal
	T_2	Thickness of the M2 metal
	ε_{Sub}	Relative permittivity of the substrate
	ε_{ILD}	Relative permittivity of the ILD
	ε_{IMD}	Relative permittivity of the IMD
	σ_{Sub}	Conductivity of the substrate

the following equations are given as values per unit length. To model section A_x, we first calculate the air-filled capacitance ($C_{\text{Ax}}^{\text{air-filled}}$) of section A_x. In the condition that the space (S_1) is wide and $W_1 \gg H_{\text{ILD}}$, the supported coplanar waveguide can be considered to be a microstrip line [15]. Therefore, the air-filled capacitance ($C_{\text{Ax}}^{\text{air-filled}}$) of section A_x is calculated by (2) [15], which is the equation for the capacitance caused by all faces (top face, bottom face, and two side faces) of the microstrip line obtained from the conformal mapping-based empirical approach

$$C_{\text{Ax}}^{\text{air-filled}} = \varepsilon_0\left(\frac{W_1}{H_{\text{IMD}}} + 0.77 + 1.06\left(\frac{W_1}{H_{\text{IMD}}}\right)^{0.25} + 1.06\left(\frac{T_1}{H_{\text{IMD}}}\right)^{0.5}\right). \quad (2)$$

The next step is the extraction of the external inductance (). $L_{\text{ext(Ax)}}$ is calculated by (3) [16]

$$L_{\text{ext(Ax)}} = \frac{1}{c^2 C_{\text{Ax}}^{\text{air-filled}}} \quad (c\text{: speed of light } (c = 3 \times 10^8 \text{m/s})). \quad (3)$$

The third step is the extraction of the internal impedance (Z_i) based on a PEM. First, the geometric factor (G_{Ax}) of section A_x should be calculated. The geometric factor of section A_x can be obtained when we know the external inductance [$L_{\text{ext(Ax)}}(W_1, h_{\text{IMD}}, T_1)$] of section A_x. The geometric factor represents the surface current distribution of section A_x. Because the external magnetic flux is proportional to the surface current density, the increment of the external inductance is associated with the distribution of the current density on section A_x. The geometric factor is obtained from the derivative of the external inductance and some algebraic manipulations [14] based on the recession of the conducting

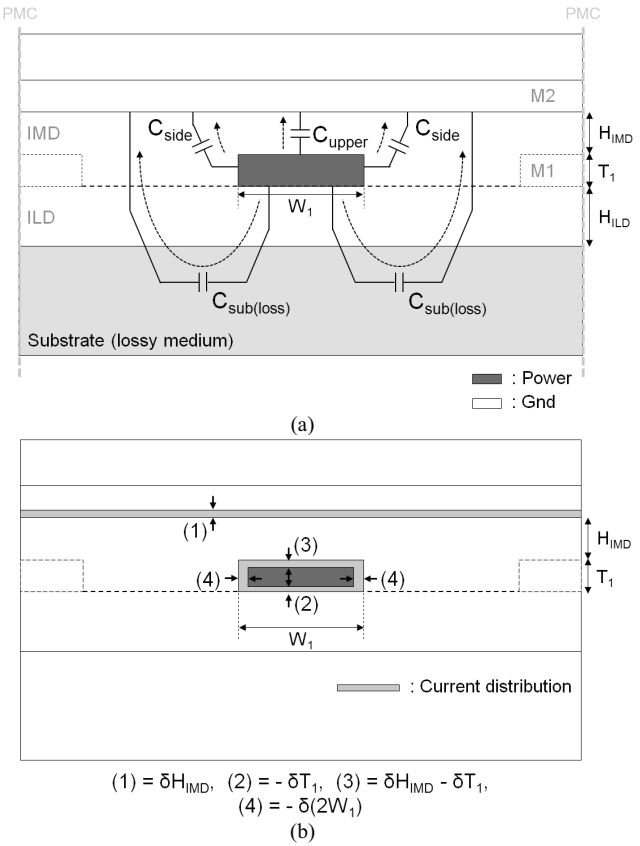

Fig. 5. (a) All capacitances (Cupper, Cside, and Csub) are shown according to the position of the electric field generatedin section A_x. (b) Current distribution caused by the field penetration and physical parameter variation according to the current distribution.

walls shown in Fig. 5(b), as presented in (4).

$$G_{\text{Ax}} = \frac{1}{\mu}\sum_m\left(\frac{\partial L_{ext(Ax)}(W_1, H_{\text{IMD}}, T_1)}{\partial n_m}\right) = \frac{1}{\mu}\left[\left(\frac{\partial L_{ext(Ax)}}{\partial H_{\text{IMD}}}\right)_{(1)} + \left(-\frac{\partial L_{ext(Ax)}}{\partial T_1}\right)_{(2)} + \left(\frac{\partial L_{ext(Ax)}}{\partial H_{\text{IMD}}} - \frac{\partial L_{ext(Ax)}}{\partial T_1}\right)_{(3)} + \left(-2\frac{\partial L_{\text{ext(Ax)}}}{\partial W_1}\right)_{(4)}\right]. \quad (4)$$

In (4), the number m is the number of metal faces [(1), (2), (3), and (4) in Fig. 5(b)], in which we consider the shallow penetration.

Using this geometric factor, we can calculate the internal impedance ($Z_{i,\text{pwr}}$ and $Z_{i,\text{gnd}}$) of the P/G line of section A_x using (5) [16]

$$Z_{i,\text{pwr}} = Z_s G_{\text{Ax}} \coth\left(\frac{1+j}{\delta} A_{\text{pwr}} G_{\text{Ax}}\right)$$
$$Z_{i,\text{gnd}} = Z_s G_{\text{Ax}} \coth\left(\frac{1+j}{\delta} A_{\text{gnd}} G_{\text{Ax}}\right)$$

where

$$Z_s = (1+j)\frac{1}{\sigma\delta}$$
$$A_{\text{pwr}} = W_1 T_1, \quad A_{\text{gnd}} = 10 H_{\text{IMD}} T_2. \tag{5}$$

In $Z_{i,\text{gnd}}$ of (5), we use $10H_{\text{IMD}}$ as the width of the current density because the current predominantly flows in the area $A_{\text{gnd}}(=10H_{\text{IMD}}\text{T}_2)$. From these internal impedances, we can calculate the resistance (R) and internal inductance (L_i) of section A_x, as presented in (6) [16]

$$R = \text{Re}(Z_{i,\text{pwr}} + Z_{i,\text{gnd}}), \quad L_i = \frac{1}{\omega}\text{Im}(Z_{i,\text{pwr}} + Z_{i,\text{gnd}}). \tag{6}$$

Finally, to calculate the capacitance of section A_x, we split the capacitance into subcapacitances, such as C_{upper}, C_{side}, and $C_{\text{sub(loss)}}$, as shown in Fig. 5(a), because this separation is needed to extract the substrate effect, such as $C_{\text{sub(loss)}}$. All subcapacitances are calculated based on a conformal mapping method. C_{upper} is the capacitance only caused by the electric field between the top of the M_1 metal and the bottom of the M_2 metal, as presented in (7) [13]

$$C_{\text{upper}} = \varepsilon_0 \varepsilon_{\text{IMD}} \left(\frac{W_1}{H_{\text{IMD}}} + \frac{4\ln(2)}{\pi} \right). \tag{7}$$

C_{side} is the capacitance caused by the electric field between the side of the M_1 metal and the bottom of the M_2 metal, as presented in (8) [13]

$$C_{\text{side}} = \frac{\varepsilon_0 \varepsilon_{\text{IMD}}}{2} M(k(T_1, H_{\text{IMD}})). \tag{8}$$

In (8), k is a parameter related to the geometrical dimensions T_1 and H_{IMD}. M is a function of k. The equations for calculating these parameters have already been introduced in [13].

As shown in Fig. 5(a), the electric field between the bottoms of the M_1 metal and M_2 metal penetrates the substrate. When the substrate is a loss-inducing medium, such as a silicon substrate, it is necessary to model the dielectric loss of the substrate. To model the dielectric loss of the substrate, we have to model the capacitance that is generated in the substrate itself. The capacitance is calculated using the effective dielectric constant, which includes the conductivity of the substrate.

The microstrip line is a symmetrical structure. When we calculate the capacitance of the line, we assume that there is a PMC boundary on the center of the line. As shown in Fig. 6, the half structure of the microstrip line can be transformed into parallel plates by Wheeler's transformation [17]. Through this transformation, we can easily calculate the capacitance of the microstrip line using the equation for calculating the capacitance between parallel plates. The capacitance caused by the electric field penetrating the inter-metal dielectric (IMD) (shaded area in the right side of Fig. 6) is predominantly calculated as C_{upper} and C_{side}. To calculate $C_{\text{sub(loss)}}$, we focus on the capacitance on the bold box in the right side of Fig. 6.

In the bold box, there are two dielectric materials, the inter-layer dielectric (ILD) and substrate. The substrate material, such as the silicon, can include a high conductivity. In the case, that one substrate is loss-free (ε_{ILD}) and the other is loss-including ($\varepsilon_{\text{Sub}} + \frac{\sigma_{\text{Sub}}}{j\varepsilon_0\omega}$), the effective dielectric constant is calculated according to (9) [18]

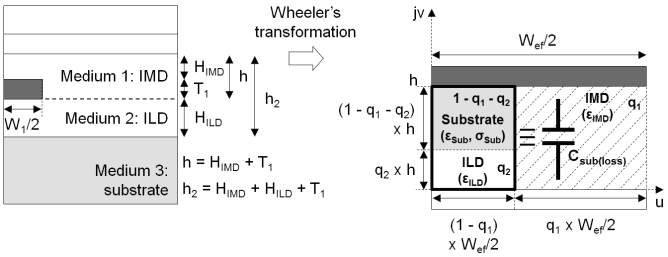

Fig. 6. Half of the microstrip line is transformed into the parallel plate by Wheeler's transformation to calculate the capacitance $C_{\text{sub(loss)}}$ caused by the electric field penetrating the substrate.

$$\tilde{\varepsilon}_{\text{eff}} = \varepsilon_{\text{eff}} + \frac{\Delta\varepsilon}{1+j\omega\tau} \tag{9a}$$
$$q_{\text{lossy}} = \frac{(1-q_1-q_2)h}{q_2 h + (1-q_1-q_2)h} \tag{9b}$$
$$\varepsilon_{\text{eff}} = \frac{\varepsilon_{\text{ILD}}\varepsilon_{\text{Sub}}(1+2q_{\text{lossy}})}{q_{\text{lossy}}(\varepsilon_{\text{ILD}}+\varepsilon_{\text{Sub}})+\varepsilon_{\text{Sub}}} \tag{9c}$$
$$\Delta\varepsilon = \frac{q_{\text{lossy}}\varepsilon_{\text{ILD}}\varepsilon_{\text{eff}}}{(1+q_{\text{lossy}})\varepsilon_{\text{Sub}}} \tag{9d}$$
$$\tau = \frac{q_{\text{lossy}}(\varepsilon_{\text{ILD}}+\varepsilon_{\text{Sub}})+\varepsilon_{\text{Sub}}}{(1+q_{\text{lossy}})\sigma_{\text{Sub}}}. \tag{9e}$$

In (9a)–(9e), $\tilde{\varepsilon}_{\text{eff}}$ is the complex dielectric constant of the mixture and ε_{eff} is the effective dielectric constant at high frequencies. $\Delta\varepsilon$ and τ are the dielectric strength of the interfacial polarization and the relaxation time of the polarization, respectively. q_{lossy} is the filling factor of the substrate and is calculated by the ratio of the area of the substrate to the total area of the mixture. In (9b), there are two filling factors q_1 and q_2 that are the filling factors of IMD and ILD, respectively. q_1 and q_2 are the functions of W_1, h, and h_2, as represented in [17].

Using the complex dielectric constant ($\tilde{\varepsilon}_{\text{eff}}$) of the mixture, we can calculate the capacitance [$C_{\text{sub(loss)}}$] using (10)

$$C_{\text{sub(loss)}} = \tilde{\varepsilon}_{\text{eff}} \frac{\frac{W_{\text{eff}}}{2}(1-q_1)}{h}. \tag{10}$$

Finally, C_{pg} shown in the RLGC-lumped model of Fig. 4(a) is calculated by (11)

$$C'_{\text{pg}} = C_{\text{upper}} + 2C_{\text{side}} + 2C_{\text{sub(loss)}}. \tag{11}$$

The structure of section B_x shown in Fig. 4(b) is a coplanar waveguide. We also follow the modeling steps of section A_x to model section B_x. First, we calculate the air-filled capacitance ($C_{\text{Bx}}^{\text{air-filled}}$) of section B_x. Because of the symmetry of section B_x in the horizontal and vertical axes, we can extract$C_{\text{upper}}^{\text{air-filled}}$ and$C_{\text{side}}^{\text{air-filled}}$ to calculate the air-filled capacitance ($C_{\text{Bx}}^{\text{air-filled}}$) of section B_x.

$C_{\text{upper}}^{\text{air-filled}}$ is the air-filled capacitance caused by the electric fields between the tops of the P/G line bounded by PMC in

section B_x. The capacitance is calculated by (12) [15]

$$k = \cos\left(\frac{(P_1 - S_1)\pi}{2P_1}\right) \tag{12a}$$

$$C_{\text{upper}}^{\text{air-filled}} = \frac{\varepsilon_0}{2}\left(\frac{K(k')}{K(k)}\right). \tag{12b}$$

In (12a) and (12b), $K(k)$ and $K(k')$ are the complete elliptic integral of the first type and its complement, respectively. k and k' are the elliptic modulus and complementary elliptic modulus, respectively. The relationship between k and k' is $k' = \sqrt{1-k^2}$.

$C_{\text{side}}^{\text{air-filled}}$ is the air-filled capacitance caused by the electric fields between the sides of the P/G lines in section B_x. The capacitance is calculated by (13)

$$C_{\text{side}}^{\text{air-filled}} = \varepsilon_0\left(\frac{T_1}{S_1}\right). \tag{13}$$

Using $C_{\text{upper}}^{\text{air-filled}}$ and $C_{\text{side}}^{\text{air-filled}}$, we can calculate the air-filled capacitance ($C_{\text{Bx}}^{\text{air-filled}}$) of section B_x according to (14)

$$C_{\text{Bx}}^{\text{air-filled}} = \frac{1}{\varepsilon_{\text{IMD}}}\left(4C_{\text{upper}}^{\text{air-filled}} + 2C_{\text{side}}^{\text{air-filled}}\right). \tag{14}$$

The external inductance ($L_{\text{ext(Bx)}}$) of section B_x is extracted the same way using (3) and (14).

The geometric factor of section B_x is obtained from the derivative of the external inductance ($L_{\text{ext(Bx)}}$), as presented in (15)

$$\begin{aligned} G_{\text{Bx}} &= \frac{1}{\mu}\sum_m\left(\frac{\partial L_{\text{ext(Bx)}}(T_1, S_1)}{\partial n_m}\right) \\ &= \frac{1}{\mu}\left[\left(-\frac{\partial L_{\text{ext(Bx)}}}{\partial T_1}\right)_{(1)} + \left(-\frac{\partial L_{\text{ext(Bx)}}}{\partial T_1}\right)_{(2)}\right. \\ &\quad \left. + \left(\frac{\partial L_{\text{ext(Bx)}}}{\partial S_1}\right)_{(3)} + \left(\frac{\partial L_{\text{ext(Bx)}}}{\partial S_1}\right)_{(4)}\right]. \end{aligned} \tag{15}$$

Using this geometric factor, we can calculate the internal impedance ($Z_{i,\text{pwr}}$ and $Z_{i,\text{gnd}}$) of the P/G lines using (16)

$$\begin{aligned} Z_{i,\text{pwr}} &= Z_s\left(= (1+j)\frac{1}{\sigma\delta}\right) G_{\text{Bx}} \\ &\quad \times \coth\left(\frac{1+j}{\delta}A_{\text{pwr}}(= W_1T_1)G_{\text{Bx}}\right) \\ Z_{i,\text{gnd}} &= Z_s\left(= (1+j)\frac{1}{\sigma\delta}\right) G_{\text{Bx}} \\ &\quad \times \coth\left(\frac{1+j}{\delta}A_{\text{gnd}}\left(= \frac{W_1}{2}T_1\right) G_{\text{Bx}}\right). \end{aligned} \tag{16}$$

From these internal impedances, we can calculate the resistance (R) and internal inductance (L_i) of section B_x, as presented in (17)

$$\begin{aligned} R &= \text{Re}\left(Z_{i,\text{pwr}} + \frac{1}{2}Z_{i,\text{gnd}}\right) \\ L_i &= \frac{1}{\omega}\text{Im}\left(Z_{i,\text{pwr}} + \frac{1}{2}Z_{i,\text{gnd}}\right). \end{aligned} \tag{17}$$

Finally, to calculate the capacitance of section B_x, we split the capacitance into the subcapacitances C_{upper}, C_{side}, C_{psi}, C_{gsi}, and $C_{\text{sub(loss)}}$ shown in Fig. 11(a).

To calculate C_{upper}, we calculate the capacitance ($C_{\text{upper(IMD)}}$) of the height H_{IMD2} according to (18) [15]

$$\begin{aligned} \varsigma &= ((\exp(P_2\pi/(2H_{IMD2}))/2 - 1)/ \\ &\quad ((\exp(P_2\pi/(2H_{\text{IMD2}}))/2 + 1))^2 \end{aligned} \tag{18a}$$

$$k_1 = sn\left(\frac{S_2}{P_2}K(\varsigma), \varsigma\right) \tag{18b}$$

$$C_{\text{upper(IMD)}} = \varepsilon_{\text{IMD}}\frac{\varepsilon_0}{2}\left(\frac{K(k_1')}{K(k_1)}\right). \tag{18c}$$

Next, by summing $C_{\text{upper(IMD)}}$ and $C_{\text{upper}}^{\text{air-filled}}$, we can calculate C_{upper} according to (19)

$$C_{\text{upper}} = C_{\text{upper}}^{\text{air-filled}} + (\varepsilon_{\text{IMD}} - 1)\frac{\varepsilon_0}{2}\left(\frac{K(k_1')}{K(k_1)}\right). \tag{19}$$

Using (13), we can calculate the capacitance C_{side}, as represented in (20)

$$C_{\text{side}} = \varepsilon_{\text{IMD}}C_{\text{side}}^{\text{airfilled}}. \tag{20}$$

To model the electric fields penetrating the substrate, we use the capacitances C_{psi}, C_{gsi}, and $C_{\text{sub(loss)}}$. In the conventional case that H_{ILD} is in the order of several micrometers and S_1 is in the order of tens of micrometers, there are no electric fields in the ILD itself. We verified this using a conformal mapping method. The verification indicates that all electric fields between the bottoms of the P/G lines penetrate the substrate. Conventionally, the substrate is a loss-inducing medium. To include the dielectric loss in the substrate, we split the electric fields into the electric fields between the power line and substrate, the electric fields between the ground line and substrate, and the electric fields in the substrate. We model the classified electric fields using the capacitances C_{psi}, C_{gsi}, and $C_{\text{sub(loss)}}$, as represented in (21)

$$C_{\text{psi\&gsi}} = \varepsilon_0\varepsilon_{\text{ILD}}\left(\frac{W_1}{H_{\text{ILD}}} + \frac{4\ln(2)}{\pi}\right) \tag{21a}$$

$$C_{\text{sub(loss)}} = 2\varepsilon_{\text{Sub}}\left(1 + \frac{\sigma_{\text{Sub}}}{j\varepsilon_{\text{Sub}}\omega}\right)C_{\text{upper}}^{\text{air-filled}}. \tag{21b}$$

As shown in Fig. 7(b), the capacitances in the model are composed of C_{pg}, $C_{\text{psi\&gsi}}$, and C_{sub}. The capacitance C_{pg} is calculated by (22)

$$C_{\text{pg}} = 2C_{\text{upper}} + 2C_{\text{side}}. \tag{22}$$

Although the electric fields in section C_x are separated into two current paths, all electric fields in section C_x are the same as those in section A_x. Because the area of a current path in section C_x is reduced to half of that in section A_x and the capacitance is split in two, the R and L of each current path are twice the values of section A_x. Because these two current paths are, however, connected in parallel, section C_x has the same lumped model with section A_x, as shown in Fig. 4. It means that section C_x has the same characteristic impedance as section A_x. We confirmed the similarity in the impedance between sections A_x and C_x through the 3-D EM simulation by CST MWS using the waveguide port.

The unit cell of the interposer PDN is finally modeled by connecting the RLGC-lumped models of all TL sections

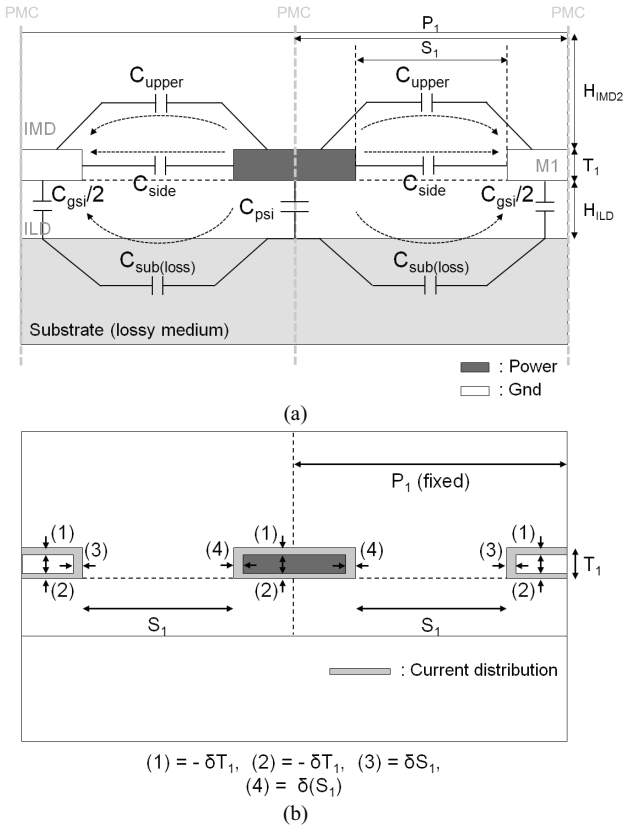

Fig. 7. (a) All capacitances (C_{upper}, C_{side}, C_{psi}, C_{gsi}, and C_{sub}) are shown according to the position of the electric-field generatedin section B_x. (b) Current distribution caused by the field penetration and physical parameter variation according to the current distribution.

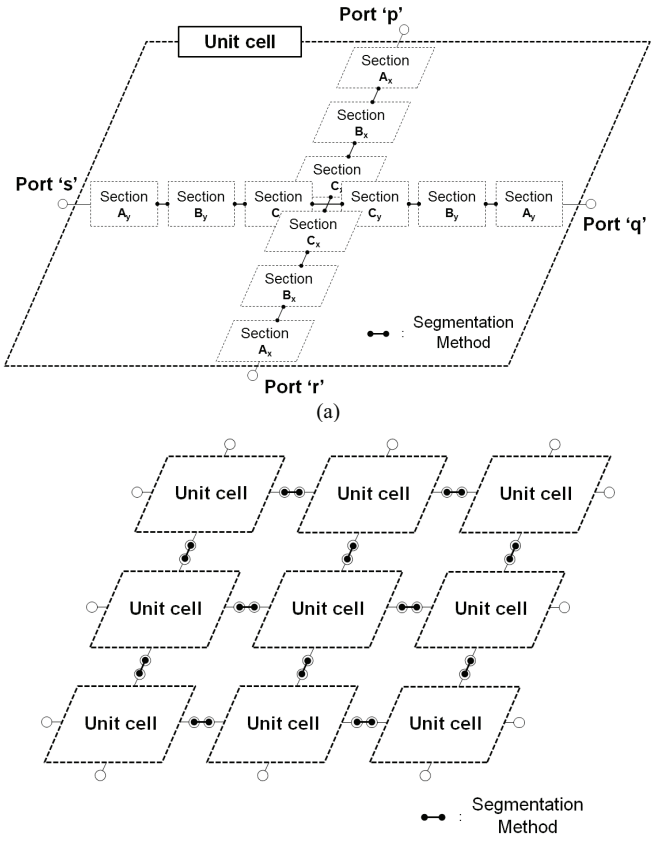

Fig. 8. (a) Unit cell is modeled by connecting the RLGC-lumped models of all TL sections based on a segmentation method. (b) To model the interposer PDN, all ports of a unit cell are connected with the face-to-face ports of the adjacent unit cells with a segmentation method.

based on a segmentation method, as shown in Fig. 8(a). A segmentation method, which is a matrix calculation method [12], is used to incorporate the decomposed structures into a whole structure. Then, by connecting all ports of a unit cell with the face-to-face ports of the adjacent unit cell based on a segmentation method, we can model the whole interposer PDN, as shown in Fig. 8(b).

B. Modeling Method for TSV-Based Stacked Grid-Type PDNs

As shown in Fig. 2, the on-chip and interposer PDNs are hierarchically connected by P/G TSVs and become a TSV-based stacked grid-type PDN. In reality, the impedance estimation of the TSV-based stacked grid-type PDN is more important than that of the interposer PDN itself in 3-D-ICs. The TSV-based stacked grid-type PDN can be modeled based on a segmentation method using grid-type PDN models for the on-chip and interposer PDN and P/G TSV models, as shown in Fig. 9. We previously proposed this modeling method for TSV-based stacked on-chip PDNs in [11]. We apply this modeling method to the modeling of the TSV-based stacked grid-type PDN, including the on-chip and interposer PDN shown in Fig. 1. As shown in Fig. 9, using a segmentation method, the models of the on-chip and interposer PDN are connected with P/G TSV models in a hierarchical order. The upper grid-type PDN representing an on-chip PDN and the lower grid-type PDN representing an interposer PDN can

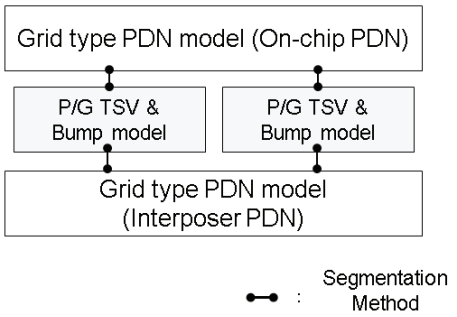

Fig. 9. TSV-based stacked grid-type PDN is modeled by the sequential connections between two grid-type PDN models and the P/G TSV models in a hierarchical order with a segmentation method.

be modeled using the proposed model for interposer PDNs. The structure and the parameters of a P/G TSV pair including bumps and contacts are shown in Fig. 10. Because the physical length of the P/G TSV pair is much shorter than the operating frequency wavelength of several or tens of gigahertz, the lumped approximation is valid, and a single lumped stage is sufficient for the TSV model [19].

Through sequential connections formed in the hierarchical order shown in Fig. 9, a TSV-based stacked grid-type PDN can be modeled. Because we only consider the case in which P/G TSV pairs are further apart from each other than the irrespective heights, we can ignore the coupling between them [20].

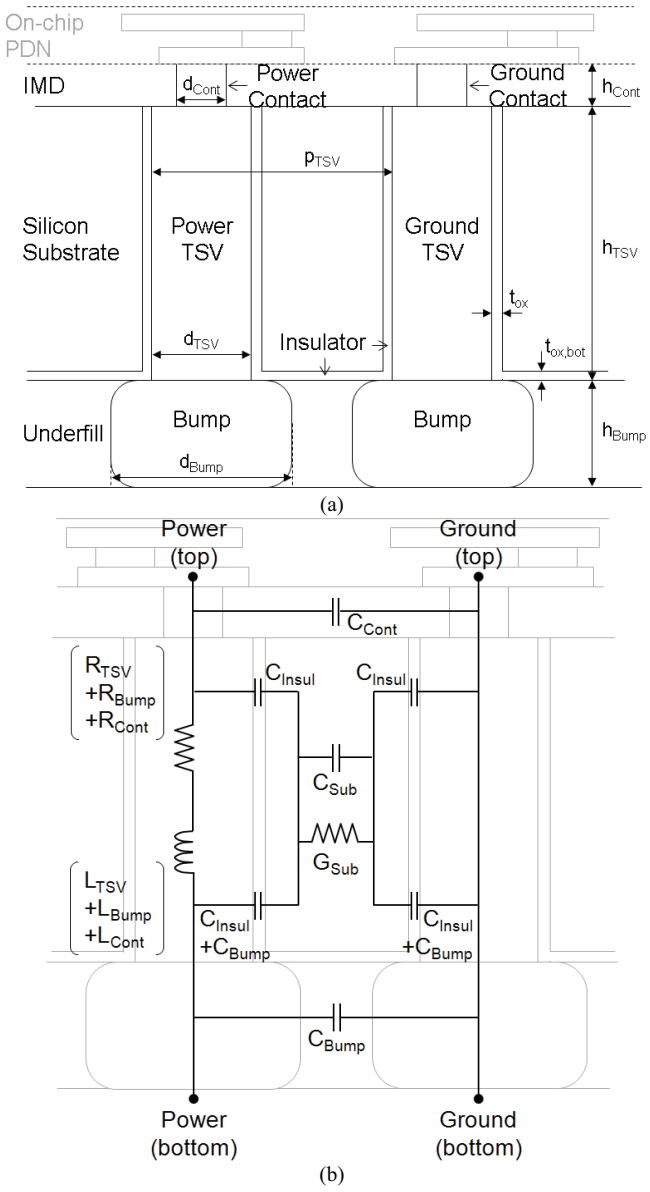

Fig. 10. (a) Structure of a P/G TSV pair including bumps and contacts and their structural parameters. (b) The scalable RLGC-lumped model of a P/G TSV pair.

III. Verification of Models for an Interposer PDN and a TSV-Based Stacked Interposer PDN

To verify the proposed model for the interposer PDN, we compare the PDN impedance curves estimated from the proposed model with those estimated from the EM simulations by CST MWS in the frequency range from 0.1 to 20 GHz. Through these comparisons, the proposed model for the interposer PDN has been validated in the frequency domain. Additionally, we fabricated the TSV-based stacked grid-type PDN composed of two grid-type PDNs, located on the upper level and the lower level shown in Fig. 13, and five P/G TSV pairs. By comparing the PDN impedance curve estimated from the proposed model for the TSV-based stacked grid-type PDN with that obtained from the 3-D simulation and measurement in the frequency range from 0.1

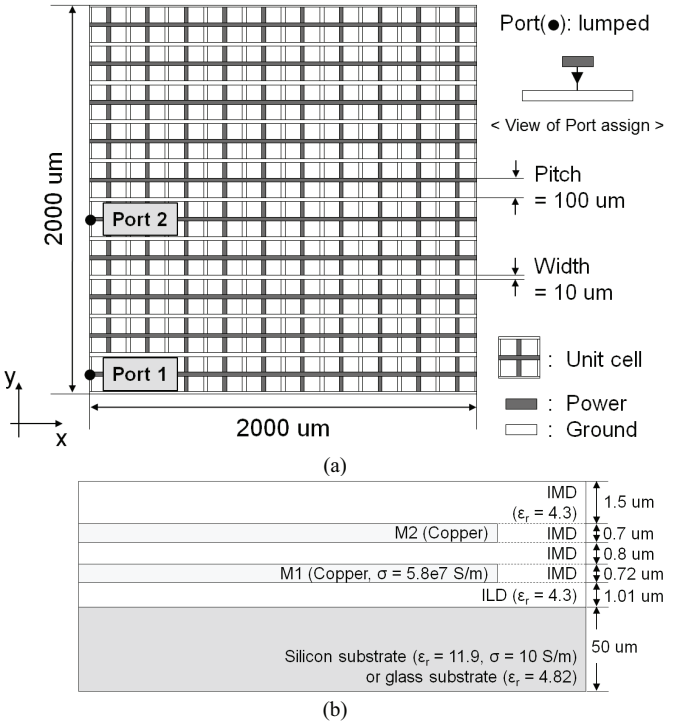

Fig. 11. (a) Top view of the simulated interposer PDN on the silicon substrate with a size of 2 × 2 mm and its assigned port. The metal width and metal pitch between the power and ground lines are 10 and 100 μm, respectively. (b) Stacking information, physical dimensions, and material characteristics of the simulated interposer PDN.

to 20 GHz, the proposed model was verified in the frequency domain.

For verification of the proposed model for the interposer PDN, we simulated the interposer PDNs shown in Fig. 11. The size of the PDN pattern is 2 mm × 2 mm. The metal width and metal pitch between the P/G lines are 10 and 100 μm, respectively. The pattern includes two ports: ports 1 and 2. As shown in Fig. 12(a) and (b), the simulated PDN impedance curves (a self-Z curve and a transfer-Z curve) of the interposer PDNs on the silicon substrate are well matched with those estimated from the proposed model when considering the log–log scale. For the strict comparison between the proposed model and simulation, we plot the percent error (gray circles) between them using (23), as shown in Fig. 12. The percent error between the proposed model and simulation is distributed from 0% to 40%.

$$\text{Error}(\%) = \left| \frac{|\text{PDN}Z_{\text{SIMULATION}}| - |\text{PDN}Z_{\text{PROPOSEDMODEL}}|}{|\text{PDN}Z_{\text{SIMULATION}}|} \right| \times 100 \quad (23)$$

Even though this percent error range is quite large from an engineering-scale perspective, we can closely estimate the impedance level and resonance frequency of the interposer PDN in the frequency range of 0.1–20 GHz when considering the complexity of the interposer PDN and 3-D EM simulation error.

From these observations, we successfully verified the proposed model for the interposer PDN in the frequency range

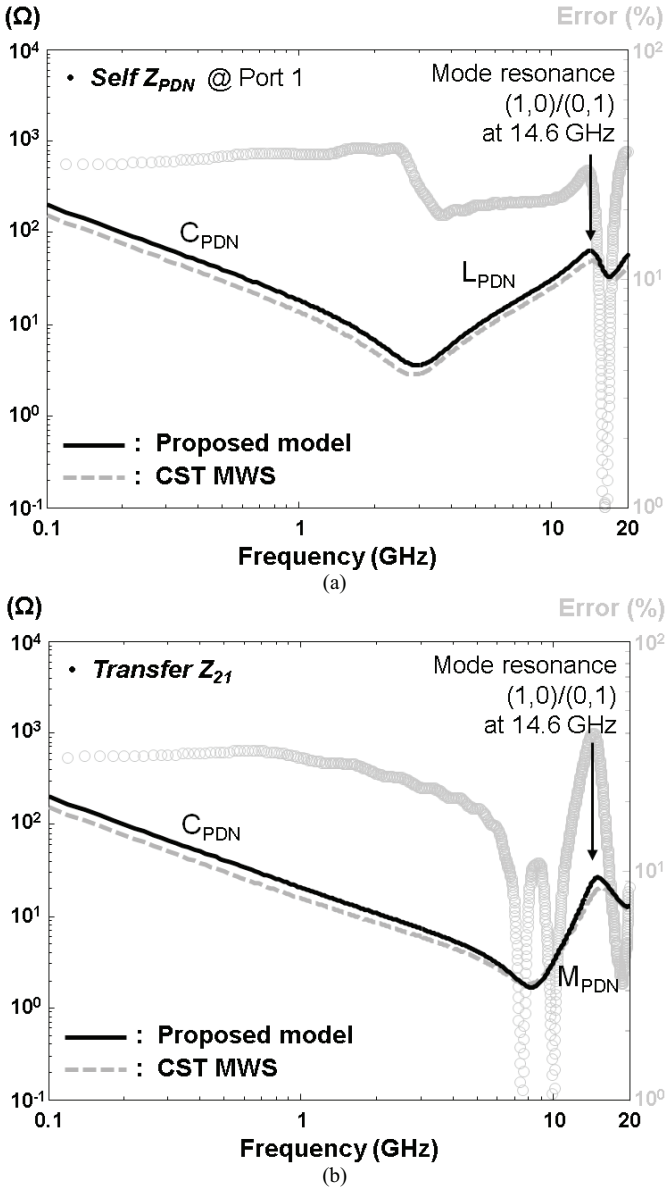

Fig. 12. (a) Self-impedance curve of the interposer PDN on the silicon substrate shown in Fig. 11 obtained from the proposed model and EM simulation by CST MWS. (b) Transfer-impedance curve of the interposer PDN on the silicon substrate shown in Fig. 11 obtained from the proposed model and EM simulation by CST MWS.

of 0.1–20 GHz. The self and mutual inductances (L_{PDN} and M_{PDN}), shown in Fig. 12(a) and (b), respectively, are accurately estimated. Additionally, the mode resonance (1,0)/(0,1) peak generated at 14.6 GHz on the interposer PDNs is successfully estimated using the proposed model. This result confirms the ability of the proposed model to estimate the PDN inductance and mode resonance of the interposer PDNs. We can save time in impedance estimation using the proposed model. The 3-D EM simulator (CST MWS) takes a long time (~25 h) to simulate the interposer PDN (# of the mesh cells: 1 219 212 ea.) shown in Fig. 11 when we use a computer with the following specifications: Intel(R) Core i7-2600 processor @ 3.4 GHz and 16-GB RAM memory. On the contrary, the proposed model for the interposer PDN takes only 17.68 s [unit cell modeling (0.93 s) + grid-type PDN modeling (16.75 s)] to estimate the PDN impedance. Therefore, we conclude that the proposed model is an accurate and efficient method to estimate the impedance of interposer PDNs on the silicon substrate.

For experimental verification of the modeling method in the TSV-based stacked grid-type PDN, we fabricated the double-stacked grid-type PDN shown in Fig. 13. The horizontal size of both upper and lower level grid-type PDNs is 960 μm × 960 μm. They have the same PDN structure. The physical dimensions of the doublestacked gridtype PDN are shown in Table II.

The upper and lower level grid-type PDNs are connected to each other by five pairs of P/G TSVs, as shown in Fig. 13(a). The P/G TSVs play an important role in determining the impedance of the TSV-based stacked grid-type PDN because the total loop inductance of the PDN is critically determined by the number of the P/G TSVs. Therefore, it is important to confirm the TSV connection of the fabricated PDN. To confirm this connection, we took SEM photos, which are shown in Fig. 13(b). To take the SEM photos, we cut the fabricated sample at the dashed lines with the numbers (1), (2), (3), and (4). Thus, we obtained five SEM photos that include all TSVs. From these results, we confirmed the TSV connection and physical dimensions of the fabricated PDN shown in Table II.

Based on physical dimensions and the results of the TSV connection test, we model the fabricated double-stacked grid-type PDN using the proposed interposer PDN models, P/G TSV models [19], and an [Inductance (L) and Capacitance (C)] (LC)-lumped pad model extracted from CST MWS based on the modeling method shown in Fig. 9.

The PDN impedance curves observed at the probing pad are shown in Fig. 14. The solid line represents the PDN impedance that is estimated from the proposed model for the TSV-based stacked grid-type PDN. The dashed line represents the PDN impedance obtained from the measurement. For this measurement, we use a vector network analyzer (Agilent N5230A, bandwidth of instrument: 300 kHz to 26.5 GHz) and a microprobe (FPC-series GS type with a 250-μm pitch from cascade microtech and its calibration kit (106–683 A) for widepitch microprobes). Using these instruments, we measured the impedance of the fabricated PDN in the frequency range of 0.1–20 GHz. The dotted line represents the PDN impedance estimated from the -3-D EM simulation by CST MWS.

As shown in Fig. 14, these three impedance curves are well matched with each other. For the strict comparison between the proposed model and measurement, we plot the percent error (gray circles) between them using (23), as shown in Fig. 14. For the calculation of the percent error, we replace PDN $Z_{SIMULATION}$ in (23) with PDN $Z_{MEASUREMENT}$. The percent error between the proposed model and measurement is distributed from 0% to 60%.

Even though this percent error range is quite large from an engineering-scale perspective, we can closely estimate the impedance level and resonance frequency of the interposer PDN in the frequency range of 0.1–20 GHz when considering

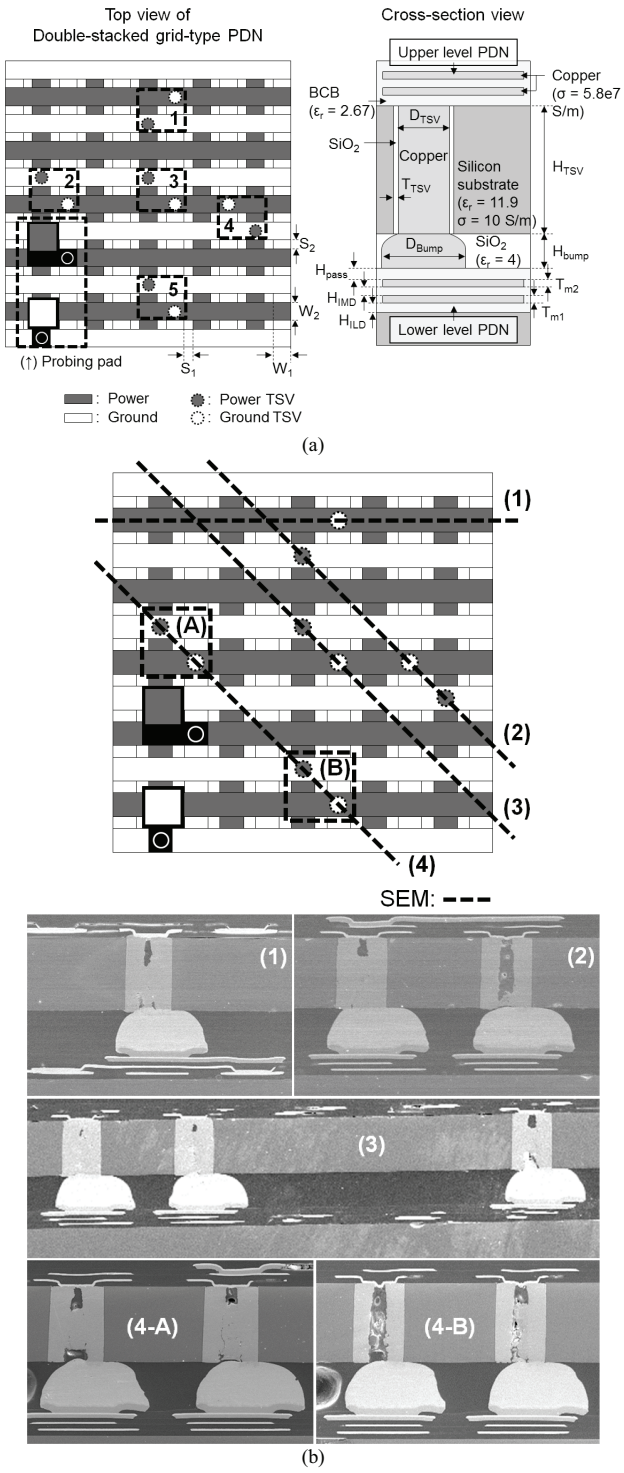

Fig. 13. (a) Top and cross-sectional view of the fabricated double-stacked interposer PDN. The upper-level PDN is connected with the lower-level PDN by five pairs of P/G TSVs. (b) To confirm the TSV connection and physical dimensions of the structure, we took SEM photos. We obtained five SEM photos that include all TSVs. Using the SEM photos, we confirmed that all TSVs are connected with the upper- and lower-level PDNs.

the complexity of the interposer PDN and the dimensional variation in the fabricated PDN.

From this result, we conclude that the modeling method for the TSV-based stacked grid-type PDN is experimentally

TABLE II
PHYSICAL PARAMETERS AND THEIR VALUES IN A FABRICATED DOUBLE-STACKED GRID-TYPE PDN

Parameter	*Description*	*Value*
W_1	Metal width of the M_1 metal	60 μm
W_2	Metal width of the M_2 metal	60 μm
S_1	Space between the power line and ground line on the M1 metal	30 μm
S_2	Space between the power line and ground line on the M2 metal	30 μm
H_{ILD}	Height of the ILD layer	3.88 μm
H_{IMD}	Height of the IMD layer	3.82 μm
H_{pass}	Height of passivation	3.10 μm
T_{m1}	Thickness of the M1 metal	1.94 μm
T_{m2}	Thickness of the M2 metal	1.94 μm
H_{TSV}	Height of the TSV	63 μm
H_{Bump}	Height of the bump	39 μm
D_{TSV}	Diameter of the TSV	40 μm
D_{Bump}	Diameter of the bump	88 μm
T_{SiO2}	Thickness of the SiO_2	0.5 μm

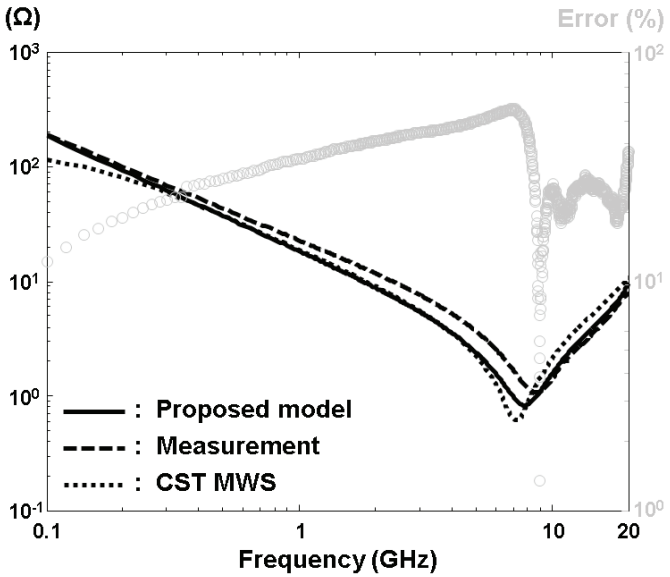

Fig. 14. PDN impedance curves obtained from the proposed model, measurement, and 3-D EM simulation observed at the probing pad shown in Fig. 13.

verified in the frequency range of 0.1–20 GHz. More importantly, we greatly decreased the simulation time. The 3-D EM simulator (CST MWS) takes a long time (25.5 h) to simulate the double-stacked interposer PDN shown in Fig. 13(a) (# of the mesh cells: 259 346 ea.), when we use a computer with an Intel(R) Core i7-2600 CPU and 16 GB of RAM that is operating at 3.4 GHz. In contrast, the proposed model for the stacked grid-type PDN takes only 5.79 s [unit cell modeling (1.73 s) + grid-type PDN and TSV-based grid-type PDN modeling (4.06 s)] to estimate the impedance of the double-stacked grid-type PDN. Therefore, we conclude that the proposed model is an accurate and efficient method to estimate the PDN impedance of TSV-based stacked grid-type PDNs.

IV. Analysis of Impedance Curves of an Interposer PDN and a TSV-Based Stacked Grid-Type PDN

A. Analysis of Impedance Curves of an Interposer PDN With Variation in the PDN Horizontal Size

In this section, we analyze the impedance curves of the interposer PDN and TSV-based stacked grid-type PDN. In the design of the interposer PDN and TSV-based stacked grid-type PDN, the horizontal size of the interposer PDN and the number of P/G TSVs in the TSV-based stacked grid-type PDN are the main design issues. To analyze the PDN impedance curves according to the variations in these design issues, we estimate the PDN impedance curves when changing the horizontal size of the interposer PDN and the number of P/G TSVs in the TSV-based stacked grid-type PDN using the verified models.

First, we estimate the impedance curves of the interposer PDN in the frequency range from 0.1 to 20 GHz with respect to the variation in the horizontal size of the interposer PDN. As shown in Fig. 15(a), there are three types of interposer PDNs with different horizontal sizes. However, they are composed of the same unit cells shown in Fig. 11. PDN (A) is exactly the same as the 2 × 2 mm interposer PDN shown in Fig. 11(a). The horizontal sizes of PDN (B) and PDN (C) are 4 × 4 mm and 6 × 6 mm, respectively. These PDNs have the same port position (0 mm, 0.1 mm) in the x- and y-axes. The reason why we selected this position as the port position is that all mode resonances occur at the boundary of the interposer PDN because the states of the voltage and current of all modes at the boundary are always high and low, respectively.

As shown in Fig. 15(b), the capacitance (C_{PDN}) and inductance (L_{PDN}) of the interposer PDN increase, as the PDN size increases. Because of these increases, the PDN impedance determined by the capacitance is lowered in the low-frequency range, and the impedance determined by the inductance is increased in the midfrequency range. The capacitance (C_{PDN}) increases proportionally to the increase of the PDN size. We can represent this capacitance increase according to the size variation using (24)

$$C_{\mathrm{TARGET}} = \frac{A_{\mathrm{TARGET}}}{A_{\mathrm{REF}}} C_{\mathrm{REF}}. \tag{24}$$

In (24), C_{REF} and C_{TARGET} are the capacitances of the reference and target PDN, respectively, on the condition that these PDNs are composed of the same unit cells. A_{REF} and A_{TARGET} are the horizontal sizes of the reference and target PDN, respectively.

The inductance (L_{PDN}) increases proportionally to the increase in the length of the PDN in both the x- and y-axes when the PDNs are square. We can represent this inductance increase according to the size variation using (25). This equation is experimentally derived by comparing the inductances obtained when the PDN size is varied. The inductances are calculated using the capacitance values of the PDNs and the series resonance frequency [f_A, f_B, and f_C in Fig. 15(b)]

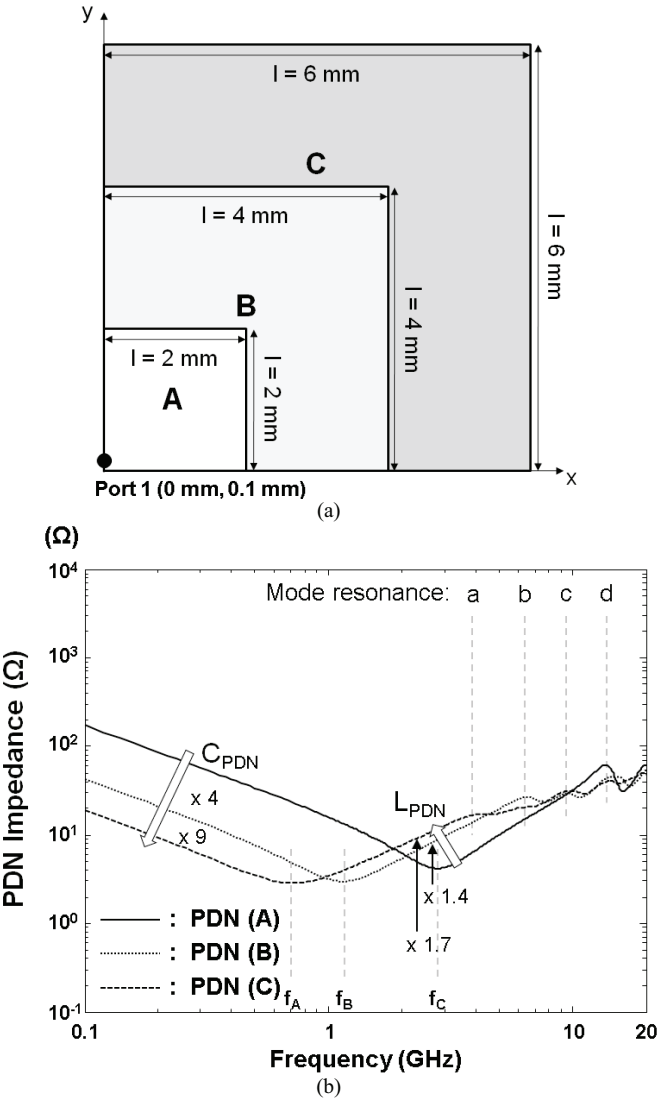

Fig. 15. (a) Size and port assigned to interposer PDNs (A), (B), and (C). (b) PDN impedance curves of PDN (A), PDN (B), and PDN (C). As the size of the interposer PDN increases, the capacitance and inductance of the PDN are increased. Additionally, the mode resonance occurs at the lower frequency with the increase in the PDN size.

using

$$L_{(A,B,C)} = \frac{1}{(2\pi f_{(A,B,C)})^2 C_{(A,B,C)}}$$

$$L_{\mathrm{TARGET}} = \sqrt{\frac{l_{\mathrm{TARGET}}}{l_{\mathrm{REF}}}} L_{\mathrm{REF}}. \tag{25}$$

In (25), L_{REF} and L_{TARGET} are the inductances of the reference and target PDN, respectively, on the condition that these PDNs are composed of the same unit cells. l_{REF} and l_{TARGET} are the lengths of the reference and target PDN, respectively. Based on (24), the capacitances of PDN (C) and PDN (B) are nine and four times more than the capacitance of PDN (A), respectively. The inductances of PDN (C) and PDN (B) are $\sqrt{(6\,\mathrm{mm})/(2\,\mathrm{mm})} = \sqrt{3}$ times and $\sqrt{(4\,\mathrm{mm})/(2\,\mathrm{mm})} = \sqrt{2}$ times more than the inductance of PDN (A), respectively, as determined by (25).

As a distinct feature of the large-sized interposer PDN, the mode resonances of PDN (A), PDN (B), and PDN (C)

TABLE III
MODE NUMBERS OF MODE RESONANCES OF PDN (A), PDN (B) AND PDN (C)

Mode resonance and resonance frequency	*Mode number*
a (at 4.36 GHz)	(1,0)/(0,1) in PDN (C)
b (at 6.58 GHz)	(1,0)/(0,1) in PDN (B) (1,1) in PDN (C)
c (at 9.64 GHz)	(1, 1) in PDN (B) (2,0)/(0,2) in PDN (C)
d (at 14.0 GHz)	(1,0)/(0,1) in PDN (A) (2,0)/(0,2) in PDN (B) (2,1)/(1,2) in PDN (C)

occur at the resonance frequency a (4.36 GHz), b (6.58 GHz), c (9.64 GHz), and d (14.0 GHz) in the high-frequency range. The mode numbers of these mode resonances are shown in Table III. In mode resonances (i, j), the numbers i and j are the mode numbers for the x- and y- axes, respectively. The mode resonance is generated by the standing wave formed on the interposer PDN, when $(N/2)$, $(N = 1, 2, 3 \ldots)$ of the wavelength is equal to the lengths of the PDN in the x- or y-axes. At this time, the number N is the mode number of the mode resonance. The mode resonance (2,1) means that the standing wave with one wavelength is formed on the x-axis and the standing wave with half of the wavelength is formed on the y-axis. Additionally, the mode resonance (1,0)/(0,1) means that the standing wave with half of the wavelength is formed on the x- or y-axis, because the length of the PDN along the x-axis is equal to that along the y-axis in the square-shaped PDN.

As shown in Fig. 15(b), the mode resonance occurs at a lower frequency range and more resonances occur as the PDN size increases. Fortunately, Q-factors at the resonances are reduced because of the increase in the resistive electrical components caused by the increase in the PDN size. These reductions make the parallel resonance peaks flat. However, because the mode resonances of the larger PDN occur at its high inductance, the impedance gap between the larger PDN and the smaller PDN is significant. For example, the impedance level of PDN (C) is 17.09 Ω at resonance frequency a. In contrast, the impedance level of PDN (A) is 7.162 Ω at this frequency. The impedance of PDN (C) is more than two times higher than that of PDN (A). Therefore, the SSN generated on PDN (C) at the frequency is more critical than that on PDN (A) in 3-D ICs.

From the analysis on the change in the PDN impedance according to the variation in the horizontal size of the interposer PDN, we conclude that the larger PDN brings a significant increase in the impedance level in the mid- and high-frequency range because of the increased inductance and mode resonances. Of course, the increase in the PDN size helps to reduce the PDN impedance in the low-frequency range. Nevertheless, because there is a powerful method to increase the capacitance using decoupling capacitors, it is necessary to reduce the PDN size when we design the interposer PDN to ultimately reduce the SSN on the interposer PDN. In spite of the difficulty in designing the size of the interposer PDN, the reason why we use the interposer PDN is that the grid-type interposer PDN can critically reduce inductances on power-supply paths compared with P/G TLs. Therefore, the optimum size of the interposer PDN is the minimum size that can supply power to all other PDNs stacked on the interposer PDN serving as the grid-type PDN.

B. Analysis of Impedance Curves of a TSV-Based Stacked Grid-Type PDN With Variation in the Number of P/G TSVs

As shown in Fig. 1, the on-chip PDN is stacked on the interposer PDN, and they become a TSV-based stacked grid-type PDN. In this case, an on-chip PDN is vertically connected with the interposer PDN by P/G TSVs. In the design of the TSV-based stacked grid-type PDN, the main design issue is to determine the number of P/G TSVs used for the connection between the upper-level and the lower-level grid-type PDNs. As the second analysis item, we estimate and analyze the change in the impedance of TSV-based stacked grid-type PDNs with respect to the variation in the number of P/G TSV pairs in TSV-based stacked grid-type PDNs in the frequency range from 0.1 to 20 GHz.

In the TSV-based stacked grid-type PDNs shown in Fig. 16(a), the upper-level grid-type PDN, which is the same as the PDN (A) in Fig. 15(a), is connected to the lower-level grid-type PDN, which is the same as the upper-level PDN through the different number of P/G TSV pairs. The solid line represents the impedance curve of the double-stacked grid-type PDN including a P/G TSV pair. The dotted line represents the impedance curve of the PDN including the P/G TSV pairs (3 ea.). The dashed line represents the impedance curve of the PDN including the P/G TSV pairs (9 ea.), and the dash-dot line represents the impedance curve of the PDN including the P/G TSV pairs (15 ea.).

Because of the TSV connection, the capacitance of the double-stacked grid-type PDN is twice that of a grid- type PDN itself, as shown in Fig. 16(b). The increase in the capacitance results in an impedance reduction in the low-frequency range. The biggest change in the PDN impedance is the reduction of the PDN loop inductance ($L_{\mathrm{PDN\,loop}}$) as the number of P/G TSV pairs increases. In the double-stacked grid-type PDNs, the PDN loops are formed through not only the grid-type PDNs but also the P/G TSV pairs.

To analyze the change in the loop inductance, we look at the change in the PDN loop according to the variation in the number of P/G TSV pairs. The sizes of the PDN loops generated through the P/G TSV pairs are bigger than the loop size of a grid-type PDN itself. Therefore, the loop inductance ($L_{\mathrm{PDN\,loop}}$) of the double-stacked grid-type PDN is higher than the inductance of a grid-type PDN. Because the PDN loops through the P/G TSV pairs are connected in parallel, the loop inductance is reduced with the increase in the number of P/G TSV pairs. The reduction in the loop inductance, however, cannot be continued below the inductance of the interposer PDN. Because of the limit on the reduction of the loop inductance, the number of P/G TSV pairs, which is larger

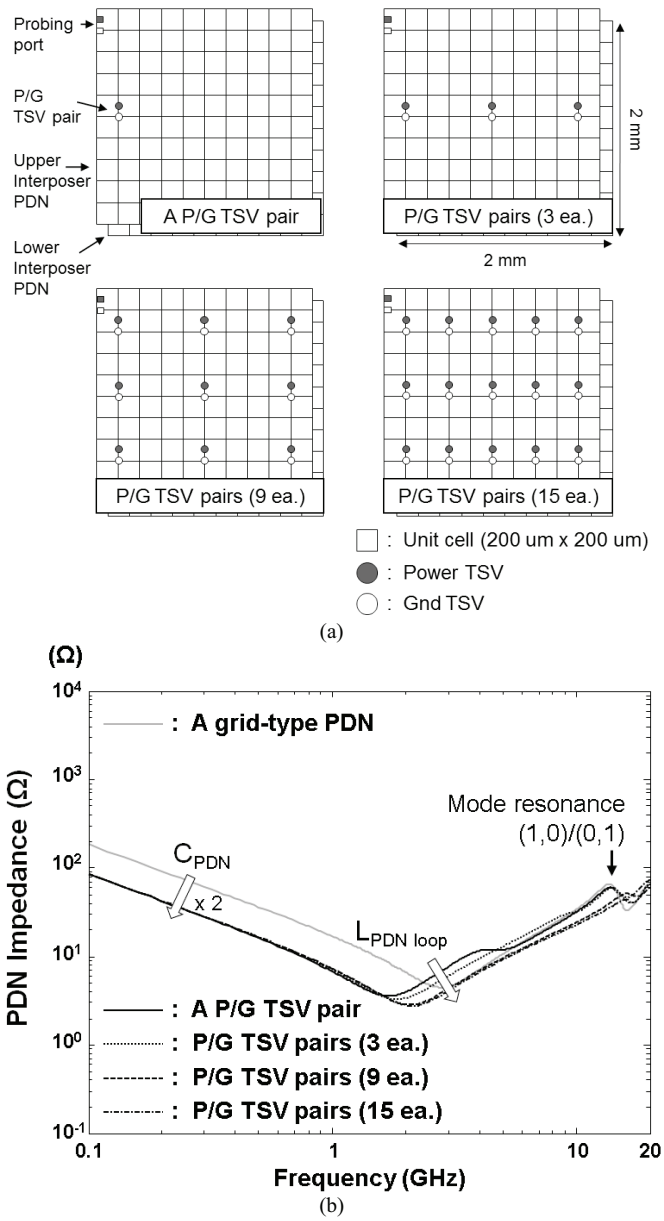

Fig. 16. (a) Four cases of double-stacked interposer PDNs. In these cases, we vary the number of P/G TSV pairs. (b) PDN impedance curves according to the variation in the number of P/G TSV pairs. When the number of P/G TSV pairs increases, the PDN loop inductance (LPDN loop) is reduced. However, the reduction is limited.

than necessary, cannot help reduce the loop inductance. As shown in Fig. 16(b), the loop inductance is rapidly reduced, as the number of P/G TSV pairs increases. In the graph of Fig. 16(b), we observed that only nine P/G TSV pairs are sufficient to reduce the loop inductance in a 2 mm × 2 mm double-stacked grid-type PDN. Therefore, we conclude that the number of P/G TSV pairs can be determined as the number required to prevent EM on TSVs. Fortunately, as the number of P/G TSV pairs increases, Q-factor at the mode resonance (1,0)/(0,1) decreases. This decrease makes the mode resonance peak flat. Therefore, the mode resonance cannot be a problem in the well-designed TSV-based stacked grid-type PDNs that include enough P/G TSVs.

V. Conclusion

In this paper, we proposed models for large-sized interposer and TSV-based stacked grid-type PDNs. Because the interposer plays a significant role in the power distribution in 3-D-ICs, accurate and efficient modeling of interposer PDNs is needed. Therefore, we proposed models for the interposer PDN and TSV-based stacked grid-type PDN. The models are distributed scalable RLGC-lumped models for wide bandwidth and impedance estimation according to variations in the observing position. Additionally, the models can accommodate changes in the physical and material properties of the PDN, allowing us to obtain the physical insights from the structural changes in the PDNs.

The modeling method that we proposed is based on a structural decomposition into TL sections. The accurate modeling of each TL section is very important because errors in a TL section model result in substantial errors in the whole PDN model. Therefore, we used a conformal mapping method to accurately model the capacitance. Additionally, with an increase in the target frequency, a wide bandwidth in the model is necessary. For an accurate modeling at high frequencies, we have to model the frequency-dependent internal impedance of the conductor. To do so, we use a PEM to estimate the internal impedance variation caused by the shallow penetration of the EM fields as the frequency increases. After modeling the decomposed sections, we connect all the TL sections that form the PDNs based on a segmentation method. The matrix-based calculation using a segmentation method accelerates the calculation speed for the PDN impedance estimation. By comparing the PDN impedance curves and simulation time obtained from the proposed models, simulations, and measurements, we successfully verified the accuracy and efficiency of the proposed models for the interposer and TSV-based stacked grid-type PDNs. Through these verifications, we conclude that the proposed models for the interposer PDN and TSV-based stacked grid-type PDN can be powerful and target-flexible models.

Using these verified models, we estimated and analyzed the PDN impedance curves with respect to the variations in the horizontal size of the interposer PDN and the number of P/G TSVs in the double-stacked grid-type PDN, which are the main design issues. From these analyses, we suggested a design guide for the interposer PDN and TSV-based stacked grid-type PDN as required in the predesign steps.

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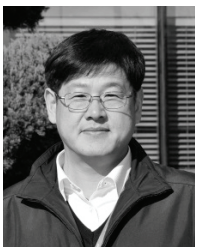

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