Stack Diffusion Process for Cost- and Energy-Efficient Boron Emitter Formation

Marius Meßmer, Sattar Bashardoust, Udo Belledin, Bishal Kafle, Baljeet Singh Goraya, Sven Seren, Heiko Zunft, Sebastian Mack, and Andreas Wolf

***Abstract*—The boron emitter formation for tunnel oxide passivated contact (TOPCon) solar cells faces higher costs compared to the $POCl_3$ diffusion for passivated emitter and rear (PERC) solar cells due to the requirement for higher temperatures and longer process times. This work presents an alternative energy-efficient and low cost of ownership boron diffusion approach for TOPCon solar cells, enabling a highly increased throughput compared to the typically used gas phase diffusion. We use an atmospheric pressure chemical vapor deposition borosilicate glass layer as the boron dopant source and combine it with a subsequent thermal anneal in a quartz tube furnace for dopant drive-in. Here, we either use a conventional single-slot quartz boat configuration, or, for highly increased throughput, a vertical wafer stack configuration with the wafer surfaces in direct contact with each other. We show that this approach yields an emitter doping profile comparable to the state-of-the-art gas phase diffusion with sufficient uniformity across the wafer area. We further investigate the emitter dark saturation current densities j_{0e} as well as the energy conversion efficiency of TOPCon solar cells fabricated for each configuration and compare the results to those of a BBr_3 reference process. These solar cells achieve energy conversion efficiencies exceeding 23% for the stack diffusion approach. Additionally, we demonstrate a potential reduction in both the cost of ownership and the specific electricity consumption of the presented approach.**

***Index Terms*—Atmospheric pressure chemical vapor deposition (APCVD), borosilicate glass (BSG), BBr_3, boron diffusion, high throughput, stack diffusion, tunnel oxide passivated contact (TOPCon).**

I. Introduction

PASSIVATED contacts on n-type monocrystalline silicon wafers are widely seen as the forthcoming cell technology. Within this decade, this technology is expected to gain a considerably high market share of cell technology [1]. While the passivated emitter and rear (PERC) solar cell [2], [3] on p-type monocrystalline silicon is still the working horse in the photovoltaic (PV) industry, the PV industry is currently looking for a cost-effective way to transfer the tunnel oxide passivated contact (TOPCon) [4] solar cells into mass production. On the laboratory scale, already high energy conversion efficiencies are reported [5], [6] and also in industrial manufacturing, promising results are published [7], [8], [9]. Nevertheless, the TOPCon process still faces high costs, as apart from a significantly higher metallization cost [10], boron diffusion requires much higher temperatures and longer process times compared to the $POCl_3$-diffusion for PERC solar cells [10]. Recently, we presented a high throughput boron emitter formation process [11] by means of a predeposited doping source and thermal diffusion using stacked wafers. This work investigates this approach in more detail and presents a cost of ownership (COO) analysis, details on the development of the stack diffusion process, as well as independently confirmed solar cell results.

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Marius Meßmer, Sattar Bashardoust, Udo Belledin, Bishal Kafle, Baljeet Singh Goraya, Sebastian Mack, and Andreas Wolf are with the Fraunhofer Institute for Solar Energy Systems, 79110 Freiburg, Germany (e-mail: marius.messmer@ise.fraunhofer.de; sattar.bashardoust@ise.fraunhofer.de; udo.belledin@ise.fraunhofer.de; bishal.kafle@ise.fraunhofer.de; baljeet.singh.goraya@ise.fraunhofer.de; sebastian.mack@ise.fraunhofer.de; andreas.wolf@ise.fraunhofer.de).

Sven Seren and Heiko Zunft are with the Gebr. SCHMID GmbH, 72250 Freudenstadt, Germany (e-mail: seren.sv@schmid-group.com; zunft.he@schmid-group.com).

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II. Approach and Cost Calculation

The state-of-the-art emitter formation technique for TOPCon (on n-type substrate) or other n-type solar cells is the tube furnace gas phase diffusion using e.g., boron tribromide BBr_3 as liquid dopant source [1]. This process includes a formation of the borosilicate glass (BSG) layer and a subsequent drive-in phase at elevated temperatures. Typical load for this process is up to 1600 wafers (up to M10 size) per process/per tube. Due to the higher temperature and longer process time, the boron diffusion process induces significantly higher processing cost compared to a $POCl_3$-diffusion. The recently presented high throughput approach [11] allows for a cost-effective and energy-efficient boron emitter formation. This approach features a predeposition of the BSG layer and an undoped capping layer of silicon oxide SiO_x by atmospheric pressure chemical vapor deposition (APCVD). Alternative BSG deposition methods, such as a tube furnace process using BBr_3 are also possible. The following thermal process required for the in-diffusion of boron dopants into the silicon is performed in a stacked configuration to increase throughput. In this stacked configuration, a theoretical limit (volume limit for a typical tube furnace) of 10 000 wafers per process/tube enables an increase of the throughput by a factor of 6.25 for M10 sized wafers. For the following COO calculation, a conservative throughput of 6000 wafer per process/tube (factor

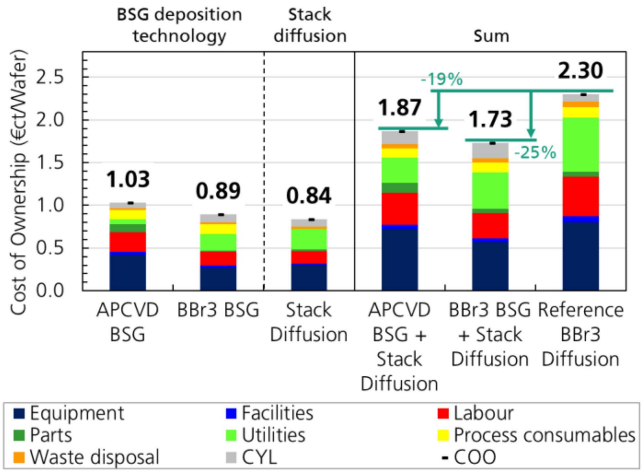

Fig. 1. COO calculation for the high throughput approach of BSG deposition (first and second bar) in combination with a stack diffusion process (third bar) for M10 sized wafers. The sum of the total process is shown in the fourth and fifth bar and compared to the state-of-the-art BBr_3 diffusion process in the sixth bar. The colors represent different cost types; see legend, including the cost of yield loss.

TABLE I
ESTIMATED SPECIFIC POWER CONSUMPTION FOR THE BORON EMITTER FORMATION

	BBr_3 reference	Stack diffusion	APCVD BSG	BBr_3 BSG
Specific power consumption (Wh/wafer)	31	11.9	1.9	9.5

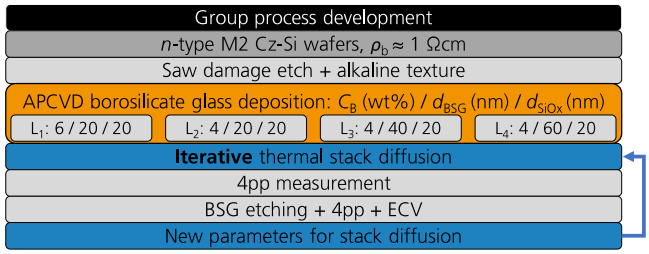

Fig. 2. Process scheme for the iterative thermal stack diffusion process development using different APCVD stack layers containing BSG with different thicknesses and boron concentration, each capped with a 20 nm thick SiO_x layer.

3.75) is assumed due to a possible mechanical limitation by the weight of the wafers.

We calculated the specific COO (cost per wafer) for our state-of-the-art process route for TOPCon solar cells with BBr_3 diffusion, as well as for the high throughput approach using APCVD layers and thermal stack diffusion proposed in this article. The calculations were conducted with the "SCost" COO model [12], which is aligned to the SEMI standards E35 [13] and E10 [14]. The model input data is based on industrial equipment and process parameters assuming M10 sized wafers. The results are depicted in cost split charts in Fig. 1. For the BSG predeposition we analyzed two alternative processes. As a first approach, the BSG/SiO_x stack is deposited by APCVD, resulting in a COO of 1.03 €ct/Wafer. As an alternative method, we calculated a BSG deposition in a typical tube furnace process using BBr_3 with a load of 1600 wafers per tube/process. The COO for this approach is 0.89 €ct/Wafer, close to the cost estimated for the APCVD approach. For both the presented deposition methods, the cost model applies the stack diffusion process for the subsequent drive-in step. Here, we assume a load of 6000 wafers per tube and 10 tubes per machine. For this amount of wafers and their higher load, an adapted automation as well as increased mechanical strength of paddles is taken into account by increasing the investment cost for the equipment (furnace + automation) by 30%. Furthermore, the increased heat capacity due to the additional wafers is considered by increasing the power consumption of the machine by 23%. This results in a COO of 0.84 €ct/Wafer for the thermal process alone. The COO sum for the emitter formation with APCVD or BBr_3 BSG deposition followed by the stack diffusion process is 1.87 €ct/Wafer or 1.73 €ct/Wafer, respectively. Comparing this result with the state-of-the-art BBr_3 diffusion (2.30 €ct/Wafer) shows a significant COO reduction of 19% or 25%, respectively.

Besides the COO, we calculate the specific power consumption (Wh/wafer) of the different approaches, see Table I. The heating of the M10 wafer itself to the peak temperature only requires 3.3 Wh/wafer, calculated from the temperature-dependent heat capacity of silicon. However, the BBr_3 diffusion exhibits a power consumption of 31 Wh/wafer, several times higher than the energy required for heating up the wafers. Comparing the stack diffusion process to the BBr_3 diffusion shows a reduction of the specific power consumption from 31 to 11.9 Wh/wafer and thus a 61% reduction in energy consumption. However, a fair comparison needs to include the power consumption required for the dopant source deposition. The BBr_3 BSG deposition in a tube furnace (1600 wafer per tube/process) requires an additional 9.5 Wh/wafer. Thus, a total specific power consumption reduction of 31% is achieved for the combination of BBr_3 BSG deposition and stack diffusion. The APCVD BSG deposition only requires 1.9 Wh/wafer, enabling a total specific power consumption reduction of 55% compared to state-of-the-art emitter formation. This shows that our approach with predeposited dopant source in combination with a stack diffusion process is an energy- and cost-efficient alternative route for boron emitter formation.

III. EXPERIMENTAL

A. Diffusion Process Development

The scheme for the development of the boron emitter formation with the earlier described approach using predeposited APCVD layers and a subsequent thermal diffusion process is shown in Fig. 2. We use *n*-type phosphorus-doped Czochralski-grown silicon (Cz-Si:P) wafers with an M2 format and a base resistivity of $\rho_b \approx 1\ \Omega$cm as the starting material. After saw damage etching (SDE) and alkaline texturing of the wafers, the dopant source is deposited by APCVD. Here, we deposit four different stack layer systems on one side of the wafer. For the stack layer system L_1, we deposited a BSG layer with a thickness of $d_{BSG} = 20$ nm capped by an undoped silicon oxide SiO_x layer

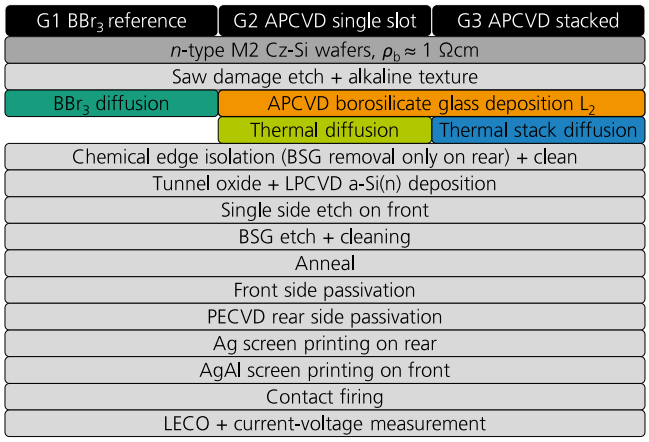

Fig. 3. Process scheme for the fabrication of TOPCon solar cells: Group 1 represents the reference process with boron diffusion from boron tribromide BBr_3. Groups 2 and 3 uses APCVD BSG layers as a dopant source with the in-diffusion process in single slot or stack configuration, respectively. More details on the cell process are given in Ref. [11].

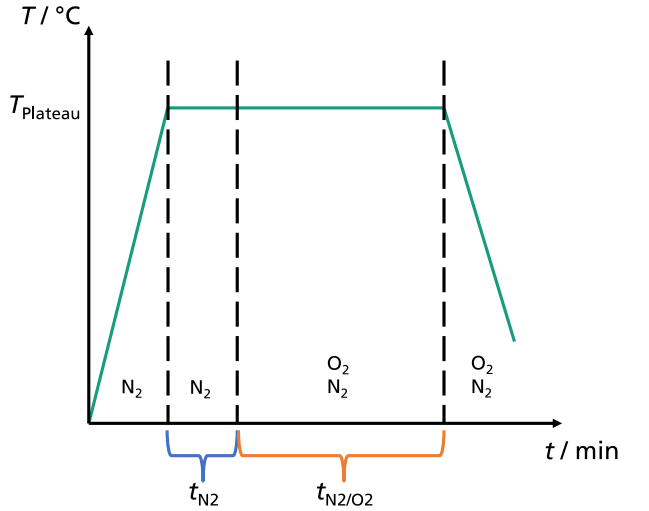

Fig. 4. Schematic illustration of the temperature-time profile of the stack diffusion process with the respective gases of the process atmosphere.

with a thickness of $d_{\mathrm{SiOx}} = 20$ nm. For the BSG deposition we use a ratio

$$R_{\mathrm{B2H6}} = \phi_{\mathrm{B2H6}} / \phi_{\mathrm{SiH4}} \tag{1}$$

for the gas flow of diborane B_2H_6 and silane SiH_4, ϕ_{B2H6} and ϕ_{SiH4}, respectively, of $R_{\mathrm{B2H6}} = 0.215$. This results in an expected boron concentration C_{B} within the BSG layer of $C_{\mathrm{B}} \approx 6$ wt% from comparison to literature data [15]. For L_2 - L_4, we use a ratio of $R_{\mathrm{B2H6}} = 0.136$ for the BSG layer, resulting in an expected concentration of $C_{\mathrm{B}} \approx 4$ wt% implementing different thicknesses of $d_{\mathrm{BSG}} = \{20, 40, 60\ \mathrm{nm}\}$, each capped with a layer of $d_{\mathrm{SiOx}} = 20$ nm. Then, an iterative process development is performed, containing thermal stack diffusion, four-point probe (4pp) measurement to determine the emitter sheet resistance R_{sh}. For selected samples the BSG/SiO_x layers are removed wet-chemically prior to 4pp and electrochemical capacitance-voltage (ECV) measurement [16] to determine the active charge carrier concentration as a function of the depth. With this result, new parameters for the stack diffusion process are selected.

B. Solar Cell Fabrication

The fabrication process for TOPCon solar cells is depicted in Fig. 3, as presented in Ref. [11]. For all groups, n-type phosphorus-doped Czochralski-grown silicon (Cz-Si:P) wafers with M2 format and a base resistivity of $\rho_{\mathrm{b}} \approx 1\ \Omega$cm serve as starting material. Group 1 represents the reference group with boron tribromide BBr_3 as liquid dopant precursor. Groups 2 and 3 receive an APCVD process on one side of the wafer with layer L_2 with a BSG layer of $d_{\mathrm{BSG}} = 20$ nm ($C_{\mathrm{B}} = 4$ wt%) capped by a SiO_x layer with $d_{\mathrm{SiO2}} = 20$ nm. For group 2, the wafers are placed in dedicated slot each in a conventional quartz boat (single slot configuration, 2.38 mm distance), whereas for group 3, the wafers are stacked vertically in small groups of four wafers in one slot of the quartz boat. Ref. [11] presents more details on the solar cell process.

Besides the solar cells, we fabricate test samples for the characterization of the emitter sheet resistance R_{sh} by 4pp mappings and the dark saturation current density $j_{0\mathrm{e}}$ by quasi steady-state photoconductance decay (QSSPC) measurements using the procedure from [17].

IV. Results and Discussion

A. Diffusion Process Development

The development of a stack diffusion process for predeposited APCVD layers, as described in Section III-A, starts with a diffusion process as schematically shown in Fig. 4. After loading the wafers in a special quartz boat for wafer stacks [18], the temperature in the process tube is ramped up in a nitrogen (N_2) atmosphere to the plateau temperature T_{Plateau}. On the plateau, a first phase of N_2 for a time t_{N2} takes place before the atmosphere is switched to a mixture of N_2 and oxygen (O_2) for a time $t_{\mathrm{N2/O2}}$. In this second phase, a SiO_2 diffusion barrier grows at the BSG/Si interface and oxidizes a possible boron-rich-layer [19], [20], [21], [22]. This N_2/O_2 mixture is kept as the process atmosphere until the wafers are unloaded from the tube furnace.

The aim of this development is a boron emitter comparable to the emitter processed with the state-of-the-art BBr_3 diffusion process. This means an emitter sheet resistance of $R_{\mathrm{sh}} \approx 120\ \Omega$/sq, a depth of $x \approx 1.1\ \mu$m, and a peak concentration of $N_{\mathrm{max}} \approx 1{\cdot}10^{19}\ \mathrm{cm}^{-3}$. A first stack diffusion process results in $73 < R_{\mathrm{sh}} < 82\ \Omega$/sq for different APCVD layers, see Fig. 5. For the layers L_2 – L_4 with $C_{\mathrm{B}} = 4$ wt% boron, the R_{sh} decreases with increasing thickness of the BSG layer d_{BSG}, as expected since a higher amount of boron is available. Furthermore, N_{max} and x also increases with increasing d_{BSG} due to the higher total boron dose as apparent in the charge carrier concentration profiles in Fig. 5. L_1 with $C_{\mathrm{B}} = 6$ wt% boron and $d_{\mathrm{BSG}} = 20$ nm shows comparable charge carrier concentration profile and R_{sh} as layer L_3 with the lower boron concentration of $C_{\mathrm{B}} = 4$ wt% but higher layer thickness of $d_{\mathrm{BSG}} = 40$ nm. This shows that for our high throughput approach, APCVD BSG layers of only

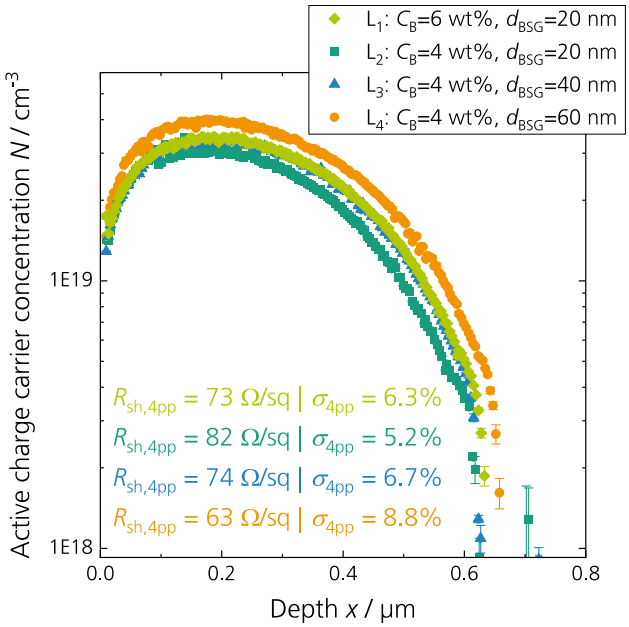

Fig. 5. Active charge carrier concentration profile as a function of the depth measured by ECV on textured surface for the process development version V1 for all four investigated APCVD layer systems. Also given are the sheet resistances near the ECV measurement spot $R_{\mathrm{sh,4pp}}$ in the wafer center and the standard deviation $\sigma_{4\mathrm{pp}}$ of the whole wafer sheet resistance (same order as in the legend). The profiles are scaled to match the locally measured sheet resistance.

$d_{\mathrm{BSG}} = 20$ nm thickness and a low boron concentration of $C_{\mathrm{B}} = 4$ wt% are sufficient to diffuse an adequate amount of boron into the wafer. This is advantageous in terms of throughput and process consumable usage.

In further development steps, the APCVD boron emitter formation is further optimized by adapting T_{Plateau}, t_{N2} and $t_{\mathrm{N2/O2}}$ of the stack diffusion process to mimic the profile and sheet resistance of the reference BBr_3 process. In Fig. 6(a), a 4pp map as a first result close to the desired R_{sh} is shown. We reach $R_{\mathrm{sh}} = 105.4$ Ω/sq with a high standard deviation of $\sigma = 11.4$ Ω/sq. Apparently, the process yields a nonuniform, radial R_{sh} distribution over the wafer surface, showing a higher doping in the wafer middle, decreasing toward the wafer edges. The development of the stack diffusion process showed that the influence of the time and temperature when oxygen (O_2) is introduced into the process is of high importance for the uniformity of the doping. It is known from the literature, that stacked wafers heat up more nonuniformly compared to free-standing wafers [23]. This temperature nonuniformity might influence the local growth of the SiO_2 interface layer acting as a diffusion barrier, which in turn influences the homogeneity of the doping over the wafer surface.

Taking this into account, we adjusted the parameters for introducing oxygen to the process and were able to reduce the relative standard deviation to $\sigma = 3.5\%$ [see Fig. 6(b)], which is similar to the uniformity of the BBr_3 reference process. Fig. 7 shows the charge carrier concentration profiles from the APCVD BSG stack diffusion and a reference BBr_3-diffusion. We reach a similar maximum peak concentration of $N_{\mathrm{max}} \approx 1{\cdot}10^{19}$ cm^{-3} and a slightly deeper doping profile, resulting in a slightly lower sheet resistance compared to the state-of-the-art emitter by BBr_3-diffusion.

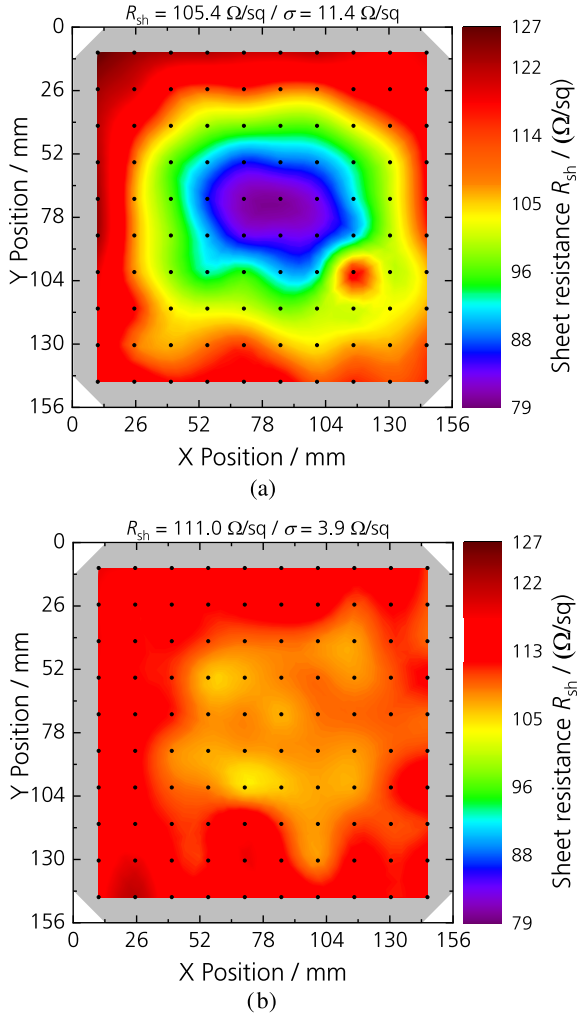

Fig. 6. Sheet resistance distribution over the entire wafer surface measured by 4pp in a 10 × 10 mapping on M2 sized wafers. (a) First development result close to the desired R_{sh} with nonuniform doping over the surface. (b) Further developed R_{sh} results with uniform doping.

B. Solar Cell Fabrication

In this section, we introduce the APCVD technology into the TOPCon solar cell manufacturing sequence, as shown in Fig. 3. For the single slot as well as the vertically stacked wafers, the same thermal diffusion process is performed. The APCVD layers in this cell batch are from a different run than the layers for the process development in Section A and exhibit slightly changed boron content. Fig. 8 shows the emitter dark saturation current density $j_{0\mathrm{e}}$ as a function of the emitter sheet resistance R_{sh} for the reference BBr_3 diffusion process as well as for both configurations of the thermal diffusion process with APCVD BSG layers. The sheet resistance is measured by 4pp in a 10 × 10 pattern over the wafer surface. The dark saturation current density $j_{0\mathrm{e}}$ is extracted from QSSPC data with five measurements per wafer. The reference BBr_3 process yields an emitter dark saturation current density $j_{0\mathrm{e}} = (26 \pm 3)$ fA/cm^2 at an emitter

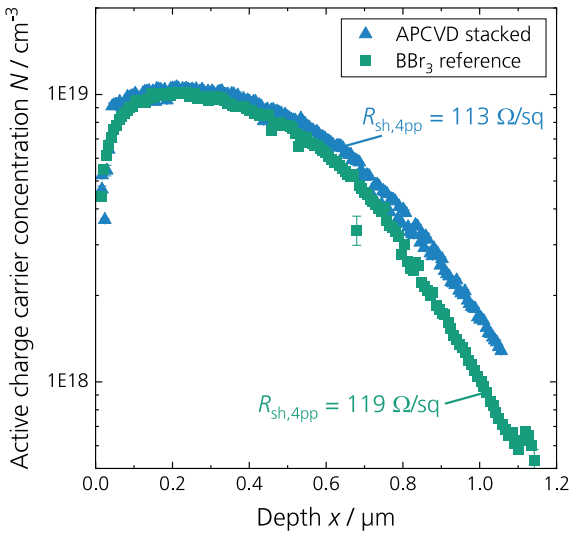

Fig. 7. Active charge carrier concentration profile as a function of the depth measured by ECV on textured surface for the APCVD stack diffusion process development with the APCVD layer L_2 with $C_B = 4\%$ boron and a thickness of $d_{BSG} = 20$ nm compared to the BBr_3 reference process. Both measurements are performed in the wafer center; the profiles are scaled to match the locally measured sheet resistance.

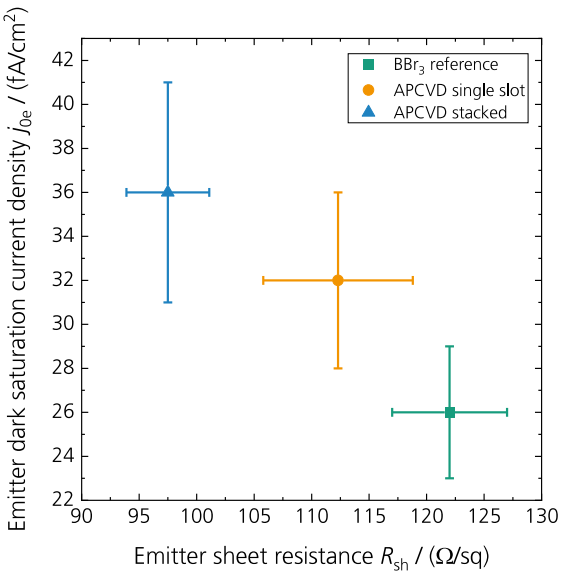

Fig. 8. Average value and standard deviation of the emitter dark saturation current density j_{0e} measured by QSSPC on five positions per wafer as a function of the emitter sheet resistances R_{sh} after the diffusion process measured by 4pp in a 10 × 10 pattern on one wafer per group.

sheet resistance $R_{sh} = (122.0 \pm 5.0)$ Ω/sq. For the APCVD single slot configuration the thermal diffusion processes yields a slightly increased j_{0e} with $j_{0e} = (32 \pm 4)$ fA/cm^2 at a slightly decreased R_{sh} of $R_{sh} = (112.3 \pm 6.5)$ Ω/sq, while stacking shows a stronger in-diffusion of the dopants with $R_{sh} = (97.5 \pm 3.6)$ Ω/sq resulting a further increased $j_{0e} = (36 \pm 5)$ fA/cm^2. This increase of j_{0e} is only partly related to the higher doping level and thus, increased Auger recombination. The reason for the increased j_{0e} for the stacked configuration compared to single slot is not jet clear and needs to be further investigated.

The difference in R_{sh} between single slot configuration and stacked samples is explained by the earlier mentioned influence of the introduction of O_2 in Section IV-A. Our hypothesis states that for stacked samples, the oxygen gas needs more time to reach the wafer surfaces which are in direct contact to each other due to stacking. Therefore, the growth of the silicon dioxide SiO_2 diffusion barrier is suppressed and thus, the in-diffusion of boron into the wafer is prolonged compared to free standing samples. This result in a stronger doping and decreased R_{sh} for the stacked wafers compared to free standing wafers in single slot configuration where O_2 can reach the wafer surface directly.

The implementation of boron diffusion from APCVD BSG layers into solar cell processing in combination with single slot and stacked configuration yields the solar cell current voltage (*IV*) parameters shown in Fig. 9 as box plots measured by an industrial cell tester (grid touch unit for the 0BB front side metallization and a nonreflective rear side chuck) after laser enhanced contact optimization (LECO) [24], [25]. The reference sequence using BBr_3 diffusion yields a median energy conversion efficiency of $\eta = (22.6 \pm 0.2)\%$ with a peak energy conversion efficiency of $\eta = 22.9\%$. Here, open-circuit voltages $V_{oc} = (695 \pm 2)$ mV are reached in median, peaking in $V_{oc} = 698$ mV. Performing the boron diffusion with a APCVD BSG source in a subsequent thermal diffusion process in single slot configuration yields a median energy conversion efficiency of $\eta = (22.5 \pm 0.1)\%$, which is slightly lower than the reference processing. This mainly results from a slightly reduced V_{oc} of $V_{oc} = (693 \pm 2)$ mV, compared to the reference. Here, also high peak energy conversion efficiency of $\eta = 22.7\%$ are reached.

Using stacked wafers with APCVD BSG layers results in a median energy conversion efficiency of $\eta = (21.9 \pm 0.3)\%$ with decreased *FF* and a 10 mV lower median V_{oc} in comparison to the single slot configuration. Nevertheless, high peak energy conversion efficiency of $\eta = 22.5\%$ with a $V_{oc} = 694$ mV are reached for this group with a highly increased throughput potential. Further investigations are necessary to identify the reason for the loss in V_{oc} for the stacked wafers compared to the single slot configuration. From the slight increase in j_{0e} shown in Fig. 8, a reduction in V_{oc} of only 1 to 2 mV is expected. This holds for the best cell results but not for the median values. The stack configuration exhibits a slightly reduced pseudo *FF* (*pFF*) of about $0.4\%_{abs}$, which might be related to defects induced by the manual vertical stacking with four wafers in one slot. Table II shows calibrated *IV* measurements of the best cells from each group measured at Fraunhofer ISE CalLab PVCells using Pasan GridTouch unit with 30 wires on a golden, reflective chuck with a full area rear side contact. These measurement shows $V_{oc} >= 700$ mV for each diffusion configuration resulting in energy conversion efficiencies $\eta > 23\%$. The reference processing yields $\eta = 23.6\%$, followed by the APCVD in single slot diffusion configuration with $\eta = 23.3\%$. The APCVD in stack diffusion configuration with highly increased throughput potential and cost- and energy-efficient emitter formation yields $\eta = 23.1\%$. Results for stacking of wafers during thermal processing from [18], [26], [27], [28] showed no significant negative influences on the doping and emitter dark saturation current density. This shows that there is still potential to overcome the gap in V_{oc}/η for

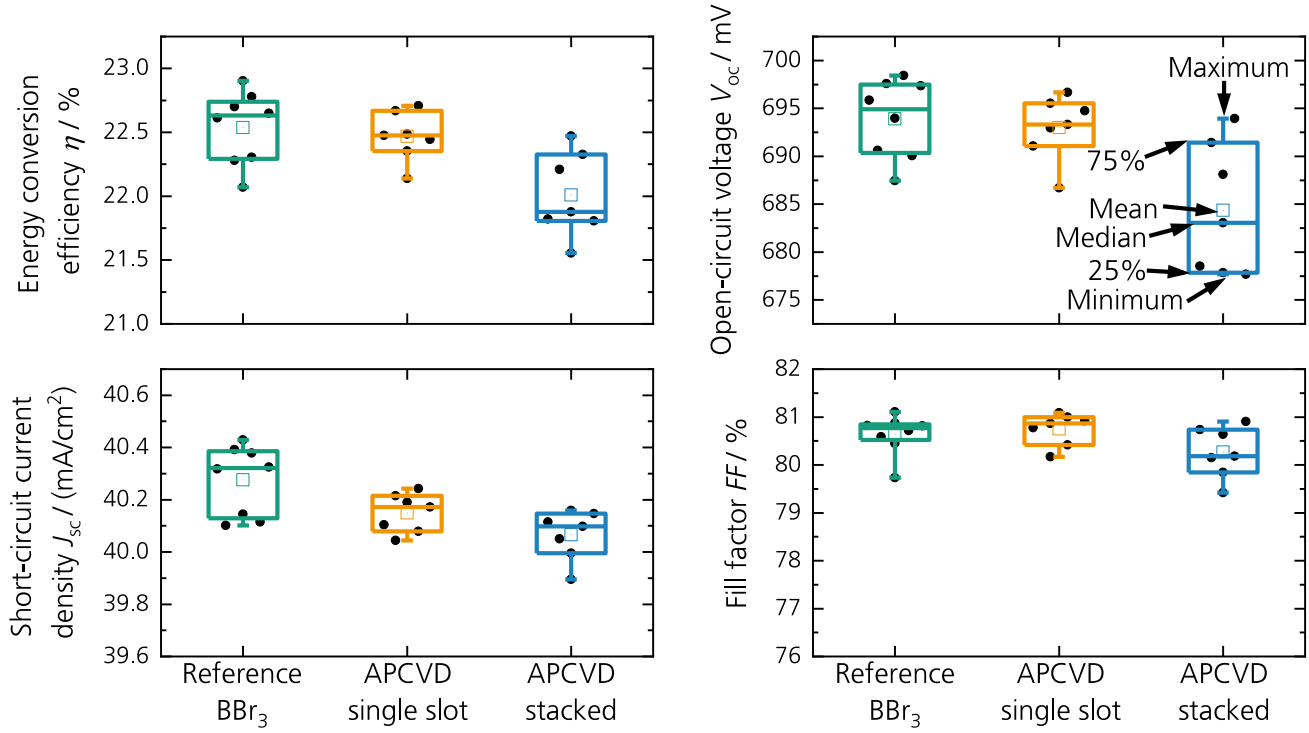

Fig. 9. *IV* parameters measured with an industrial cell tester for the three groups with different emitter formation processes: the reference processing using BBr_3 diffusion, as well as BSG deposition by APCVD with subsequent thermal diffusion process in single slot and stacked. The meaning of the box plots is exemplary explained on the top right data set.

TABLE II
CALIBRATED *IV* PARAMETER OF THE BEST SOLAR CELLS FOR THE THREE GROUPS WITH DIFFERENT EMITTER FORMATION PROCESSES MEASURED BY FRAUNHOFER ISE CALLAB PVCELLS USING A PASAN GRIDTOUCH UNIT WITH 30 WIRES ON A GOLDEN, REFLECTIVE CHUCK WITH A FULL AREA REAR SIDE CONTACT

Diffusion Configuration	Calibrated *IV* parameter			
	V_{oc} / mV	j_{sc} / mA/cm²	*FF* / %	η / %
BBr_3 Reference	705	40.9	81.6	23.6
APCVD BSG Single Slot	702	40.8	81.4	23.3
APCVD BSG Stacked	700	40.7	81.1	23.1

the stack diffusion approach, which will be addressed in future work.

V. CONCLUSION

In this article, we present an approach for high throughput boron emitter formation with predeposited BSG layers and stack diffusion for TOPCon solar cells. COO calculations show that this approach reduces the COO for the boron emitter diffusion by 19% to 25%, compared to the reference gas phase diffusion. Moreover, a reduction of the specific power consumption of up to 55% enables an energy-efficient boron emitter formation. The process development of the stack diffusion process shows that 20 nm thin and lowly doped APCVD BSG layers are sufficient for the emitter formation, allowing a more sustainable process consumable usage. Furthermore, the development reveals that a proper stack diffusion process with controlled temperature and oxygen usage is necessary to reach uniform doping over the wafer surface. M2 sized wafers from the stack diffusion process reach a sufficient uniformity of the emitter sheet resistance with a relative standard deviation of $\sigma = 3.5\%$ over the wafer area. With this process, emitter dark saturation current densities of $j_{0e} = (36 \pm 5)$ fA/cm² at $R_{sh} = (97.5 \pm 3.6)$ Ω/sq for stacked samples are reached slightly higher than for unstacked single slot wafers. With this approach, we reach an efficiency of up to $\eta = 23.1\%$ (CalLab) for TOPCon solar cells with a highly increased throughput potential. Our results still show a performance gap compared to BBr_3-diffused reference solar cells, which requires further investigation. With further optimization of the thermal diffusion process for these layers, further efficiency improvements will be possible.

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