Development of a 16.8% Efficient 18-μm Silicon Solar Cell on Steel

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Abstract—**Thin crystalline silicon solar cells have the potential to achieve high efficiency due to the potential for increased voltage. Thin silicon wafers are fragile; therefore, means of support must be provided. This paper reports the design, development, and analysis of an 18-μm crystalline silicon solar cell electrically integrated with a steel alloy substrate. This ultrathin silicon is epitaxially grown on porous silicon and then transferred onto the steel substrate. This method allows the independent processing of each surface. The steel substrate enables robust handling and provides a conductive back plane. Three groups of cells with planar and textured structures are compared; significant improvements in J_{sc}, V_{oc}, and fill factor (FF) are achieved. The best cell shows an efficiency of 16.8% with an open-circuit voltage of 632 mV and a short-circuit current density of 34.5 mA/cm^2.**

Index Terms—Steel substrate, thin silicon solar cell.

I. INTRODUCTION

THE advantage of thin crystalline silicon (c-Si) solar cells is that they not only use less silicon but also offer the potential of achieving higher performance compared with conventional wafer approaches due to higher open-circuit voltages. In the 1980s, Wolf predicted that the limiting efficiency was 25%. In his calculations, the optimum cell thickness was in the range of 50–150 μm, and practical light trapping including a textured front surface and an optical internally reflecting back surface was used [1]; however, there was some loss of light from the front surface with this light-trapping scheme. Spitzer *et al.* predicted a theoretical upper limit efficiency of 27% on a 15-μm silicon cell, in which perfect front and back mirrors were assumed; therefore, there was no light escaping from either surface [2]. However, practically these higher efficiencies have not been realized. An efficiency of 9.75% has been reported for a 25–30-μm-thick silicon solar cell on a metallurgical grade substrate

[3], and an efficiency of 9.5% has been reported on a 20-μm silicon cell on a steel substrate [4].

Since 1990, many thin silicon technologies have been reported, such as mechanically or chemically thinning [5], [6], high-temperature deposition or recrystallization on foreign substrate [7], [8], low-temperature crystallization polycrystalline thin silicon [9], [10], amorphous silicon [11], epitaxial growth on silicon [12], and epitaxial growth on a porous silicon layer [13], [14]. The porous silicon layer can also enable transfer of the epitaxial layer [15]–[17]. Porous silicon layer transfer has demonstrated high efficiencies. A 43-μm free-standing silicon solar cell formed by porous silicon showed a confirmed efficiency of 19.1%; this solar cell had a passivated emitter and rear cell (PERC) both-sides-contacted structure, and its improved performance was mainly due to the improved surface passivation by aluminum oxide [14]. However, such a free-standing thin silicon wafer is fragile and difficult to handle. Another 43-μm silicon solar cell made by porous silicon layer transfer was attached onto a resin and fiber carrier and had a confirmed efficiency of 20.1%. The area of this cell was 242.6 cm^2, and it had an all-back-contact design: Both emitter and base contacts were processed on what became the rear surface before layer transfer [13], [18].

The design of our ultrathin silicon (UTSi) solar cell on steel substrate not only leads to a robust device but also enables the independent processing of each surface. One side of the thin silicon is processed while it is attached to the host wafer. Then, thin silicon is bonded to a steel carrier that provides rigidity and integrates one of the electrical conductors. After transferring the wafer to the steel, the other side of thin silicon is processed. The structure of this UTSi solar cell has been briefly described; the theoretical maximum open-circuit voltage and efficiency were calculated by PC1D [19], and the *I–V* curve and external quantum efficiency curve of the light-trapped cell were presented [20]–[22].

The contributions of this paper are as follows:
1) description of the design of the UTSi solar cell on steel;
2) further analysis of its potential performance;
3) description of the fabrication process of this solar cell;
4) comparison of planar cell and light-trapped solar cells;
5) comparison with other layer transferred cells.

II. DESIGN

Fig. 1 illustrates the generic structure, which includes the requirements and features for the design of the UTSi solar cell. The requirements and features include the following [22]:
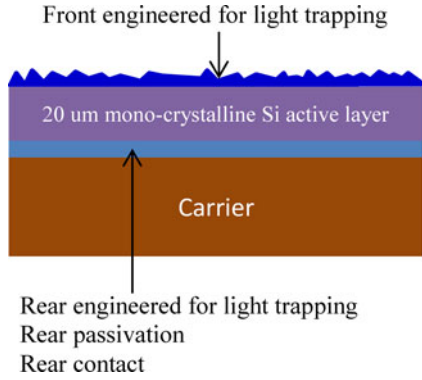1) a thin monocrystalline Si active layer;

Fig. 1.   Generic structure of ultra-thin Si solar cell.

2) conductive bonding to conductive carrier. This enables simultaneous back contact formation and bonding to a robust substrate;

3) independent processing of both of the thin wafer surfaces. This enables the independent passivation and light-trapping implementation on each surface.

PC1D [19], [23] is used to calculate the upper limit efficiency and open-circuit voltage of a 20-μm silicon solar cell. Lifetimes of the n+ front surface field (FSF) layer and p+ emitter of 10 μs and a lifetime of the n base of 1000 μs are assumed. The maximum current density (J_{sc}) used in this model is 39.5 mA/cm^2, which was calculated, elsewhere, by assuming a Lambertian back reflector [20]. The modeled upper values of V_{oc} and efficiency are 767 mV and 25.4%, respectively, as shown in Fig. 2. These values are plotted as a function of surface recombination velocity (SRV).

In addition to the PC1D model, first principle calculations are used to calculate V_{oc}. We first separate the surface recombination from bulk recombination by assuming SRV (s_n, s_p) to be 0 cm/s so that there is only bulk recombination in the base (J_{0b}) and emitter (J_{0e}). The J_0 equation becomes $J_0 = J_{0b} + J_{0e} = \frac{qD_n n_i^2}{L_n N_A}*\tanh\left(\frac{W_p}{L_n}\right) + \frac{qD_p n_i^2}{L_p N_D}*\tanh\left(\frac{W_n}{L_p}\right)$, where N_A and N_D are doping densities; L_n and L_p are minority carriers diffusion lengths; W_p and W_n are the thickness; S_n and S_p are minority carriers surface recombination velocities; D_n and D_p are minority carriers diffusivity at p and n silicon, respectively; and n_i is the intrinsic concentration.

J_0 is determined by $\frac{W_p}{L_n}$ and $\frac{W_n}{L_p}$, the ratio of thickness over diffusion length. The maximum V_{oc} is 758 mV for a 20-μm cell, with an n base 18-μm, 5e15 cm^{-3} and a lifetime of 1000 μs, a p+ emitter 1 μm, 5e17 cm^{-3} and lifetime of 10 μs. No n+ FSF layer is considered in this calculation.

Fig. 2 shows the effect of SRV on the voltage and efficiency. Our experimental results indicate that values around 1000 cm/s for the SRVs are probable for our devices and can be a limit to the higher performance of our present structures.

III. DEVICE STRUCTURE AND FABRICATION

Fig. 3 shows the detailed structure of the UTSi solar cell on steel substrate. Each wafer surface is independently processed
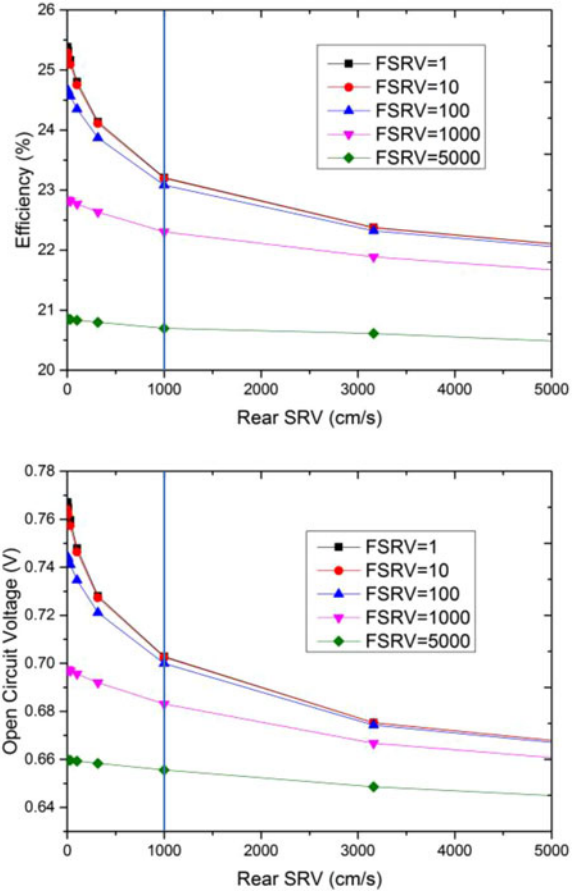

Fig. 2.   Efficiency and open-circuit voltage as functions of SRV from PC1D modeling. FSRV indicates front SRV.
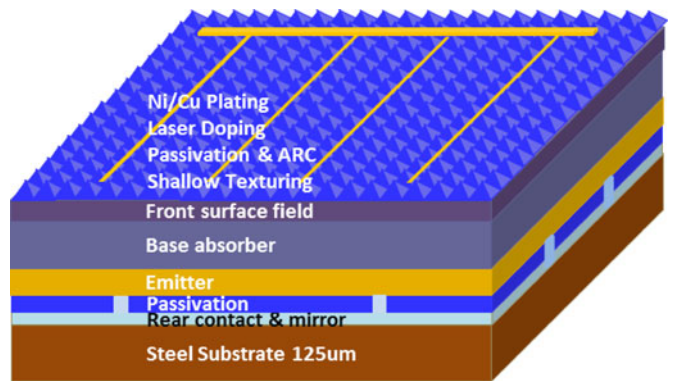
Fig. 3.   Diagram of the ultrathin silicon solar cell on steel substrate.

the same as conventional thick wafers including surface passivation, light trapping, and contact integration.

The process flow of this cell is shown in Fig. 4. The first four steps are performed at AmberWave including the porous silicon layer formation on p+ wafer, the epitaxial growth on porous silicon, the rear surface passivation and metallization, the bonding and transfer, resulting in an "enhanced wafer." This "enhanced wafer" is sent to UNSW for solar cell completion, testing, and analysis. The finishing steps at UNSW include removal of the

Fig. 4. Fabrication flow of UTSi solar cells. First four steps are finished in AW, and the "enhanced wafer" is sent to UNSW for solar cell completing.
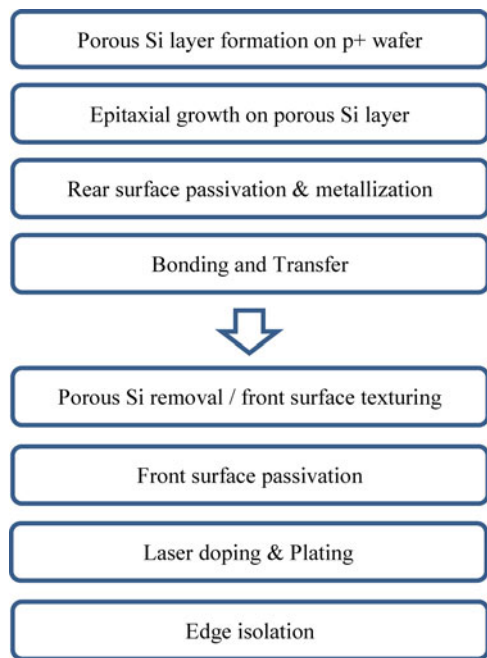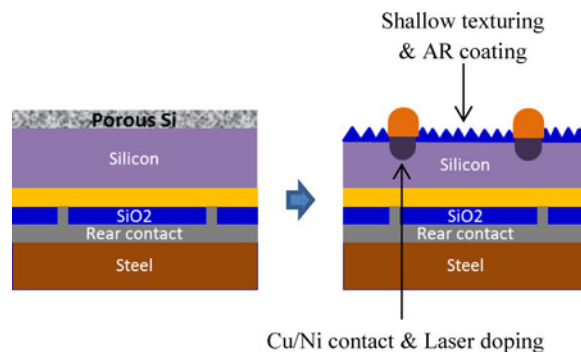

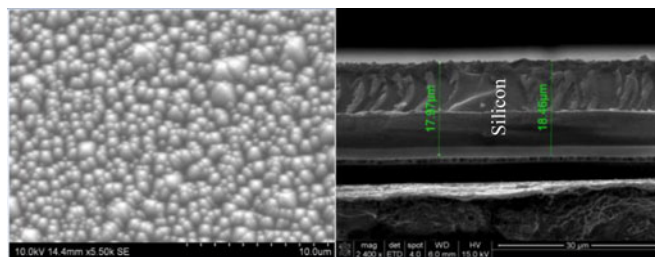Fig. 5. Illustration of the work at UNSW. (Left) Structure of the enhanced wafer. (Right) Finished solar cell.

Fig. 6. SEM image of shallow textured front surface (left) and the cross section of a textured thin silicon solar cell (right).

porous silicon, shallow texturing of the front surface, the front surface passivation, the laser doping and contact plating, and the edge isolation.

A. Process at AmberWave

The semiconductor layers are epitaxially grown by reduced pressure chemical vapor deposition on porous silicon on heavily doped p-type wafers at temperatures above 1000 °C [24]. This approach was first described by Canon in 1994 [15]. These layers include a 2-μm n+ FSF (5e17 cm^{-3}), 18 μm n-type base (5e15 cm^{-3}), and 1-μm rear p+ emitter (5e17 cm^{-3}). The n+ layer is designed to form an FSF and reduce the series resistance due to current lateral flow. The 18-μm n base is the absorber layer; its low doping density (5e15 cm^{-3}) allows long minority carriers lifetime so that photogenerated carriers can be collected before recombining. The 1-μm p+ emitter forms a rear junction. The design includes shallow texturing on the front (top) surface for light trapping. This texturing is done after the epi layers are grown and transferred, which leads to a rear junction being required.

The rear surface process includes thermal oxide passivation, limited area aluminum contact, and a metal mirror. A conductive metal bond and steel substrate are added afterwards. This is similar to a PERC [25] solar cell rear surface design whose mostly passivated rear surface can lead to a high open-circuit voltage. The thermal oxide provides passivation and is part of the mirror structure. The oxide is patterned for limited area rear contacts using photolithography. The coverage of these openings is 0.56% of the rear surface with vias of 15 μm × 15 μm with 200-μm spacing. The Al rear contact and p+ emitter form an ohmic contact without firing; the 1-μm 5e17 cm^{-3} p+ emitter

leads to a low series resistance. Al together with SiO$_2$ forms a reflective rear mirror that confines light within silicon when combined with the front texture.

The conductive bond from AmberWave integrates the UTSi with the steel substrate. The 125-μm steel substrate acts as a carrier as well as a rear electrode. The thermal expansion coefficient of the steel alloy sufficiently matches silicon over the range of processing temperature. The proprietary conductive bonding layer, which can be deposited using high-volume production methods, will withstand high temperature processing during subsequent process steps such as during the creation of the passivation and ARC layers. Following the bonding process, separation is initiated manually, resulting in a transfer of the UTSi solar cell structure onto the conducting steel substrate. This results in an "enhanced wafer."

B. Process at the University of New South Wales

Fig. 5 illustrates the work at UNSW. First, the front surface porous silicon layer is removed in an NH$_4$F and H$_2$O$_2$ solution. The porous silicon removal process results in a polished surface and, it does not etch the silicon layer underneath. Then, the front surface is etched to form shallow texturing in a KOH solution with isopropanol and polyethylene glycol. The shallow texturing step etches away around 2 μm silicon and results in 18-μm silicon base layer, thus much of the n+ layer is removed during this process. The average diameter of pyramids is in the range of 1–2 μm. This surface is shown in Fig. 6.

The front surface is then passivated by 75-nm silicon oxynitride (SiON) with a refractive index of 2.0 deposited by PECVD [26], which provides surface passivation, as well as an

TABLE I
PERFORMANCE OF 20-μm PLANAR CELLS VERIFIED BY NREL

ID	Area (cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF%	Eff%
TS464-2	1.21	609.9	26.55	72.5	11.8
TS464-3	1.21	612.2	26.86	73.7	12.1

TABLE II
PERFORMANCE OF LIGHT-TRAPPED CELL CELLS AND BEST VALUES OF SOLAR
CELLS MEASURED BY NREL

ID	Aperture area (cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF%	Eff%
TS507-1	0.99	606.8	33.98	73.1	15.1
TS507-2	0.99	606.4	33.85	73.8	15.1
MS197-4	4.00	632.2	34.49	77.2	16.8
MS197-5	4.00	640.4	33.81	76.8	16.6
Best values	–	642.3	34.49	78.0	–

These cells were measured using apertures.

antireflection (AR) coating. Contacts are formed by first selective laser doping [27]. The locally heavy doping resulting from the laser doping reduces the contact resistance. The dielectric layer opening is in between 15 to 20 μm. Ni and Cu are plated through the dielectric openings, which leads to the self-aligned light-induced plating in the subsequent step. In the laser doping step, a phosphoric acid layer is applied, and a 532-nm laser beam is used to transmit through both the phosphoric acid layer and the SiON coating into the silicon. Silicon is brought to its melting point temperature after absorbing the laser energy to create a selective heavily doped region [28]. The laser doping step patterns the front contact and leads to the local heavy doping. The Ni/Cu contact is plated using self-alignment from the laser removal of the SiON and light-induced plating [29]. There is a deglazing step before Ni plating to strip away any oxide formed within the laser opening. The deglazing step needs to be optimized for good plating without affecting AR coatings. After metallization, these samples are isolated by laser cutting from the rear surface followed by an HF: nitric: acetic acid edge clean.

The last step is edge isolation which is composed of two steps. 1) A laser cuts through the steel substrate from the rear side; 2) the sample is cleaved along the laser cut line; and 3) the cleaved edges are cleaned in diluted HNA solution, during which the front surface is protected by photoresist, followed by photoresist removal.

IV. RESULTS AND DISCUSSION

A. Results of Planar and Light-Trapped Solar Cells

1.1×1.1-cm^2 planar devices of thin silicon on steel were fabricated; Table I shows the performance of two planar (i.e., nontextured) solar cells whose efficiencies were confirmed by the National Renewable Energy Laboratory (NREL). The rear steel acts as the rear electrode during the measurements.

Front surface shallow texturing minimizes the front surface reflectance, redirects photons, and traps photons reflected by the planar rear mirror. Table II shows the performance of such light-trapped cells and best single parameters measured, with J_{sc} much higher than in Table I. Fig. 7 plots the I–V curve measured by the NREL, and Fig. 8 plots EQE and reflection curves of both the planar cell TS464-3 and light-trapped cell MS197-4.

B. Discussion of Results

Two MS197 cells have significantly higher V_{oc} than the rest of the planar cells TS464 and textured cells TS507. This difference is reflected by their PL image as well, as shown in Fig. 9. A higher V_{oc} corresponds to a higher PL counts, and *vice versa*.
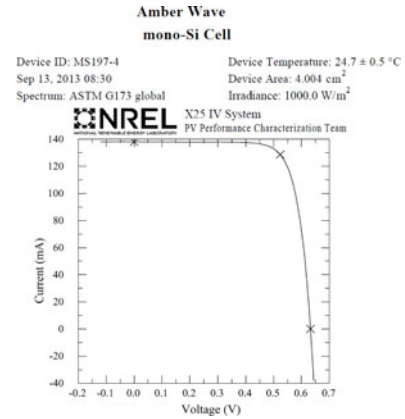

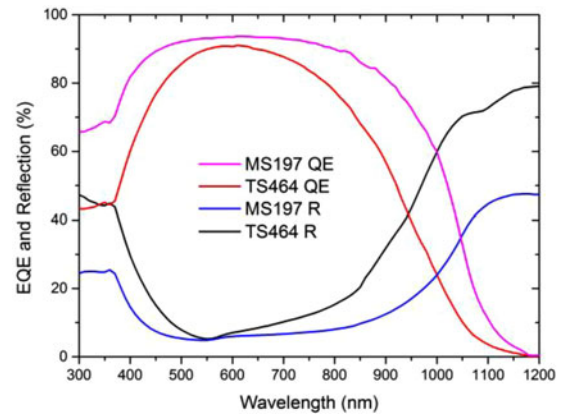Fig. 7. I–V curve of MS197-4 measured by NREL.

Fig. 8. EQE and reflectance curves of both planar cell (TS0464-3) and light-trapped cell (MS197-4).
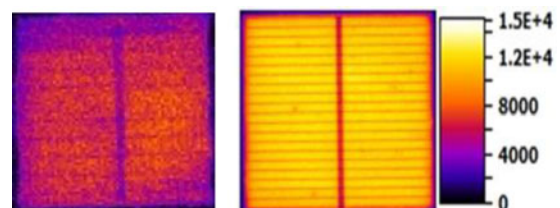

Fig. 9. PL images of TS507-2 (left) with an average PL counts 4100 s^{-1} and MS197-4 (right) with an average PL count 10 400 s^{-1}.
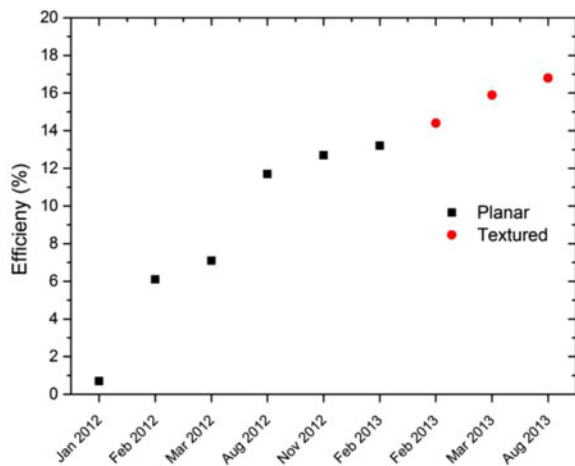
Fig. 10.   Efficiency improvement of thin silicon solar cell on steel verses time.

Fig. 11.   Short-circuit current densities reached by kerfless thin-film c-Si solar cells by porous silicon layer transfer.

These textured cells experienced the same fabrication process except the epi growth with all key steps monitored. The V_{oc} increase results from the improved material quality with reduced stacking-fault density (SFD) from 10^6 to 10^4 cm^{-2}. Thus, the density of stacking faults for MS197 is approximately 1% of those for TS507. The quality of epitaxial layer is related to the thickness and porosity of porous silicon stack layers [30] and subsequent H$_2$ annealing conditions [31]. After porous etching, the surface of the wafer has a mesoporous structure. This structure does not lend itself to high-quality epitaxy, resulting in a form of epitaxial lateral overgrowth across the nm sized porous openings causing high defect density. Therefore, a restructuring of the surface was required to create a smooth uniform layer for the subsequent growth. This restructuring occurs through hydrogen anneal, allowing the surface pores to seal, forming a template for homoepitaxy. The effectiveness of the anneal was quantified by the reduction in SFD post growth, seen via optical microscopy. During the course of the anneal experimentation, the SFD decreased almost two full orders of magnitude to ultimately 5e3 cm^{-2}. While lower SFD should be possible with this approach, the electrical performance increases began to show a plateau below a SFD of 1e4 cm^{-2}. A lifetime as high as 195 μs was reported by the Interuniversity Microelectronics Centre (IMEC) on a 50 μm epilayer with a doping density 10^{16} cm^{-3} [30]. Although we did not directly measure the lifetime of transferred epitaxial thin silicon, a same epi process on monitor wafer (single crystal FZ) showed lifetimes of 500–1000 μs. According to our simulation, V_{oc} of UTSi solar cell starts to saturate at a lifetime of 70 μs, which is equivalent to a diffusion length of 285 μm, or 15.8 times the thickness of the 20-μm base layer. Larger lifetime would not increase the performance significantly.

The light-trapped cell has better EQE response at both short and long wavelengths than the planar cell owing to the improved light trapping. The J_{sc} increase of 7.59 mA/cm^2 (28.2%) from TS464-3 to MS197-4 is mainly due to the effect of light trapping.

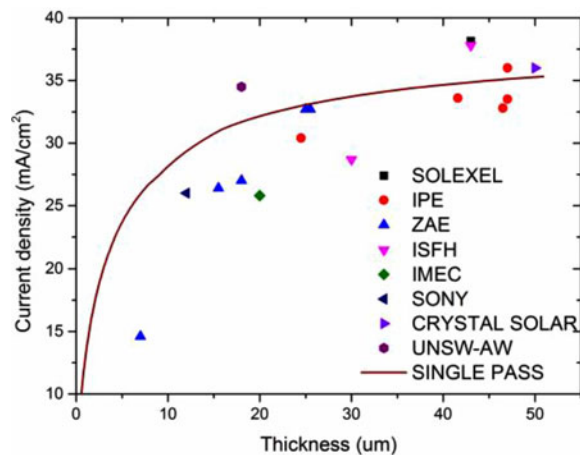Another difference between planar cell and textured cell is the n+ FSF layer. To investigate if the n+ FSF layer caused performance differences, planar and textured cells were fabricated using material from the same wafer. These two structures did not have a significant difference in their PL, V_{oc}, and IQE at short wavelength. Thus, we conclude that the n+ FSF layer did not affect the performance.

MS197 cells have higher fill factor than both TS464 and TS507 cells. The larger area cells MS197 have less edge damage (in part due to the larger size) leading to higher shunt resistance. In addition, MS197 cells added an additional Ni sintering process which formed low resistivity nickel silicide, resulting in lower series resistance [32].

Fig. 10 plots the efficiency improvement of the UTSi solar cell with time. At the beginning period, planar devices demonstrated a confirmed efficiency of 12.1%. Then, light trapping increased the efficiency to 15.1%. After that, the improved Si and processing led to a confirmed efficiency of 16.8%.

C. Comparison With Other Layer Transferred Solar Cells

Fig. 11 summarizes the results reported on thin Si solar cells by epi on porous Si and layer transfer. The results are reported in work from the Institute of Physical Electronics, University of Stuttgart [33], [34], Bavarian Center for Applied Energy Research [35]–[38], the Institute for Solar Energy Research Hamelin [14], [39], Solexel [13], Crystal Solar [40], IMEC [41], and Sony [42]. The solid line is the current density expected from a single pass that assumes that the effective optical path length equals the physical thickness of the solar cell and all absorbed photons are collected. The University of New South Wales—AmberWave represents the J_{sc} of MS197-4, which is 34.49 mA/cm^2, which is higher than the single pass line and higher than these from other cells with similar thicknesses.

There are two groupings of cell thicknesses: one at 40 to 50 μm, which can be described as "thick" in this context, and one at less than 20 μm, described as "thin." The UTSi solar cell efficiency is 16.8%, which is the highest efficiency for epi on porous layer with transfer cells thinner than 40 μm. Fig. 12 plots efficiencies of all these cells.
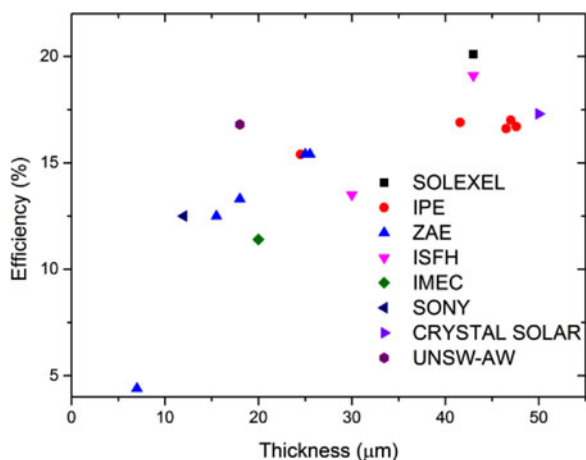
Fig. 12.   Efficiency of thin-film c-Si solar cells formed by epi on porous silicon and layer transfer.

D. Future Plan

The greatest opportunity for efficiency increase is for voltage. Our model suggests SRV for both surfaces around 10^3 cm/s, and reduction of both of these to 100 cm/s can lead to a 7.5% (51.5 mV) increase in voltage. Further voltage increases are expected from reduced recombination on rear surface by replacing SiO_2 with advanced passivation layer and reduced surface damage by the laser doping process. This improved laser process can also lead to increased fill factor, and the front surface reflection can be reduced with a better AR coating and finer grid lines. The combination of these can lead to efficiencies in excess of 20%.

V. Conclusion

This paper has described the design, development, results, and analysis of a UTSi on steel solar cell. High performance is predicted on a 20-μm silicon solar cell according to our modeling. Improved Si material and improved processing led to a confirmed efficiency of 16.8%. Its efficiency of 16.8% and J_{sc} 34.49 mA/cm^2 are significantly higher than those previously reported in solar cells with similar thicknesses.

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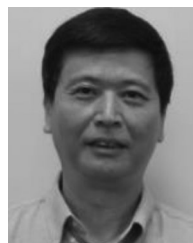
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