Semitransparent Perovskite Solar Submodule for 4T Tandem Devices: Industrial Engineering Route Toward Stable Devices

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Abstract—Perovskite technology has been advancing at unprecedented levels over the past years, with efficiencies reaching up to 26.1%. State-of-the-art results are obtained on a very small area scale (<0.1 cm²), by adopting high materials wasting processes not compatible with industry and with market exploitation. Silicon is a well-established technology and one of the advantages of perovskite is its ability to pair with silicon forming a tandem device that extracts charges reducing transmission and thermalization losses. In this work, we focused on finding a strategy to fabricate 15.2×15.2 cm² perovskite modules by using blade/slot-die coating and avoiding any spin coating deposition. Furthermore, we optimized the indium tin oxide top electrode deposition by adjusting the sputtering process and buffer layer deposition; finally, we focused on light management by applying an antireflective coating. We obtained a semitransparent and a tandem silicon-perovskite module in a four-terminal (4T) configuration over 225 cm² (4T configuration) with 13.18% and 20.91% efficiency, respectively, passing International Summit on Organic PV Stability ISOS-L1 (under continuous light soaking in the air) test with a remarkable T₈₀ of 1459 h.

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Index Terms—Four-terminal (4T) architecture, perovskite/ silicon tandem solar modules, photovoltaics (PVs), printing, semitransparent perovskite solar module (ST-PSM).

I. INTRODUCTION

DEROVSKITE solar cells (PSCs) reached an impressive efficiency of up to 26.1% in only one decade of research [1]. Perovskite strength lies in the possibility to tune optoelectronic properties according to the field of application and on the solution-based fabrication process suitable for large-scale industrialization [2], [3]. In this context, semitransparent perovskite solar cells (ST-PSCs) have attracted the interest of photovoltaic (PV) community, owing to their multiple applications, from building integrating PVs to tandem devices [4]. The research on perovskite/silicon-based tandem cells is a very hot topic nowadays, with record efficiencies' announcements succeeding in a very short time. Tandem solar cells, which are formed by two or more semiconductor materials to capture a wider spectrum of sunlight, come in various configurations, notably two-terminal (2T) and four-terminal (4T) designs. The 2T configurations entail a monolithic integration where the PV layers are connected in series, demanding stringent current matching but benefiting from simpler external circuitry. The 4T configurations, however, feature separate external connections for each cell layer, eliminating the need for current matching and allowing for the independent optimization of each layer at the cost of more complex circuitry. The 2T configurations offer simplicity and potentially lower manufacturing costs but require current matching and uniform layer conformality, which can complicate fabrication and limit device efficiency. On the other hand, 4T configurations eliminate the need for current matching and allow for separate optimization of each cell, leading to potentially higher efficiencies [5]. The use of a textured substrate in 2T tandem configurations introduces heightened complexity in achieving uniform layer conformality during fabrication [6], [7]. While evaporation techniques are typically advantageous for achieving conformal deposition, they tend to be energy intensive, resulting in elevated energy consumption that impacts the energy payback time and the overall carbon footprint of the product. On the other hand, the traditional 4T designs, while offering advantages, come with the drawback of requiring twice the number of inverters compared with single junction and 2T tandem modules. This increased demand for power electronics

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24 20 4-Terminal Devices 3 16 12 8 4 0 100 200

Large Area (≥1 cm² a.a.)

Small Module (21 cm² a.a.)

Fig. 1. State-of-art table for ST-PSCs and PSM and 4T devices efficiency.

Active Area [cm²]

raises the total cost, especially when considering that the balance of system cost surpasses that of module fabrication [8], [9], [10].

One significant challenge in the development of tandem devices involves the comparison between 2T and 4T configurations. The absence of current matching requirements and layer conformality limitations positions 4T tandem configurations as advantageous [11]. In 4T devices, each cell is independently connected to an inverter and extracts power separately from the incident light. In this case, the efficiency of the tandem device is the sum of the top cell and the bottom cell, as filtered by the top cell. The 4T tandem devices represent a promising choice because of the separate fabrication processes of top and bottom cells. For large-area devices, fundamental topics, such as scalability and module fabrication, for tandem technology have not yet been sufficiently explored in the scientific community. Only a few works in the literature report semitransparent cells and modules fabrication with 4T applications with a perovskite bandgap < 1.7 eV (see Fig. 1). Dewi et al. [12] made the highest efficient solar cells in this configuration using 1.58 eV triplecation perovskite (PVSK) with a power conversion efficiency (PCE) for the 4T tandem of 25.5%; Jaysankar et al. [13] report a 4T tandem efficiency of 20.2% on methylammonium lead iodide (MAPI) minimodule (4 cm^2 aperture area) with an indium tin oxide (ITO) counter electrode and, according to our knowledge, no works are present for 4T devices on submodule scale; Sofia et al. [14], for example, explore the market implication for perovskite/silicon tandem configurations (4T and 2T). From their study, it emerges that 4T terminals can have plenty of room to grow, especially with less efficient multicrystalline silicon considering the levelized cost of electricity. With respect to this, 2T devices suffer from many evaporation steps required to have a conformal deposition on textured silicon and the entire cost of the fabrication cannot benefit from this processing method. On the other hand, perovskite devices in 4T devices can be entirely made by solution processes till semitransparent electrode, making them more reliable for large-area scale production [15]. Moreover, for rooftop market scenarios,

a tandem using a high-cost, high-efficiency bottom cell, despite achieving a higher efficiency, is likely not economically favorable compared with its subcells or compared with the low-cost tandem. This finding stands in contrast with much of the perovskite-silicon tandem device development and motivates research to explore lower cost, lower efficiency silicon bottom cells for tandems that may not achieve record efficiencies but are likely to be more commercially viable. Silicon-perovskite in 4T configuration should be considered more by the scientific community, exploring viable pathways for cost-effective fabrication production of this technology [14]. Despite the intriguing possibility of using low-cost bottom cells in tandems, our study focuses on Si heterojunction cells. This selection prompts a critical examination of the tandem configuration choice (2T versus 4T) and underscores the need to explore cost-effective fabrication pathways for silicon-perovskite in a 4T configuration. Our work aims to contribute to this exploration by delving into the scientific and economic aspects, striving for advancements that align with the evolving landscape of perovskite-silicon tandem device development.

In this study, we aim to advance the current state-of-the-art in 4T silicon/PVSK devices by expanding to a submodule size of 225 cm² [8]. The choice of a 4T configuration for our study stems from its flexibility in cell optimization and favorable technoeconomic aspects, particularly in integrating cells with different optoelectronic properties without the constraints of current matching. Specifically, our focus on silicon heterojunction (Si HJ) as the bottom cell leverages its high efficiency and mature technology, promising an effective synergy with perovskite top cells in enhancing tandem device performance.

We have thoroughly considered the challenges associated with the scaling-up process in this work, spanning from laser patterning (P1-P2-P3) to layer-by-layer deposition (ETL/PVSK/HTL) utilizing meniscus coating techniques and the ITO sputtering process. In this regard, the optimization of laser patterning is a crucial step to minimize contact losses and the inactive area between cells [9]. Concerning wet processes, we have employed blade coating and slot-die coating techniques in ambient air, which are the leading methods for scaling-up perovskite technology [10]. We have successfully produced high-quality perovskite films with an impressive efficiency of over 20% on a small area (0.09 cm² active area) [16] and above 16% for a 187 cm² active area module [17].

Transparent conductive oxides (TCOs) represent a key component in the fabrication of ST-PSCs and 4T devices must provide robust chemical stability, high-lateral conductivity, as well as transparency [18]. However, the usual method for TCO deposition, i.e., radio frequency (RF) magnetron sputtering, can induce damage to the underlying layers. Thus, the routes of tuning the deposition parameters and/or introducing a protective buffer layer must be followed to tackle the sputtering damage.

One of the main challenges of the developed fabrication process is to better fit in a production line from the perspective of an integration with silicon PVs. Indeed, the tunable gap of perovskite makes it suitable to be employed as the top cell in a tandem device, where the bottom cell is represented by the well-established silicon technology. Among the various silicon technologies, the most efficient one is amorphous silicon/crystalline Si HJ [19], which held the record conversion efficiency for a single-junction solar cell of 26.8% [20]. Based on these considerations, it follows that coupling perovskites with silicon HJ represents a promising option for tandem configuration.

Our large area modules, obtained by the out-of-the-glovebox meniscus process, are well suited to be the top semitransparent part of a tandem device, able to filter a whole 240 cm² silicon solar cell. We were able to fabricate a semitransparent PVSK solar submodule on a 225 cm² substrate with an efficiency of 13.18%. We characterized the module by electroluminescence (EL) mapping for uniformity assessment and stressed it under a light soaking test according to international summit on organic PV stability (ISOS)-L1 for 1459 h. Finally, we got 20.91% efficiency in 4T tandem with c-Si.

II. MATERIALS AND METHODS

A. Materials

All materials were used as received without purification as follows: tin oxide, SnO2 (Alpha Aesar 15% in H2O colloidal dispersion), lead iodide, PbI2 (Sigma-Aldrich, 99.999%), lead bromide, PbBr₂ (Sigma-Aldrich, 98%), cesium iodide, CsI (Sigma-Aldrich, 99%), formamidinium iodide, FAI (Great-Cell Solar), formamidinium bromide, FABr (GreatCell Solar), methylammonium bromide, MABr (GreatCell Solar), phenethylammonium iodide, PEAI (Dyenamo) spiro-MeOTAD (Borun, 99.5%), lithium bis- (trifluoromethanesulfonyl)imide, LiTFSI (Sigma-Aldrich, 99.95%), 4-tert-butylpyridine, TBP (Sigma-Aldrich, 96%), cobalt salt, FK209 (GreatCell Solar, 98%), gold, Au (Sigma-Aldrich 99.99%), N,Ndimethylformamide, DMF (Sigma-Aldrich, anhydrous), dimethyl sulfoxide, DMSO (Sigma-Aldrich, anhydrous), ethanol, EtOH (Sigma-Aldrich, 96%), acetone (Sigma-Aldrich), isopropanol, isopropanol (IPA) (Sigma-Aldrich, anhydrous), and chlorobenzene (Sigma-Aldrich, anhydrous).

B. Fabrication of Perovskite Solar Modules (PSMs)

Substrate preparation: Fluorine-doped tin oxide (FTO) glass substrates (7 Ω /sq., Pilkington) were patterned (P1) to form 22 series-connected cells by a nanosecond raster scanning laser ($\lambda = 355$ nm, Nd:YVO4 pulsed at 80 kHz, and fluence = 10.2 J/cm²). The substrates were cleaned with a soap/water solution and then with acetone, ethanol, and 2-propanol. After solvent washing, the samples were transferred to a UV-ozone lamp for 30 min to eliminate the organic residual.

Electron transport layer (ETL): Before tin oxide deposition, each substrate was treated for 10 min in a UV-ozone lamp to improve wettability of aqueous solution, then a colloidal solution of tin oxide diluted in water 2% v/v (from 15% colloidal solution Alfa Aesar) was deposited by slot-die coating technique in ambient air according to Vesce et al. [17], [21]. Then, the film was annealed in air at 150 °C for 30 min to obtain about 40-nm-thick SnO₂. *Perovskite and passivating layer*: The substrates were treated under a UV-oven ozone lamp to improve the wettability prior to the PVSK deposition. The 3C PVSK 1.1 molar solution $[Cs_{0.05}(MA_{0.17}FA_{0.83})_{0.95}Pb(I_{0.83}Br_{0.17})_3$ in DMF/DMSO] (Lead Iodide from TCI Co., Ltd; CsI, FAI, and MABr from GreatCell Solar) was deposited by hybrid blade/slot-die coating (ambient air, 30% RH) one-step technique assisted by a heated airflow [3]. Then, 5 mM phenethyl ammonium iodide (Dyenamo) solution in IPA was slot-die coated according to Vesce et al. [21].

Hole transport layer (HTL) and top electrode: The hole transport material (HTM) Spiro-OMeTAD solution (60 mM, Sigma Aldrich) in chlorobenzene (the molar ratio between the dopants and the Spiro-OMeTAD is 0.5 and 3.3 for lithium bis(trifluoromethanesulfonyl)imide and 4-tert-butylpyridine, respectively) was coated by an air-assisted slot-die method in ambient [21]. For the ST perovskite solar modules (ST-PSMs), buffer layers (molybdenum oxide, MoO_x , or gold, Au) were thermally evaporated on top of the HTL. The following step was the removal (P2) of the full stack (ETL/PVSK/PEAI/HTL) deposited on FTO from the vertical connection areas to series connect two adjacent cells with the subsequent electrode deposition. Substrates were transferred on a raster scanning laser for P2 process $(\lambda = 355 \text{ nm}, \text{Nd: YVO4} \text{ pulsed at } 80 \text{ kHz}, \text{ and fluence} = 182 \text{ mJ}$ cm⁻²). Afterward, the 120-nm-thick Au counter electrode was thermally evaporated in a high-vacuum chamber (10^{-6} mbar). In the case of ST-PSMs, a 100-nm-thick ITO layer was deposited by RF magnetron sputtering with a linear system by Kenosistec Srl. with In₂O₃/SnO₂ composition of 90:10 wt.%, base pressure of $5 \times 1e^{-6}$ mbar, process pressure $1.1 \times e^{-3}$ mbar, Ar flow rate = 40 sccm, and input power density from 0.26 to 0.4 W/cm². Finally, the counter-electrode P3 ablation was performed ($\lambda =$ 355 nm, Nd:YVO4 pulsed at 80 kHz, and fluence = 200 mJ cm^{-2}) to obtain the electrical insulation between the counter electrodes of adjacent cells. For the best-performing module, a 100-nm-thick MgF₂ layer was deposited by thermal evaporation on the glass side, as an antireflective coating (ARC). The patterned module shows 22 series-connected cells with 7.63 cm² cell area, 5.4 mm, 14 cm, and 500 μ m cell width, height, and dead area width, respectively, with a total active area of 168 cm^2 and a geometrical fill factor (GFF) equal to 91%. About 1 cm on two sides of the substrate was used for taking the contacts, defined as the busbars of the module.

Silicon-based HJ: Amorphous silicon/crystalline Si HJ solar cell used as a bottom cell in 4T tandem configuration is based on n-type CZ 1–5 Ω cm silicon wafer. Both sides are passivated by a thin intrinsic layer of a-Si:H, ~5 nm thick. Selective contacts are produced by (n)a-Si:H and (p)a-Si:H of about ~5 nm and ~15 nm thickness, respectively, completed by sputtered ITO and screen-printed silver grid of opportunely designed finger spacing for both sides. The cell area was 225 cm² for tandem characterization. The *J*–*V* characteristic of the bottom cell was measured under a continuous light WACOM class A sun simulator at AM1.5G under standard test conditions (STC) with thermal stabilization of samples. The whole solar cell was filtered by the semitransparent perovskite module. The external quantum efficiency (EQE) of the filtered HJ was measured with an in-house system with a modified setup for 4T tandem devices.



Fig. 2. (a) Process scheme of the fabrication of perovskite film deposition over $15.2 \times 15.2 \text{ cm}^2$. (b) Estimated effective mass of perovskite material on substrate per cm² and total mass of solution utilized for one perovskite deposition; the total amount (gray column) is normalized for each technique.

C. Film and Device Characterization

The PV characteristics and the maximum power point (MPP) were measured with a class A sun simulator (Sun 2000, Abet) at AM 1.5 1000 W/m² calibrated with an SKS 1110 sensor (Skye Instruments Ltd., Llandrindod Wells, U.K.); the system is equipped with a 2612 source meter (Keithley Instruments Inc., Cleveland, OH, USA) and a LabVIEW interface. A LabViEW/Python-based code manages the J-V and MPP tracking (MPPT) state. A standard perturb and observe tracking algorithm was used for the MPPT. The EL imaging on the module adopts a silicon charge couple device (CCD) camera. The illumination intensity was kept constant for the different measurements [22].

III. RESULTS AND DISCUSSION

The aim of the work is to fabricate an ST-PSM and investigate its application in tandem configuration surpassing the conventional laboratory process techniques, such as spin coating, by employing industrial-scalable methods along with cost-effective fabrication processes.

In this context, perovskite has a wide process window [24], [25], allowing us to focus on industrial scalable techniques that are feasible to be coupled with an established technology already in the market, such as silicon solar technology: To do so, we were able to fabricate ST-PSMs with the same size of a standard silicon modules, i.e., 6 in² (\sim 15.2 × 15.2 cm²).

The flow of the process is summarized in Fig. 2(a). All scalable techniques were used, in particular, SnO₂, perovskite, and Spiro-MeOTAD layers were deposited by slot-die coating, a technique that is already exploited in other commercialized products, such as thin film PVs, batteries, printed electronics, fuel cells, and so on [25], [26], [27]. The use of slot-die coating, in particular, for the perovskite layer is highly efficient in terms of materials usage and results in very low wastage levels of inks compared with other deposition methods, such as spin coating or spray and screen printing [24]. To make ST-PSMs, we replace the standard opaque top electrode conventionally used in PSC, such as gold, silver, carbon, or copper [28], [29] with ITO and TCOs. ITO is deposited by the sputtering technique, an industrial-scalable technique based on plasma activation and ion bombardment to hit the target, whose molecules, subsequently, deposit over the substrates [30]. However, the underlying layers can be affected by the ion bombardment and the UV plasma during the process. To protect the surface before sputtering deposition, a buffer layer of MoO_x or thin Au (2 nm) is deposited on the HTL by thermal evaporation, as shown in Fig. 2(a). All these five processes were chosen to limit material waste during the fabrication of ST-PSMs. To quantify the material waste, we conducted a study on the amount of wasted materials during perovskite deposition, comparing spin and blade/slot-die coating, as shown in Fig. 2(b). Our findings underscore a compelling observation: When evaluating the material required for a single perovskite deposition over a 15.2×15.2 cm² area, the utilization of blade/slot-die coating uses only 8.47% of the perovskite solution, in stark contrast to the 91.53% required by spin coating techniques, a standard common solution process technique. This methodology not only provides a substantial advantage in terms of material and cost savings during the fabrication process but also demonstrates an impressive reduction of over 90% in perovskite deposition requirements compared with conventional spin coating methods.

To verify the sputtering condition, ITO was sputtered directly on the Spiro-MeOTAD. Notably, the resulting J-V curve exhibited an S-shape, indicating the occurrence of sputtering-induced damage during the ITO deposition process, as shown in Fig. 3. It is known that the S-shape is mainly caused by the damage of ITO sputtering against Spiro-MeOTAD, increasing the overall device barrier height, proven also by equivalent circuit models [31]. For this reason, we investigated the use of a buffer layer to mitigate the sputtering damage effects. Molybdenum oxide (MoOx) was employed in other studies as a protective layer in n-i-p PSCs [32], [33], [34], [35]. Here, we showed that an ultrathin (<10 nm) evaporated MoO_x layer, as well as thin evaporated Au layer, is sufficient to protect the underlying layers since no S-shape was observed in the J-V curve of the MoO_x-based semitransparent device (see Fig. 3). The introduction of a buffer layer, such as MoO_x or thin Au (2 nm), enables to reach a fill factor up to 74.25%, compared with 47.38% when the buffer layer is not added before sputtering process. The final performance of the stack on a small area (0.09 cm²) reached 15.56% efficiency by using MoO_x, compared with 9.07% efficiency when a buffer layer is not employed.

The scaling up to ST-PSM was investigated by studying two different protective layers (MoOx and Au) on the full module



Fig. 3. J-V curves of the small area semitransparent devices without MoO_x (black curve) and with the introduction of MoO_x prior to ITO deposition (red curve) on small area size (0.1 cm²).

 TABLE I

 PERFORMANCE PARAMETERS OF THE PSMs FABRICATED

Demonstrate Mardada terra		EE(0/)	T (A)	MAD
Perovskite Module type	η (%)	FF (%)	I (MA)	V (V)
Au	15.94	71.13	113.41	23.92
MoOx-ITO 90w-180c	6.72	65.43	55.19	20.42
MoOx-ITO 60w-240c	8.23	64.64	65.87	21.27
Au(2 nm)-ITO 60w-240c	12.56	59.81	103.21	22.41

Module stack for all is the following: glass/FTO/SnO2/Perovskite/PEAI/Spiro-MeOTAD. Four different top electrodes were analyzed and characterized.

area and two different sputtering deposition procedures by varying the input power from 90 to 60 W and the number of cycles, from 180 to 240 cycles of deposition. One cycle represents the horizontal symmetric movement of the sample holder, backward and forward, under the rectangular ITO target. This is fundamental for the uniformity of the deposition. The choice of these optimization parameters comes from a previous optimization setup done in our group, where the combination of these values allows a uniform deposition, with a final thickness of 100 nm, ideal thickness necessary to have metal-like conductivity, and a suitable transparency [29], [30].

A reference module with Au as a standard opaque top electrode has been reported for comparison. The main results of the module performances are shown in Table I and Fig. 4.

The different stacks used for the PSMs, as shown in Fig. 4(b), are the following: glass/FTO/SnO₂/Perovskite/PEAI/Spiro-MeOTAD plus one of the final layers, as summarized in Table I. In the case of Au reference, no buffer layer was needed since thermal evaporation is a mild technique that prevents damaging of the layer underneath. All modules were performed with a design of 22 cells series connected: the voltage of the module is the sum of the voltage of all cells. Reference PSM with Au shows a PCE of 15.94%, fill factor (FF) of 71.13%, current (I) of 113.41 mA, and voltage (V) of 23.92 V.





Fig. 4. (a) *I–V* curves of the different buffer layers and top electrodes used. (b) Photograph of the four perovskite modules compared, showing the slot-die machine used to deposit ETL/Perovskite/HTL layers.

ST-PSMs show lower performances on the fill factor side, and this could happen because photons are not back reflected to recombine in the perovskite layer, as in the case of an opaque top electrode. PSM with MoOx-ITO 90w-180c (with ITO sputtering condition at 90 W and 180 cycles) shows 6.72% PCE, 65.43% FF, 55.19 mA *I*, and 20.42 V. PSM with MoO_x-ITO 60w-240c (with ITO sputtering condition at 60 W and 240 cycles) shows 8.23% PCE, 64.64% FF, 65.87 mA I, and 21.27 V. Finally, PSM with Au(2 nm) ITO 60w-240c (with ITO sputtering condition at 60 W and 240 cycles) shows 12.56% PCE, 59.81% FF, 103.21 mA I, and 22.41 V. It is interesting to analyze the voltage of the modules divided by the number of series-connected cells (22 in our module design). We get 1.087 V, 0.928 V, 0.966 V, and 1.018 V for the four Au, MoOx-ITO 90w-180c, MoOx-ITO 60w-240c, and Au(2 nm) ITO 60w-240c modules, respectively. The interface within Spiro-MeOTAD and Au (module type with top electrode Au and Au(2 nm) ITO 60w-240c) improves



Fig. 5. EL mapping of the different perovskite modules investigated: (a) with MoOx-ITO done at 90 W and 180 sputtering cycles; (b) with MoO_x-ITO done at 60 W and 240 sputtering cycles; (c) with Au as opaque reference; (d) with Au(2 nm) and ITO done at 60 W and 240 cycles; and (e) picture of the fabricated 15×15 cm2 module.

voltage and current of the PSM: this can be speculated by a series of factors, such as a better band alignment between this interface respect to Spiro-MeOTAD/MoO_x, less damaging deposition process while operating with thermal evaporated Au and lower shunt resistance caused by the presence of less points of nonradiative recombination [36].

Both ST-PSM with MoO_x buffer layer show similar I-Vcurves, but the J_{SC} is higher in the ST-PSM with lower sputtering power. This is an indication of the aggressive sputtering technique, damaging the overall device by reducing its final output current. The 60-W-based process required 240 cycles to reach 100 nm of ITO thickness, but, at the same time, limited the ion bombardment effect on the MoO_x that could reach the spiro-MeOTAD and the perovskite layer. Based on this result, we applied those parameters (60 W/240 cycles) also for the ST-PSM with the thin Au buffer layer. Furthermore, the abrupt measured reduction of current and voltage in the MoO_x-based devices as compared with the Au-based module could be ascribable to a reduction of oxygen vacancies upon air exposure during the P2 process. The transition metal oxides deposited via thermal evaporation are slightly substoichiometric [37]. However, oxygen exposure can cause a reduction of oxygen vacancies and defect trap states, which play a key role in charge transfer and in the final operating current. In addition, the work function and the hole-selective character of MoOx can also be affected, impacting the final device voltage [38], [39], [40]. The analyses of the deposition process on the ST-PSM were performed through EL mapping, as shown in Fig. 5. EL mapping is a powerful technique that provides a direct correlation between morphological and optical properties in a fast and nondestructive

way by visualizing the inhomogeneities at different intensities, depending on the applied voltage [41]. For EL mapping, we fixed the applied voltage to 22 V, corresponding to the average voltage generated by each module. The generated output current of the four PSMs was quite similar to the photogenerated current when exposing the ST-PSMs at 1 sun illumination. PSMs fabricated with thin and thick Au (2 nm + ITO and 100 nm, Fig. 5(d) and(c), respectively) show the best current output, with a measured peak over 50 mA, whereas PSMs fabricated with MoO_x buffer layer [see Fig. 5(a) and (b)] show an average current around 35 mA. From a qualitative point of view, devices fabricated with MoO_x show lower EL intensity, with some cells not showing any radiative behavior. For the Au-based PSMs, all cells show EL sign, with a relative intensity higher than PSM fabricated with MoO_x ; this behavior confirms the trend shown in the I-Vcurves. In Fig. 5(e), a photograph of the ST-PSM realized with Au(2 nm) ITO 60w-240c is shown. Overall, all modules show imperfections on some cells, and this is mainly related to the deposition uniformity of the different layers forming the PSM stack and interconnection failure. By a careful EL mapping inspection, the presence of dark spots in all types of modules is visible; this effect could be related to the presence of voids during one of the deposition steps since the absence of EL activity is given by a no signal, therefore a darker area in the map. We speculate that SnO₂ could be the responsible layer of this effect since is the thinner layer used in the stack and the possibility to get some discrepancy on the FTO layer is higher since also the roughness of the bottom TCO is ~ 15 nm [42] and this thickness waves can affect the uniformity of deposition. A possible follow-up of the work could be focused on planarizing



Fig. 6. Transmittance spectra from 200 to 1100 nm of the semitransparent device stack: $glass/FTO/SnO_2/$ Perovskite/PEAI/Spiro-MeOTAD/buffer layer/ITO with gold (green line) or MoOx (blue line) as buffer layer.

the bottom TCO or moving toward different TCOs (e.g., ITO) with a roughness range lower than the needed thickness for the ETL.

To evaluate the potential application as a top module in tandem configuration with silicon, the transmittance of the ST-modules was measured, as shown in Fig. 6, to quantify the losses in the near-infrared (NIR) region (780–1100 nm), the solar direct transmittance τ was evaluated and calculated as follows:

$$\tau = \frac{\int_{780\text{nm}}^{1100\text{nm}} T(\lambda) \text{ AM1.5G}(\lambda) d\lambda}{\int_{780\text{nm}}^{1100\text{nm}} \text{ AM1.5G}(\lambda) d\lambda}$$

where $T(\lambda)$ is the transmission spectrum and AM1.5G(λ) is the solar spectrum. In the case of Au and MoOx-based device, τ is 52.6% and 59.5%, respectively, proving that there is room for improvement to further enhance these values. The slight difference in the transmittance spectra in the 570–720 nm region can be due to a different perovskite thickness at the spectrophotometer lamp spots of the Au- and MoO_x-based samples. These results are taken from similar devices fabricated on a smaller area and a perovskite thickness variation might occur when changing substrate size and solution quantity to cast. In general, buffer layers work as protective layers preventing ETL/HTL modification due to sputtering ITO direct deposition, but at the same time, they are limited to transmission in the NIR region. A thin buffer layer is suitable to balance both effects.

To further improve the performance of ST-PSMs, we made use of an ARC: a thin layer of MgF_2 (100 nm) was deposited by thermal evaporation to improve the current of the final device and to reduce reflection from the incoming side of the light, that is, the glass in our study [42]. Light management is necessary on the glass side, and MgF₂ was used since it is a known ARC used in perovskite and, in general, in thin film solar technology [44], [45].

The ARC was deposited on the glass side of the Au(2 nm) ITO 60w-240c-based module to get more current on the best resulting



Fig. 7. (a) I-V curves of the different modules fabricated, with a photograph of the system used for the 4T measurement. (b) ISOS-L1 stress test under continuous light soaking, showing a remarkable T_{80} over 1459 h.

module device. The results showed an improvement in PCE, passing from 12.56% up to 13.18%, with the main improvement of the current, going from 103.2 up to 107.3 mA. There was a slight improvement of $V_{\rm oc}$ and FF, passing from 22.41 to 22.56 V and from 59.81% to 59.92%, mainly related to the measurement of the device with MgF₂ done after an aging time.

The optimized ST-PSM was tested in tandem configuration with an n-type CZ 1–5 Ω cm silicon wafer. In 4T configurations, we performed the testing of the c-Si cell filtered by PSM and measuring the single-junction PSM, with the final efficiency calculated by summing up both efficiencies obtained this way. The *I*–*V* curve is shown in Fig. 7(a), together with a photograph of the measurement setup used to couple both technologies. The c-Si cell shows a reduction of the current, passing from 36.56 mA at full AM1.5G spectrum to 13.89 mA when filtered by the perovskite module, and a consequent reduction of efficiency going from 20.96% to 7.73% (see Table II). It must be noted that the slight increase of the current of the Si filtered with the Au-based module as compared with the Si filtered with the MoO_x -based module might be due to the introduction of MgF₂ as ARC atop the ITO of the Au-based module. The addition of ARC reduced the reflection losses and might have induced an increased absorption in the perovskite, as well as in the silicon absorber [44], [47].

The sum of the efficiencies of the filtered c-Si and the PSM results in a PCE of 20.91%, which is similar to the single-junction not filtered c-Si efficiency. This result, even though is not marking a touchable improvement from a performance point of view, is important to report because perovskite can also act as a mechanical barrier protector from c-Si without losing its performance. Moreover, considering that this is a 4T configuration, it could be easy to substitute the top cell at its end of life or to increase the tandem efficiency if a new perovskite-based solution at a lower cost can be found for the top cell.

Clearly, this is true if the top and bottom cells are independent and not tightly laminated together. All these statements must be verified to determine whether tandem durability and economic values are favorable toward the exploitation of the dual-junction device.

Finally, after a sealing procedure applied to the module, ST-PSMs, composed of Au(2 nm) as a buffer layer, were tested using a standard ISOS-L1 test under continuous light soaking [42].

Results are shown in Fig. 7(b), with a photograph showing the condition of the PSM after 1000 h of aging under light soaking: the optimized PSM reaches T80, the time in which a device efficiency reaches 80% of its initial value, at 1459 h, and T90, that is the time in which the device efficiency reaches 90% of its initial value, at 712 h. These results show that this technology is improving also on the stability side, and the industrial-compatible techniques add relevance to these results.

IV. CONCLUSION

Industry-compatible ST-PSMs were fabricated with a dimension of 15.2×15.2 cm². The optimization was conducted by using slot-die coating, sputtering, and thermal evaporation processes. These techniques were used to commercialize many technologies (such as thin film PVs, batteries, printed electronics, fuel cells, and so on) and, therefore, are considered compatible at the industrial level. After a careful optimization of the buffer layer between HTL and ITO as TCO, and after the placement of an ARC, such as MgF₂, a PCE of 13.18% was reached. This module was tested in couple with industrially available C-Si cell of 6-in size, showing a total efficiency of 20.91%. The stability of the architecture was tested using ISOS-L1 protocol, proving the durability of the process retaining 80% of its initial performance after 1459 h. Perovskite technology is paving the way for tandem revolution by improving silicon technology only by placing perovskite as a filter and protecting silicon from potential mechanical damage.

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TABLE II PHOTOVOLTAIC PARAMETERS OF SILICON SOLAR CELLS STAND ALONE (SI), FILTERED WITH 2NM OF AU AND FILTERED WITH 7.5 nm OF MOOX

Silicon Cell type	η (%)	FF (%)	J (mAcm ⁻²)	V (V)
Si	20.96	79.7	36.56	0.719
Si filtered w/ Au(2nm)*	7.73	80.1	13.89	0.695
Si filtered w/ MoOx(7.5nm)	7.48	80.1	13.45	0.694

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