# Guest Editorial Memristive Circuits and Systems for Edge-Computing Applications

THIS Special Issue of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) is devoted to showcase the latest research achievements on memristive circuits and systems with special focus on edge-computing applications.

Over the past few years, the field of circuits and systems has witnessed significant changes, which have inevitably accompanied the progressive approach of the CMOS technology aggressive downscaling trend to an unavoidable end, given the clear impossibility to reduce the transistor dimensions below the atomic scale, in the near future. Tremendous efforts are being made in search for novel devices and circuits toward the development of disruptive nanotechnologies, enabling the fabrication of multi-purpose devices and circuits, which would allow to foster sustainable progress in integrated circuit design, despite further shrinking in transistor sizes shall no longer be feasible soon. In this regard, memristors, exhibiting the extraordinary capability to combine, within a single miniaturized 3-D space, data sensing, processing, and storage functionalities, offer a plethora of novel opportunities for integrated circuit design, paving the way toward the conception of multi-purpose CMOS-compatible nano-circuits, which are bound to improve the performance of state-of-the-art computing machines.

With reference to the current trends in memristor research, extensive studies on various scientific fields complement the material engineering investigations. Experimentalists deploy enormous resources to enhance the fabrication process of novel memristive nanodevices and work together with experts in physics, and in circuit and system theory toward the formulation of reliable mathematical models for the accurate reproduction of electrical characterization data. In parallel to these activities, given that techniques, enabling the analysis and synthesis of linear circuits and systems, are no longer applicable to models of intrinsically-nonlinear memristor devices and their circuits, theoretically inclined researchers work relentlessly toward the introduction of novel circuit- and system-theoretic tools to enable a comprehensive understanding of the mechanisms, underlying the dynamics of memristors, and to allow the development of a systematic approach to memristive circuit design. Meanwhile, system-level engineers contribute to the progress of this multi-disciplinary research field by devising innovative signal processing paradigms, which leverage the versatility of memristors, to solve standing issues with conventional data computing strategies, including the von-Neumann bottleneck, and to allow a biologically plausible reproduction of neuronal and synaptic activity in the human brain, to name but a couple of examples.

This Special Issue presents the latest developments in the multi-disciplinary field of memristive circuits and systems, with particular emphasis on the most recent advancements in edge-computing applications. Exploiting the versatile and rich dynamics of resistance switching memories, circuits, and networks, based on them, are expected to boost the area, time, and energy efficiency of the data management flow, as compared to what is currently possible in standard electronic systems, as already demonstrated in various works from the literature, and further revealed in works reported in this issue. The high-quality scientific contributions, authored from outstanding experimenters and theoreticians, and published in the issue, serve several purposes to the benefit of the memristive circuits and systems community, sharing knowledge, identifying open issues, and inspiring future research directions across a wide number of distinct fields, encompassing nonlinear circuit and system theory, circuit design, signal processing, computer architecture, and neuromorphic engineering.

Out of a rigorous peer-review process, only 24 articles were finally accepted for publication. These manuscripts may be categorized into four different main areas: 1) theory and modeling of memristor devices, circuits, and systems; 2) computing-in-memory memristive circuits and accelerators; and 3) memristive neuromorphic networks for edge computing and engineering applications.

## I. THEORY AND MODELING OF MEMRISTOR DEVICES, CIRCUITS, AND SYSTEMS

Since the theoretical postulation of the existence of the memristor, tracing back to Chua's 1971 seminal paper, several works have contributed to develop solid foundations for its theory as well as to explore its potential for the electronics of the future. In this session the following articles are focusing on advancing the theory of memristor devices, cells, and networks.

In [A1], Wang et al. review the state of the art of multi-state memristors, especially with different bi-layer oxide combinations and their associated CMOS/memristor circuit

Digital Object Identifier 10.1109/JETCAS.2022.3226900

design, and, moreover, discuss the challenges regarding device imperfection factors, modeling, and peripheral circuit design and layout. The difficulties and the challenges that lie in the memristive circuits and systems design, and the multi-state memristors-related applications in their most prominent aspects are also meticulously discussed.

In [A2], Innocenti et al. investigate how the multistability feature of circuits with an ideal memristor can be exploited to reproduce all the dynamics displayed by a forced nonlinear system. More specifically, if the forcing input is constant, like in FitzHugh–Nagumo model, then an input-less memristor circuit whose manifold index is related to the value of the input is considered. If the input is non-constant, like in Duffing system, then some independent voltage/current sources are introduced in the circuit and programmed according to the index variations.

In [A3], Tanaka et al. introduce the theoretical concept but also the circuit elements for a Gyrator Neuron (GN) constructed by memristive elements that has analog basic neuron operations of "CellularFlow (CF)" and executes learning by backpropagation processing and association by forward propagation processing as also proposed in the corresponding presented circuit simulator.

In [A4], Nabil et al. present a thorough analysis on the tentative differences between the Mott memristors and that of the HH voltage-gated ion channels and how these differences should be taken into account during the design process of the corresponding circuits to present biological plausible results.

In [A5], Ananda et al. proposed an optimized meminductor emulator designed by employing only MOS transistors making it realizable using monolithic IC fabrication and suitable for high-frequency operations and for a wide range of applications as verified by the design of a corresponding chaotic oscillator.

In [A6], Biolek et al. show how a generic meminductor can be synthesized using a multiport inductor and elements from Chua's table. In particular, the proposed model of the generic meminductor has a nonlinear core consisting of an inductive multiport and its ability to predict the hysteretic behavior is verified on the example of an elastic meminductive system.

In [A7], Ananda et al. proposed an optimized MOS-based memcapacitor emulator by employing active elements and a resistor, making it also suitable for monolithic IC fabrication with small area utilization, power consumption, and the ability to operate at a higher frequency when compared with the state-of-the-art emulators available in the literature.

In [A8], Ascoli et al. present a simple Reaction-Diffusion Cellular Neural Network (RD-CNN), composed of two identical resistively coupled Chua's circuits, and supporting counterintuitive dissipation-induced symmetry-breaking phenomena, accompanied by the emergence of steady-state dynamic pattern formation, including high-order chaotic solutions. A comprehensive systematic analysis, based upon the quantitative theory of local activity, enables to identify all the possible design parameter regions, within which the uncoupled cell is poised on the edge of chaos, which is crucially necessary for the array homogeneous solution to lose stability, later on, as the cells are let interact via a diffusion process. Remarkably, this manuscript further presents a rigorous mathematical analysis, which allows to derive, rigorously, the set of conditions, involving the resistance, which couple the two Chua circuits, under which the RD-CNN supports the paradoxical nonlinear phenomenon, widely known as Prigogine's Instability of the Homogeneous.

## II. Computing-in-Memory Memristive Circuits and Accelerators

A group of significant scientific contributions, gathered in this issue, advance significantly the state-of-the-art in Computing-In-Memory (CIM) circuits and accelerators, paving the way toward future applications, but also proposing interesting ideas for enhancing the memristor-centered mem-computing paradigm.

In [A9], Liu et al. introduce a mixed-bit ReRAM-based CIM accelerator to improve energy-efficient performance for Neural Architecture Search (NAS)-optimized Convolutional Neural Networks inference on edge. Furthermore, a column parallel readout with low-power cycle reduced ADC was introduced resulting in peak energy efficiency of 2490.32 TOPS/W and average energy efficiency of 479.37 TOPS/W with evaluating NAS-optimized multi-bitwidth Convolutional Neural Networks showing 14.18× improvement when compared with existing approaches.

In [A10], Li et al. proposed an effective design methodology to select the suitable multiply-and-accumulate (MAC)-error-correcting code (ECC) scheme depending on the target workload, desirable accuracy, and error level in the utilized resistive random-access memory (RRAM)-based CIM hardware in a TSMC 40 nm process and achieving a macro-level peak performance of 42.7 TOPS/W energy efficiency and 97.8 GOPS/mm$^2$ computing efficiency at 25°C and with only 2% accuracy degradation for investigated workloads up to 120°C with low-performance overhead.

In [A11], Zhou et al. propose a 81-Kb ReRAM CIM-based accelerator, which was designed using a 28-nm process with 1–4 b input/weight/output, and show-cased a processing frequency as high as 167–500 MHz, an energy efficiency of 95.3–59 TOPS/W, while operating on the CIFAR 10 data set under 1–4 b precision, and a Figure-of-Merit (FoM), defined as input-precision × weight-precision × energy efficiency, which is 3.6× higher than prior works.

In [A12], Meng et al. show that by utilizing the inherent computational granularity in CIM operations, fine-grained structured pruning can be supported with improved accuracy and minimal hardware cost; in particular, with the proposed method, a compression ratio up to 11.1 (i.e., 9% weights remaining) was achieved with only 0.6% accuracy drop and with minimal hardware overhead in the corresponding hardware design.

In [A13], Amid et al. establish a design approach, called Xbar-Partitioning, for the division of large CIM arrays into multiple sub-structures to alleviate the impacts of noise and parasitics, while keeping the computation in the analog domain. Six different bitcell layouts, five distinct memristive device technologies, and four alternative partitioning schemes for MNIST classification were investigated, proving that

bitcells of reduced size, a large number of partitions, and a high $R_{off}/R_{on}$ ratio for the memristive device enrich the noise tolerance of the fully analog IMC circuits, which enables them to feature a higher computation accuracy under a given low power budget, even in the presence of the interconnections' parasitics.

In [A14], Dias et al. introduce an auxiliary circuit able to perform conditional execution of memristive stateful logic operations by detecting any non-effective steps and discarding their execution, while its robustness has been demonstrated through several electrical simulations analyzed through the implementation of 276 functions of several benchmarks, resulting to drastically reduction of the execution time needed for this type of computing.

## III. Memristive Neuromorphic Networks for Edge Computing and Engineering Applications

This group of articles focuses on memristive neuromorphic circuits and systems, including chips, implemented by integrating resistance switching memories on top of CMOS hardware, which outperform in several figures of merit state-of-the-art bio-inspired computing platforms. Moreover, significant achievements toward a robust design of memristive circuits and networks, tuned for different engineering applications, including the implementation of deep learning algorithms, are thoroughly presented, which is expected to boost further the research on these scientific topics in the time to come.

In [A15], Zhou et al. demonstrate competitive performance on real-world datasets that go beyond static pattern recognition and handwritten digit using a fully memristive spiking neural network (MSNN) that includes both memristive synapses and memristive neurons. In particular, the paper has first mapped low-level, analog SPICE dynamics directly into an acyclic computational graph that is compatible with the backpropagation algorithm and by harnessing a blend of the intrinsic behaviors of memristors and the sparse network activity of SNNs, the power consumption and latency of the proposed approach surpasses that of all other similar methods in terms of accuracy.

In [A16], Camunas-Mesa et al. introduce a fully monolithic CMOL-like Memristor-CMOS chip realization of a neuromorphic event-driven spiking neural network. More specifically, it presents a CMOL computing core, implementing a Spiking Neural Network (SNN) with 64 input neurons, 64 output neurons, and 4096 1T1R synapses, each of which consists of a 200-nm-sized Ti/HfOx/TiN memristor integrated on top of a transistor fabricated in 130-nm CMOS technology. The computing functionalities of this neuromorphic chip have been exhaustively explored in the lab, which allowed to record successful experimental tests on template matching, and regularized stochastic binary Spike-Timing-Dependent-Plasticity (STDP).

In [A17], Wang et al. introduce a novel pipelined memristive Analog-to-Digital Converter (ADC) architecture supporting in-situ training and random weight change (RWC) learning algorithm modified to reduce the complexity of error feedback circuit. The results of integral non-linearities (INL), differential nonlinearities (DNL), signal-to-noise and distortion ratio (SNDR), and effective number of bits (ENOB) ensure that compared with other designs, the adaptive ability of the proposed mADC is substantially enhanced, and the influence of fluctuation factors such as ambient temperature and noise can be avoided.

In [A18], Oli-Uz-Zaman et al. propose an adaptive mapping method (AMM) to mitigate the stuck-at-fault (SAF) defects of memristor generated from immature fabrication and heavy device utilization for in-memory deep neural networks (DNNs) computation that when applied restores the inference accuracy up to 90% under different SAFs schemes and, moreover, improves the accuracy more than 50% in presence of high nonlinearity while the standard conductance drift does not influence the inference accuracy for CIFAR 10.

In [A19], Cao et al. propose a modeling and simulation framework for edge-AI deep neural networks (DNNs) through the utilization of memristive crossbar arrays and the introduction of a non-ideality-aware training to achieve fast and accurate early exploration of the system design and, furthermore, reduce the degradation of inference accuracy. A simplified 5-layer VGG network implemented in software on a measured $128 \times 128$ RRAM array with 3-level weight resolution succeed 83% inference accuracy with less than 3% accuracy drop when compared to ideal model for CIFAR test bed.

In [A20], Radhakrishnan et al. propose a five-memristor bridge super-resolution node and its use in a memristor crossbar array where to perform the accurate weight-summation operations required for analog neural computations. Compared with the parallel super-resolution node, the bridge nodes preserve tolerance to memristor variability and at the same time with lower area and power requirements while they present near-idealistic inference accuracy when applied to artificial and convolutional neural networks.

In [A21], Mannocci et al. proposed a novel closed-loop in-memory computing-based ridge regression circuit, capable of accelerating all typical operations of a massive multiple-input multiple-output (MIMO) transaction, including channel estimation, and uplink and downlink transmissions. The presented simulation results indicate a 4 orders-of-magnitude increase in energy efficiency and a 3 orders-of-magnitude increase in area efficiency for the same throughput of a digital solution, supporting IMC for energy-efficient pre- and post-processing in next-generation B5G and 6G networks.

In [A22], Kaur et al. proposed a Muller C-element utilizing a Programmable Metallization Cell (PMC) and a CMOS inverter and performs Bayesian inference with reasonable accuracy. The presented element implementation has been benchmarked utilizing PMC against the conventional inference circuits and prior CMOS and spintronics-based Muller C-elements also presenting the impact of spatial and temporal variations of PMC on its performance ensuring that it can potentially offer a lucrative alternative for compact, ultra-low-power Bayesian inference circuits.

## ACKNOWLEDGMENT

First of all, we unanimously wish to extend their gratitude to all the authors, who committed time and efforts to prepare scientific contributions of technical excellence. Thanks to their outstanding research works, this Special Issue is bound to attract much attention within the Memristor Circuit and System community. We are also grateful to each of the anonymous reviewers for providing valuable comments and suggestions on the submissions. We further thank the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) Editor-in-Chief (EiC), Prof. Herbert Iu, the JETCAS Associate Editor, Prof. Carl Ho, as well as the Senior Editorial Board for their continuous guidance, support, and advice. By providing a wide overview of the latest trends and developments in the ever-growing and multidisciplinary memristor circuit and system research field, this Special Issue is expected to inspire senior and early-stage researchers in the field, and even spark interest in the uninitiated scholars.

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## APPENDIX: RELATED ARTICLES

[A1] C. Wang et al., "Multi-state memristors and their applications: An overview," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 723–734, Dec. 2022.

[A2] G. Innocenti, A. Tesi, M. Di Marco, and M. Forti, "Embedding the dynamics of forced nonlinear systems in multistable memristor circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 735–749, Dec. 2022.

[A3] M. Tanaka, Y. Nishio, H. Sekiya, M. Bandai, Y. Tanji, and Y. Uwate, "CellularFlow: Memristive circuits of gyrator neurons toward brain circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 963–977, Dec. 2022.

[A4] A. Nabil, T. N. Kumar, and H. A. F. Almurib, "Mott memristors and neuronal ion channels: A qualitative analysis," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 762–773, Dec. 2022.

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[A11] K. Zhou et al., "A 28 nm 81 Kb 59-95.3 TOPS/W 4T2R ReRAM computing-in-memory accelerator with voltage-to-time-to-digital based output," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 846–857, Dec. 2022.

[A12] Meng, "Exploring compute-in-memory architecture granularity for structured pruning of neural networks,"

[A13] M. H. Amin, M. E. Elbtity, and R. Zand, "Xbar-partitioning: A practical way for parasitics and noise tolerance in analog IMC circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 867–877, Dec. 2022.

[A14] C. S. Dias, F. S. Marranghello, R. M. Brum, and P. F. Butzen, "A predictive approach for conditional execution of memristive material implication stateful logic operations," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 878–887, Dec. 2022.

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[A19] T. Cao et al., "A non-idealities aware software-hardware co-design framework for edge-AI deep neural network implemented on memristive crossbar," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 4, pp. 934–943, Dec. 2022.

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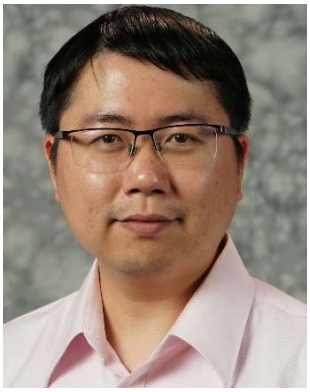

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