Introduction to the Special Issue on the 1st IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2019)

THIS issue of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) includes some of the highlights of the best articles from the 1st IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2019), which was held at the Ambassador Hotel Hsinchu, Taiwan, on March 18–20, 2019. Artificial Intelligence (AI) is driving the new revolution of not only information technology but also all other industries. New algorithms and application systems are introduced with the power of AI. New computing platforms are required to support the emerging AI algorithms and applications, from cloud servers to edge devices, from system level to circuit level. Facing this new challenge and opportunity, the first AICAS was launched and fully sponsored by IEEE Circuits and Systems Society (CASS). It is established to facilitate the state-of-the-art research, innovation, and development activities at the frontiers of AI circuits and systems. It is an ideal forum for allowing academia and industry from international communities to exchange experiences, demonstrate their results and further advance AI technologies on circuits and systems.

Thirteen articles were selected for publication in this Special Issue of JETCAS. These manuscripts provide in-depth materials beyond the articles published in the AICAS 2019 proceedings. A wide range of topics are covered. Two articles are in hardware accelerators for AI: "CNNP-v2: A memory-centric architecture for low-power CNN processor on domain-specific mobile devices" and "Hardware design of a context-preserving filter-reorganized CNN for super-resolution." Three articles are in medical AI: "Hematoxylin and eosin (H&E) stained liver portal area segmentation using multi-scale receptive field convolutional neural network", "An unobtrusive system for heart rate monitoring based on ballistocardiogram using Hilbert transform and Viterbi decoding", and "A EEG-based real-time emotion recognition system using convolutional neural network chip." Three articles are about neuromorphic processors: "Dropout and DropConnect for reliable neuromorphic inference under communication constraints in network connectivity", "Asynchronous spiking neurons, the natural key to exploit temporal sparsity", and "Neural state machines for robust learning and control of neuromorphic agents." Three articles are in deep learning algorithm/architecture: "Incremental learning of hand symbols using event-based cameras", "Review and benchmarking of precision-scalable multiply-accumulate unit architectures for embedded neural-network processing" and "MADS: A framework for design and implementation of adaptive digital predistortion systems." Two articles are in low precision neural networks: "EBPC: Extended bit-plane compression for deep neural network inference and training accelerators" and "Memory-reduced network stacking for edge-level CNN architecture with structured weight pruning."

The Guest Editors would like to express our sincere appreciation to all the authors and anonymous reviewers for putting in their effort and time to ensure high-quality manuscripts under a very tight schedule. We would also like to thank all members of the Technical Program Committee, Steering Committee, and Organizing Committee of the 1st AICAS for making the conference a success. In addition, we would like to thank Eduard Alarcón, JETCAS Editor-in-Chief, and An-Yeu (Andy) Wu, JETCAS Deputy Editor-in-Chief, for their guidance, Desiree Noel, and the JETCAS administration for their invaluable assistance in publishing this Special Issue. We hope that the articles presented in this Special Issue provide a valuable technical feast to journal readers. Finally, we encourage readers to attend the AICAS 2020, to be held at Porto Antico, Genova, Italy, on March 23–25, 2020. For more information, please visit http://www.aicas2020.eu/. We look forward to seeing you in Genova, a beautiful, historical, and fun city in Italy.

Robert Chen-Hao Chang, *Lead Guest Editor*
National Chung Hsing University
Taichung 40227, Taiwan
e-mail: chchang@nchu.edu.tw

Gwo Giun (Chris) Lee, *Guest Editor*
National Cheng Kung University
Tainan 70101, Taiwan
e-mail: clee@mail.ncku.edu.tw

Tobi Delbruck, *Guest Editor*
University of Zurich and ETH Zurich
8057 Zürich, Switzerland
e-mail: tobi@ini.uzh.ch

Maurizio Valle, *Guest Editor*
University of Genoa
16145 Genoa, Italy
e-mail: maurizio.valle@unige.it

Digital Object Identifier 10.1109/JETCAS.2019.2954760

Robert Chen-Hao Chang (S'91–M'95–SM'09) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from the University of Southern California (USC), Los Angeles, in 1995.

In 1996, he joined the Faculty of National Chung Hsing University (NCHU), Taichung, Taiwan. He served as the Director of the Center for R&D of Engineering Technology, College of Engineering from 2005 to 2006; the Chairman of the EE Department from 2006 to 2008; the Deputy Director General of the National Chip Implementation Center, Hsinchu, Taiwan, from March 2011 to January 2014; and the Dean of College of Science of Technology, National Chi Nan University, Nantou, Taiwan, from 2014 to 2017. In 2018, he became the Program Director of Semiconductor Manufacturing and Design for AI Edge Project, Ministry of Science and Technology, Taiwan. His research interests include SoC and signal processing systems and mixed-signal IC design.

Dr. Chang was a recipient of the Distinguished Teaching Award from NCHU in 2004. He was a Distinguished Lecturer of the IEEE CAS Society in 2013 and 2014. He served as an Associate Editor for the IEEE TVLSI from 2010 to 2014; the IEEE CASS Taipei Chapter Chair from 2011 to 2012; the IEEE CASS NG TC Chair from 2015 to 2017; the IEEE Systems Council CASS Primary Representative from 2016 to 2019; the General Co-Chair of AICAS 2019. He served as a Guest Editor for the IEEE JSSC in 2019. He is currently the IEEE A-SSCC TPC Chair.

Gwo Giun (Chris) Lee (S'91–M'97–SM'07) received the B.S. degree in electrical engineering from National Taiwan University, and the M.S. and Ph.D. degrees in electrical engineering from the University of Massachusetts.

He worked for Philips Semiconductor as a System Architect and a Project Leader in the Silicon Valley. He was recruited to National Cheng Kung University in 2003, where he founded and currently leads the Bioinfotronics Research Center. He is currently an Investigator of the signal processing systems field, including multimedia and bioinformatics. His system design work, based on analytics of algorithm concurrently with architecture, titled "Algorithm/Architecture Co-Design (AAC)," has made computations on system-on-chip, edge, and cloud platforms possible in resolving complex problems accurately and efficiently. His works have contributed more than 130 original research and technical publications with the invention of more than 50 patents worldwide. His AAC work was used by the industry in deploying more than 50 million LCD panels worldwide. Two of these patents were also licensed by the U.S. health industry for the development of analytics platform-based precision medicine products (Boston, MA, USA, June 2015, GLOBE NEWSWIRE). His AAC work has been pivotal in delivering feasible and realistic international standards, including 3-D extension of HEVC and Reconfigurable Video Coding in ISO/IEC/MPEG, for applications requiring the processing of big multimedia data. His low-complexity 3-D video coding technology was also included in MPEG.

Dr. Lee has been the IEEE CASS Distinguished Lecturer since 2019. He has also been an ExCom Member for the IEEE Region ten since 2017. He has also been chairing the Industry Relations Committee since 2019. He serves as an Associate Editor for the IEEE TSP and the *Journal of Signal Processing Systems*. He was formerly an Associate Editor for the IEEE TCSVT for which he received the Best Associate Editor's Award in 2011.

Tobi Delbruck (M'99–SM'06–F'13) received the B.Sc. degree in physics from the University of California, in 1986 and the Ph.D. degree from Caltech, in 1993. He is currently a Professor of physics and electrical engineering with the Institute of Neuroinformatics, University of Zurich and ETH Zurich, where he has been since 1998. The Sensors Group that he co-directs together with Prof. S.-C. Liu focuses on efficient neuromorphic sensory processing and deep neural network theory and hardware accelerators.

Maurizio Valle (SM'16) received the M.S. degree in electronic engineering and the Ph.D. degree in electronics and computer science from the University of Genova, Italy, in 1985 and 1990, respectively.

From 1992 to 2006, he was an Assistant Professor and since January 2007, he has been an Associate Professor of electronic engineering with the Department of Electrical, Electronic and Telecommunications Engineering and Naval Architecture, University of Genova, where he was a Full Professor, in December 2019. He is currently the Head of Connected Objects, Smart Materials, Integrated Circuits—COSMIC Laboratory. He is a co-author of more than 200 articles published in peer-reviewed international scientific journals and conference proceedings. His research interests include bio-medical circuits and systems, electronic/artificial sensitive skin, embedded electronic systems for tactile sensors, tactile sensing systems for prosthetics and robotics, neuromorphic touch sensors, and wireless sensor networks.

Prof. Valle has been and is currently in charge of many research contracts and projects funded at local, national, and European levels and by Italian and foreign companies. He is a member of the IEEE CAS Society.