A Circuits and Systems Perspective of Organic/Printed Electronics: Review, Challenges, and Contemporary and Emerging Design Approaches

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***Abstract*— The often touted attractive attributes of printed/organic electronics are its mechanically flexible form-factor, low-cost, green, on-demand printing, scalability, low-power operation, and intelligence (signal processing) – ideally, the creation of intelligent lightweight electronics printed by simple ubiquitous printing processes, and integrated into new ways to exploit its mechanically flexible form-factor. Printed/Organic Electronics, now an industry on its own right and recognized as one of the key technological enablers for the Internet of Things, is largely complementary to silicon because the printed transistors are slow and the printed elements are large. The sanguine projected growth of the $29 B market today to $73 B by 2027 assumes that 'intelligence' (analog, mixed-signal and digital signal processing) would be realizable. Nevertheless, many of the said attributes of printed/organic electronics remain a challenge. In this paper, we exemplify this with a comprehensive and critical review and tabulation of the state-of-the art printed digital, analog, and mixed-signal circuits. We further review the application space of printed/organic electronics and the supply chain, including their classifications and delineate the associated challenges in each constituent chain. These challenges, largely unresolved, are indeed formidable, and are discussed with a critical circuits and systems perspective. Our review depicts that contemporary design philosophies and methodologies for silicon are largely inadequate for printed/organic electronics. To this end, we discuss esoteric analog and digital design philosophies and methodologies, with emphasis on co-design and co-optimization between the different constituent supply chains that may potentially circumvent the said formidable challenges, and discuss the associated penalties thereto.**

***Index Terms*— Printed electronics, organic electronics, large area electronics, flexible hybrid electronics.**

I. Introduction

PRINTED/Organic Electronics is now an industry on its own right –the iNEMI (International Electronics Manufacturing Initiative) [1] classifies Printed/Organic Electronics ('Large Area, Flexible Electronics') as one of fourteen technologies under the broad 'Component/Subsystem Technologies' category within the electronics industry. The market size of Printed/Organic Electronics is gargantuan and projected to grow aggressively – these projections, in part, depend on how the various establishments ascertain what constitutes as organic/printed electronics. IDTechEx [2] projects that the market for Printed/Organic Electronics will grow from US$29B in 2017 to US$73B in 2027 while the Organic Electronics Association (OE-A) [3] projects the >US$24B market today to ∼US$200B within a decade.

There is intense and concerted international and local-region effort on Printed/Organic Electronics and related technology, including effort by over 3,000 organizations globally comprising academic institutions, industry, and consortia. These include government and industry-led efforts, including iNEMI [1]; the European-based OE-A [3], an industry-based association with over 230 global company-members; the USA-based Nextflex [4], USA's flexible hybrid electronics manufacturing institute; USA-based FlexTech Alliance [5]; the Canadian Printable Electronics Industry Association [6]; etc. The IEEE is also fully cognizant of the imperativeness of organic/printed electronics, where several societies, including the Circuits and Systems Society and the Electron Device Society, established their special technical committees in 2016. This review paper is part of the effort organized by the new Flexible Hybrid and Printed Electronics Technical Committee of the IEEE Circuits and Systems Society.

Printed/Organic Electronics is increasingly recognized as a key enabler for the Internet of Things (IoTs) as part of the 'Fourth Industrial Revolution' whose key technology advances are functionality and low-cost. Printed/Organic Electronics offers unique mechanical flexibility functionality and low-cost – often touted as the creation of intelligent lightweight electronics based on cheap abundant materials and printed by simple ubiquitous printing processes, and integrated into new ways to exploit its mechanically flexible form-factor. Its desirable attributes include:

- Low Cost – cost in terms of cents, potentially single-use and hence disposable
- On-demand printing – print quickly (where production time goes from months/weeks to minutes), print anywhere (simple printing equipment and infrastructure) and

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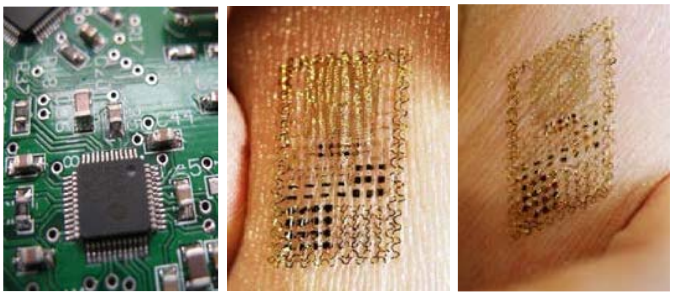
print anytime). Further, in view of low cost, all printing steps would ideally additive-only (i.e., no subtractive steps such as etching, lift-off, etc.), processed in an all-air environment (without pressure or specialty gases), low-temperature (allowing cheap substrates), and digital (no masks required); see later
- Green or 'Sustainable' –use of environmentally-friendly, earth abundant, and non-corrosive elements/chemicals, efficient use and low chemical waste, and if possible, recyclable
- Scalable – large-format printing, e.g., wallpaper and e-skin
- 'Intelligent' – the electronics embodies analog, digital and mixed-signal processing with reasonable sophistication
- Power-Efficient – low-power operation (including operable with intermittent and noisy power supplies) congruous with green/sustainability, modest energy requirements and possibly fully-energy harvested and battery less
- Robust – reliable and able to withstand the weather
- Thin and lightweight
- Mechanical Flexibility – the thin substrate is mechanically flexible such that they can be molded or bent to fit in odd and uneven spaces, adhered to curvilinear surfaces, conformable, stretchable, bendable, rollable, etc.

Put simply, it ideally resembles a low-cost, green, print anywhere, on-demand, and scalable graphics-based 'printing press' to print electronics on mechanically flexible substrates.

The advantages offered from mechanical flexibility were recognized very early in the evolution of electronics. One of the earliest exampleswas in the 1960s for a telephone [7] where by embodying flexible circuitry instead of rigid circuitry, 25% additional room was gained to contain more functionality within the same enclosure. Also in the same era, thin (<200μm) solar cell arrays were employed for aerospace and satellites [8]. The mechanical flexibility offered a convenient yet reliable means for compact stowage during launch and thereafter opened for deployment. It can be argued that Printed/Organic Electronics 'came of age' in the 1970s when the first conducting polymers were realized by Nobel Laureates Alan Heeger, Alan MacDiarmid, and Hideki Shirakawa – "plastic can, after certain modifications, be made electrically conductive" [9]. It was however over a decade later when Printed Electronics, particularly in the form of thin film transistors (TFTs) printed on a flexible substrate, was practically realized.

Fast forward to the present, Fig. 1 depicts the salient difference between conventional electronics and the possibilities offered by Printed/Organic Electronics. Conventional electronics are largely silicon-CMOS circuits realized in rigid ICs encapsulated in rigid epoxy packages and assembled with other rigid passive components on a rigid printed circuit board. Conversely, Printed/Organic Electronicsis mechanically flexiblewhere in Fig. 1(b) [10], it is bendable, conformable and stretchable; at the very least, bendable. This mechanical flexibility offers unique applications – but not without its formidable challenges; see later.

It is easy to appreciate that Printed/Organic Electronics technology is highly multi-disciplinary. Not surprisingly, there are



(a) (b) (c)

Fig. 1. (a) Conventional silicon-based electronics embodying a rigid CMOS IC encapsulated in rigid epoxy packages placed on a rigid Printed Circuit Board; (b) A Printed Electronics system (patch) placed on unstretched skin, and (c) when the stretched [10].

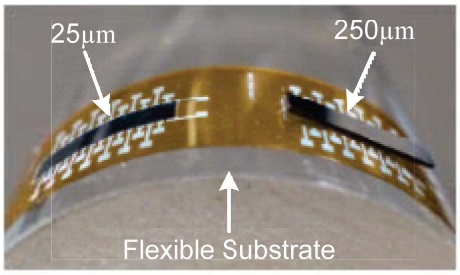


Fig. 2. An inflexible 250μm thick silicon die (right; delaminated from the bent flexible substrate) becomes flexiblewhen thinned (25μm (left; undelaminated)) [11].

a number of synonyms to 'Printed' and 'Organic' Electronics where – 'organic' is a misnomer because many materials are inorganic. The other synonyms include 'Plastic Electronics', 'Polymer Electronics', 'Large Area Electronics', 'Thin Film Electronics', 'Flexible Electronics' 'Flexible Polymer'; and a permutation of synonyms such as 'Organic Large Area Electronics', 'Flexible Organic Large Area Electronics', etc. The early USA DARPA program classified this as 'Large Area Electronics' while iNEMI classifies it as 'Large Area, Flexible Electronics'. The OE-A qualifies Organic Electronics as that "… based on the combination of a new class of materials and large-area, high-volume deposition and patterning techniques", and continues to use 'Organic' – 'organic' is not taken literally but used in the broader sense. In this review, 'Printed Electronics' and 'Organic Electronics' will be used interchangeably.

The congruity amongst all these synonyms is that the electronic elements are printed/patterned on a *flexible* substrate vis-à-vis silicon fabrication (not 'printed') on *rigid* substrates (wafers); nevertheless, a rigid substrate when thinned sufficiently (typically <50μm) does become mechanically flexible as depicted in Fig. 2 [11]. These printed elements include the entire space of electronic elements, ranging from active devices (TFTs, Organic Electrochemical Transistors, etc.), passive components (resistors, capacitors, inductors, antennas, interconnects, etc.), to power-related devices (batteries, photovoltaics (solar panel), supercapacitors, etc.)

For completeness, Flexible Hybrid Electronics is 'hybrid' technology embodying heterogeneous integration of Printed Electronics and conventional silicon-based electronics

TABLE I
PRINTED ELECTRONICS INVERTERS

Reference	Year	I_{on}/I_{off}	Delay (ms)	NM_H/NM_L (V)	Gain	V_M (V)	Supply voltage (V)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Chang, et al. [14]	2014	*p*: 10^5	5	1.5/15	2	38	60	PET	Screen printing	120	No
Ramon *et al.* [15]	2016	*p*: 10^2	-	-	2.3	-	30	PEN	Inkjet printing	-	N_2
Fukuda *et al.* [16]	2014	*p*: $10^{3.5}$*	1.12	-	1.6	6	10	Parylene-C	Spin coating, inkjet printing	150	-
Kang *et al.* [17]	2014	*p*: 10^3-10^5	2.75×10^{-3}	-	9	5.5*	15	PEN	Gravure printing, inkjet printing	140	Ozone, RF plasma (e.g., H_2/N_2)
Seungjun *et al.* [18]	2011	*p*: $10^{2.5}$*	-	-	7.8	10*	50	Polyarylate	Inkjet printing	200	-
Linrun *et al.* [19]	2014	*p*: $10^{2.5}$*	-	-	67.3	2.5*	3	PEN	Spin coating, inkjet printing	150	N_2
Kim *et al.* [20]	2012	*p*: 10^3 *n*: 10^4	-	-	60	13	20	PI	Evaporation, spin coating, CVD	200	-
Klauk *et al.* [21]	2007	*p*: $10^{3.5}$* *n*: 10^3*	-	-	100	1.5*	3	Glass or PEN	Evaporation	90	O_2 plasma
Graz *et al.* [22]	2010	*p*: $10^{4.5}$* *n*: $10^{4.5}$*	-	-	20	35*	60	PDMS	Evaporation	100	N_2
Taylor *et al.* [23]	2014	-	0.16	4.7/4.4	1.8	18*	40	PEN	Evaporation	-	Ar plasma, N_2, vacuum
Guerin *et al.* [24]	2011	*n*: $10^{5.9}$ *p*: $10^{5.3}$	0.43	17/15	29	20	40	PEN	Laser ablation, screen printing	100	No
Cao *et al.* [25]	2008	*p*: $10^{3.5}$*	-	-	2	1.5*	5	PI	Photolithography, CVD	-	-
Honda *et al.* [26]	2015	*p*: 10^2 *n*: 10^2	0.75	-	45	2*	5	PI	Sputtering, etching	-	-
Fluxrnan *et al.* [27] +	1994	*p*: 10^6 *n*: 10^6	-	-	2.5	14*	16	Glass	poly-Si TFT technology	600	-

Additive processes | Subtractive processes

* Our estimation based on reported data

NM_H: Noise Margin High; NM_L: Noise Margin Low: V_M: Switching threshold voltage; +a-Si or poly-Si

(typically thinned-down CMOS IC dies, e.g. left of Fig. 2) – the specific technology chosen is that which makes most sense – also realized on a *flexible* substrate. A comprehensive review may be found in the April 2015 issue of the IEEE Proceedings [7]. In terms of signal processing, Flexible Hybrid Electronics is substantially advantageous as CMOS transistors are significantly superior to TFTs, particularly that TFTs suffer from $>10^3$ lower carrier mobility (limiting the application space to very low speed applications; see Section 3), significantly higher (often intractable) variability, etc.; see later. Nevertheless, a Printed Electronics-only solution does offer other attractive attributes as delineated above. From these perspectives, Printed Electronics and silicon are often deemed as complementary technologies, and specific technology is judiciously exploited accordingly – not competing technologies.

In this review paper, the emphasis is Printed Electronics although some references will be made to Flexible Hybrid Electronics.In view of the emphasis from a circuits and systems perspective, this review paper is organized in a bottom-up fashion. In Section 2, we discuss the largely paucity of Printed Electronics circuits and complete systems. The review depicts the rudimentariness and nascence of Printed Electronics circuits, particularly that basic circuit parameters are largely reported and advanced parameters are unreported – Printed Electronics is indeed an emerging technology. This review provides insights into the enormity of the challenges to enable applications in the application space of Printed Electronics presented in Section 3. In Section 4, we present the complete supply chain of Printed Electronics, with emphasis on the challenges in each constituent chain and their inter-dependencies, and considerations for *functionality*, *design-ability* and *manufacturability*, and with an emphasis from a circuits and systems perspective. This review delineates the need for the circuit designer to adopt a holistic approach involving co-design and co-optimization between the different constituent chains. In Section 5, in view of these challenges, we review analog and digital circuit designs, expounding that contemporary circuit design philosophies and methodologies for silicon are largely inadequate for Printed Electronics circuits. To this end, we describe several esoteric design philosophies and methodologies that may accommodate the challenges of Printed Electronics and describe their overhead tradeoffs. Section 6 draws the conclusions.

II. A REVIEW OF PRINTED ELECTRONICS CIRCUITS AND SYSTEMS

Our review of Printed Electronics circuits is unique as it encompasses the full spectrum of Printed Electronics circuits, and is summarized in ten tables; undoubtedly some reported circuits will be omitted due to the diversity of journals whose interests include Printed Electronics. Tables 1-4 pertain to digital circuits, Tables 5-6 to analog circuits, Tables 7-8 to mixed-signal circuits,and finally, Tables 9-10 to several Printed Electronics 'systems'.

At the outset, it is edifying to note that what strictly constitutes as Printed Electronics is contentious as different groups and associations define and interpret 'printed' differently. There are several cases in Tables 1-10 that are contentious, such as circuits realized in poly-silicon

TABLE II
PRINTED ELECTRONICS RING OSCILLATORS

Reference	Year	Oscillating frequency (Hz)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Zhou *et al.* [28]	2016	96	PET	Screen printing	120	No
Jinsoo *et al.* [29]	2015	4	Plastic	Gravure printing	-	-
Kempa *et al.* [30]	2011	134	PET	Gravure printing, flexography printing	140	-
Huebler *et al.* [31]	2007	3.9	PET	Gravure printing, flexographic offset printing	-	-
Sekitani *et al.* [32]	2010	44	PI	Evaporation	100	-
Ishida *et al.* [33]	2012	156	PEN	Evaporation	-	Vacuum, O_2 plasma
Nausieda *et al.* [34]	2010	1.5	-	Photolithography, CVD, evaporation	-	-
Sun *et al.* [35]	2011	2k	PEN	Photolithography	145	O2 plasma
Baeg *et al.* [36]	2013	80k	PEN	Photolithography, spin coating	200	N_2
Mandal *et al.* [37]	2015	1k	PEN	Inkjet printing, chemical drilling, bar coating.	120 (>24hrs)	-
Daami *et al.* [38]	2011	70	PEN	Sputtering, laser ablation, screen printing	100	-
Abdinia *et al.* [39]	2012	1.2k	PEN	Sputtering, laser ablation, screen printing	-	O_2 plasma
Takamiya *et al.* [40]	2007	339	PEN	Evaporation, CO_2 laser	180	Vacuum
Hübler *et al.* [41]	2011	6	PET	Gravure printing, flexography printing, laser cutting	-	-

Additive processes | Subtractive processes

TABLE III
PRINTED ELECTRONICS LOGIC GATES, FREQUENCY DIVIDER, SHIFT REGISTERS AND DECODERS

Reference	Year	Circuits	Delay (ms)	E_{per} (μW)	Area (cm^2)	NM_H/NM_L (V)	Supply voltage (V)	I_{on}/I_{off}	Substrate	Fabrication process	Max temp. (°C)	Chamber
Ours [42]	2014	NAND gate	50	-	-	1.5/15	60	*p*: 10^5	PET	Screen printing	120	No
Ramon *et al.* [15]	2016	NAND gate	100	-	-	-	25	*p*: 10^2	PEN	Inkjet printing	-	N_2
Taylor *et al.* [23]	2014	NAND gate, NOR gate	1	-	-	-	40	-	PEN	Evaporation	-	Ar, N_2, vacuum
Ishida *et al.* [33]	2012	Frequency divider	20	-	-	9/6.7	20	-	PI	Evaporation	-	Vacuum
Cao *et al.* [25]	2008	NAND gate, NOR gate	1	-	-	-	5	*p*: $10^{3.5}$*	PI	Photolithography, CVD	-	-
Mandal *et al.* [37]	2015	D-latch	0.3	-	-	15.4/15.4	60	*p*: 10^3*	PEN	Inkjet, chemical drilling, bar coating	120 (>24hrs)	-
Schwartz *et al.* [43]	2013	Shift register	5	2.6-7.6	~0.3	-	20	-	PET	Inkjet, spin coating, laser ablation	-	-
Seong, *et al.* [44] +	2006	Shift register	10	-	-	-	35	-	Glass	a-Si TFT technology	280	-
Fluxrnan *et al.* [27] +	1994	Shift register	0.02	-	-	-	-	*p*: 10^6 *n*: 10^6	Glass	poly-Si TFT technology	600	-
Cao *et al.* [25]	2008	Decoder	1	-	~1.5	-	5	*p*: $10^{3.5}$*	PI	Photolithography, CVD	-	-
Someya *et al.* [45]	2007	Decoder	30	-	-	-	100	-	-	Vacuum sublimation, inkjet and screen printing	180	N_2, vacuum
Ng *et al.* [46]	2012	Decoder	2	-	~8	-	30	*p*: $10^{2.5}$* *n*: 10^5*	PEN	Laser ablation, inkjet, laser drilling	-	-

Additive processes | Subtractive processes

* Our estimation based on reported data + a-Si or poly-Si

(poly-Si) or amorphous-silicon (a-Si), including an inverter [27] in Table 1, shift registers [27], [44] in Table 3, microprocessors [47]–[49] (and lithography [50], [51]) in Table 4, amplifiers [59]–[62] in Table 5, comparators [66] in Table 6, and Digital-to-Analog Converters [59], [69], [67] in Table 7 – they are indicated with '+' in these tables. Some of these were reported in the early 1990s and outperforms state-of-the-art printed electronics circuits. In our review here,

TABLE IV

'PRINTED ELECTRONICS' MICROPROCESSORS; NOTE THAT THEIR CLASSIFICATION AS 'PRINTED' IS CONTENTIOUS

Reference	Year	Speed (instructions/second)	Area (cm^2)	Power (µW)	Transistor count	Supply voltage (V)	Substrate	Fabrication process
Takayama *et al.* [47] +	2004	10M	-	-	-	3.3	Plastic	poly-Si TFT technology, transfer process
Dembo *et al.* [48] +	2005	3.39M	1.96	-	71k	3.3	Plastic	poly-Si TFT technology, transfer process
Karaki *et al.* [49] +	2005	30k-500k	6.5	~725	32k	3.5-7	Plastic	poly-Si TFT technology, transfer process
Myny *et al.* [50]	2012	40	3.4	100	3381	10	PEN	Photolithography
Myny *et al.* [51]	2014	2.1k	2.3	-	3504	12	Rigid substrate	Photolithography, inkjet printing

Additive processes | Subtractive processes

+a-Si or poly-Si

TABLE V

PRINTED ELECTRONICS AMPLIFIERS

Reference	Year	Open-loop gain (dB)	GBW (Hz)	Noise	Distortion (dB)	Max. I_{out} (µA)	R_{out}	Power (µW)	Supply voltage (V)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Chang, *et al.* [14]	2014	27	70	-	-	-	-	-	60	PET	Screen printing	120	No
Fuketa *et al.* [52]	2014	28@1Hz	2k	-	-	-	-	30	2	PEN	Evaporation	90	O_2 plasma
Ishida *et al.* [33]	2012	5.5	150	-	-	-	-	-	20	PI	Evaporation	-	Vacuum, O_2 plasma
Fukuda, *et al.* [53]	2015	12	-	-	-	-	-	-	20	PEN	CVD, inkjet printing	120	N_2, 30°C and 95%RH
Maiellaro *et al.* [54]	2013	40	1.5k	-	THD: -46	160	-	650	50	PEN	Photolithography, laser ablation, screen printing	-	O_2 plasma
Khaeradmand *et al.* [55]	2016	18@400Hz	18k	-	-	-	-	-	80	PET	Laser drilling, gravure, flexography, and screen printing	-	-
Kane *et al.* [56]	2000	8.5	-	-	-	-	-	-	20	PEN	Photolithography	150	O_2 plasma
Nausieda *et al.* [34]	2011	36	7.5	-	-	-	-	2.5×10^{-4}	3	-	Photolithography, CVD, evaporation	-	-
Miguel *et al.* [57]	2017	10	3k	-	-	-	-	49	10	Plastic	Photolithography, e-beam evaporation, thermal evaporation	-	-
Guerin *et al.* [24]	2011	22	-	-	-	-	-	40	40	PEN	Laser ablation, screen printing	100	No
Marien *et al.* [58]	2010	23	500	-	-	-	-	315	15	PEN	Photolitho., laser ablation, screen printing	-	O_2 plasma
Tarn, *et al.* [59] +	2010	43	30k	-	-	-	-	3.6×10^{3}	25	Glass	a-Si TFT technology	280	-
Moy *et al.* [60] +	2016	20	>100	10^{-13} V^2/Hz	-	-	-	-	55	-	a-Si TFT technology	-	-
Jacques *et al.* [61] +	2006	13.3	5.4k	-	-	-	-	-	25	Glass	poly-Si TFT technology	600	-
Hai-Gang, *et al.* [62] +	1994	44	450k	-	-	-	-	-	30	-	poly-Si TFT technology	620	-

GBW: Gain bandwidth; R_{out}: Output Resistance

Additive processes | Subtractive processes

+a-Si or poly-Si

we will not consider these as 'printed'– they are nevertheless included in these tables for sake of completeness and because they perhaps represent what may be possible for Printed Electronics.

Before reviewing the circuits tabulated in Tables 1-10, it would be instructiveto view the functionality of these circuits in the perspective that Printed Electronics is ideally a low-cost, green, print anywhere, on-demand, and scalable graphics-based 'printing press' to print electronics on mechanically flexible substrates – Printed Electronics is not a competitor to CMOS but complementary thereto. Low cost, being one of the most important attributes, means that the simplest process and with minimum infrastructure is desired.

In this context,we classify the circuitsin Tables 1-10 into two very broad categories: Fully-Additive and Subtractive processed; note that our classification as either Fully-Additive or Subtractive is sometimes contentious as many reported work do not disclose full details, and different groups have different definitions/interpretations thereto. Fig. 3 pictorially depicts the processing complexities between Fully-Additive and Subtractive processes for patterning a structure on a substrate. In general, because Subtractive processes require etching and/or lift-off, the processing steps are not only complex and requiring sophisticated/intensive infrastructure, but also involve toxic/corrosive chemicals (un-green), generally high chemical wastage (un-green and expensive),

TABLE VI
PRINTED ELECTRONICS COMPARATORS

Reference	Year	Input sensitivity (V)	Input offset (V)	Input range (V)	Comparison rate (Hz)	Power (µW)	Supply voltage (V)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Nausieda *et al.* [63]	2011	-	0.2	-	0.14	5×10^{-3}	5	Plastic	Photolithography, CVD, evaporation	-	-
Maiellaro *et al.* [54]	2013	-	1	-	120	-	60	PEN	Photolithography, laser ablation, screen printing	-	O_2 plasma
Abdinia *et al.* [39]	2012	-	0.2	-	50	-	40	PEN	Sputtering, laser ablation, screen printing	-	O_2 plasma
Abdinia *et al.* [63]	2014	-	2	-	1	6	40	PEN	Laser ablation, screen printing	100	-
Miguel *et al.* [57]	2017	-	1	-	10k	100	10	PC	Photolithography	-	-
Marien *et al.* [64]	2011	0.2	0.4	-	1k	180	20	PI	Photolithography, laser ablation, screen printing	-	O_2 plasma
Hara *et al.* [65] +	2004	-	-	-	-	-	4	Glass	poly-Si TFT technology	-	-

+a-Si or poly-Si

Additive processes | Subtractive processes

TABLE VII
PRINTED ELECTRONICS DIGITAL-TO-ANALOG CONVERTERS

Reference	Year	Conversion rate (S/s)	Resolution (bit)	INL, DNL (LSB)	SNR (dB)	SNDR (dB)	SFDR (dB)	Power (µW)	Supply voltage (V)	Area (cm^2)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Chang, *et al.* [14]	2014	300	4	0.8, 0.9	-	-	-	-	60	~15	PET	Screen printing	120	No
Wei *et al.* [66]	2010	100	6	0.6, 0.8	-	-	24	-	3	~1.5	Glass	Photolithography, evaporation,	90	O_2 plasma, vacuum
Abdinia *et al.* [67]	2013	-	4	0.2, 0.4	25.8	19.6	-	-	40	7.1	PEN	Photolithography, laser ablation	-	O_2 plasma
Tarn *et al.* [59] +	2010	900	4	0.2, 0.7	-	-	-	-	25	5.1	Glass	a-Si TFT technology	280	-
Dey *et al.* [68] +	2010	500	7	1, 0.6	-	-	-	14	20	0.08	PEN	a-Si TFT technology	180	-
Lewis *et al.* [69] +	1992	71k	4	0.06, 0.06	-	-	-	-	15	-	Glass	poly-Si TFT technology	-	-

+a-Si or poly-Si

Additive processes | Subtractive processes

TABLE VIII
PRINTED ELECTRONICS ANALOG-TO-DIGITAL CONVERTERS

Reference	Year	Conversion rate (S/s)	Resolution (bit)	INL, DNL (LSB)	SNR (dB)	SNDR (dB)	SFDR (dB)	Power (µW)	Supply voltage (V)	Area (cm^2)	Substrate	Fabrication process	Max temp. (°C)	Chamber
Abdinia *et al.* [68]	2013	~2	4	-	25.7	19.6	-	540	40	24.5	PEN	Photolithography, laser ablation	-	O_2 plasma
Marien *et al.* [58, 64]	2011	-	-	-	26.5	24.5	-	-	15	2.6	PEN	Photolithography, laser ablation, screen printing	-	O_2 plasma
Wei *et al.* [66]	2010	100	6	1.5, -3	-	-	-	3.6	3	6.2	Glass	Photolithography, evaporation,	90	O_2 plasma, vacuum

Additive processes | Subtractive processes

usually high temperature (low-cost PET cannot be used), slow-to-print (not on-demand), and often unscalable (e.g., unable to print wallpaper size) – these largely contradict the aforesaid ideal Printed Electronics process. Put simply, Fully-Additive All-Air Low-Temperature Digital (not requiring masks/masters) processing is preferred. Nevertheless, Subtractive processes often yield better performance in terms of carrier mobility, higher resolution and reduced variations – this will be evident in Tables 1-10.

For completeness, Fig. 4 summarizes the different Printed Electronics printing processes, broadly classified as either Fully-Additive or Subtractive processes. Again, note that there are many variations, for example, a given process may embody more than one processing type, such as screen printing

TABLE IX
PRINTED ELECTRONICS SYSTEMS: RFIDS

Reference	Year	I_{on}/I_{off}	Operation frequency (Hz)	Reading distance (cm)	Data rate (bit/s)	Rectifier realization	Substrate	Fabrication process	Max temp. (°C)	Chamber
Minhun *et al.* [70]	2014	*p*: 10^3*	13.56M	2	-	Diode	PET	Gravure, Inkjet and pad printing	150	-
Fiore *et al.* [71]	2015	*p*: 10^7 *n*: 10^6*	13.56M	2-5	50	Transistor	PEN	Photolitho., laser ablation, and screen	-	O_2 plasma
Myny *et al.* [72]	2008	-	13.56M	10	787	Diode	PEN	Photolithography, spin coating	-	-
Myny *et al.* [73]	2014	*p*: $10^{1.5}$* *n*: 10^3*	13.56M	-	1.2k	Transistor	Rigid substrate or PEN	Evaporation, atomic deposition, spin coating	250	Vacuum
Blache *et al.* [74]	2006	*p*: $10^{1.5}$* *n*: $10^{1.5}$*	13.56M	4.5	-	Diode	Polyester	Photolithography, spin coating	-	-
Cantato *et al.* [75]	2007	*p*: 10^5*	125k	-	1k	Transistor	Plastic	Photolithography	-	-

* Our estimation based on reported data

Additive processes | Subtractive processes

TABLE X
PRINTED ELECTRONICS SYSTEMS: OTHERS

Systems	Reference	Year	Modules	Substrate	Fabrication process	Max temp. (°C)	Chamber
e-skin	Tee *et al.* [76]	2015	Pressure sensor	Polyurethane (transferred from wafer)	Spray coating, spin coating, evaporation	200	-
			Organic ring oscillator	PEN	Inkjet printing	-	No
OLED display	Ryu *et al.* [77]	2013	Active matrix OLED display	Glass	Photolithography, evaporation	-	-
			Organic display backplane	Glass	Photolithography, screen printing, spin coating, inkjet printing	-	-
Microphone array for audio source separation	Sanz-Robinson *et al.* [78]	2015	Microphones	PVDF (clamped to acrylic posts)	Spray coating		-
			Amplifier	Glass	a-Si TFT technology (e.g., PECVD*, and laser scribing)	180	-
			Scanning circuit	Glass	a-Si TFT technology (e.g., PECVD*, and laser scribing)	180	-

* PECVD: Plasma-enhanced chemical vapor deposition

Additive processes | Subtractive processes

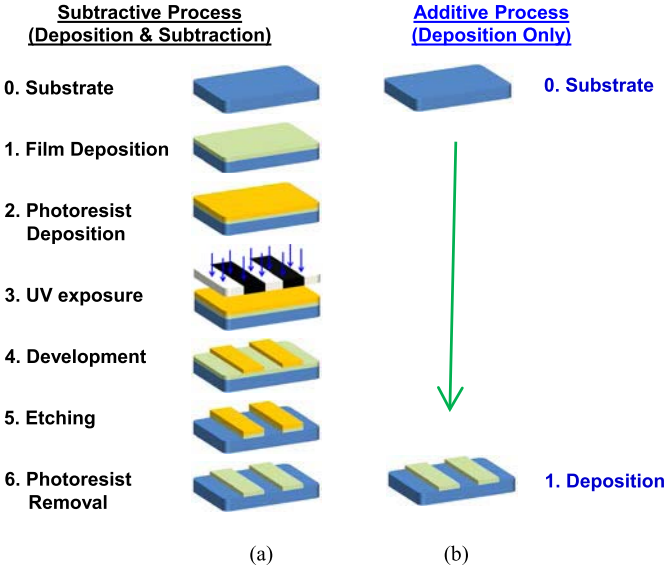


Fig. 3. Processing steps [12] to pattern a structure in a typical (a) Subtractive Process involving etching/lift-off, and (b) Fully-Additive Process; UV: Ultra-violet.

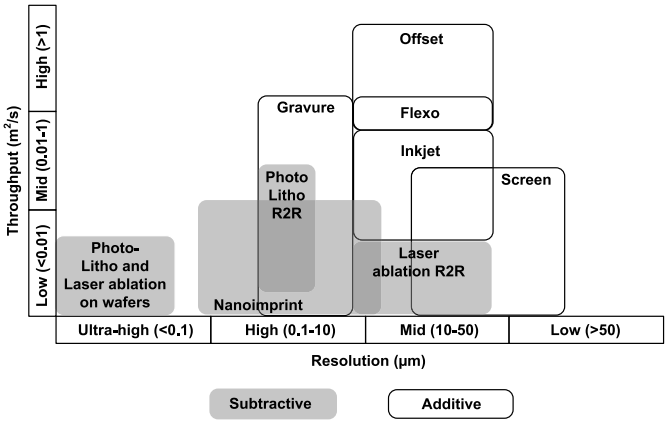


Fig. 4. Printed Electronics: Printing/Patterning Processes; adapted from [3]. R2R: Reel-to-Reel.

involving inkjet printing in one or more steps, and a combination of Fully-Additive and Subtractive processing. As there are many reported reviews on the materials and printing processes (e.g., [79], texts [80], [81], websites [82], consortia roadmap whitepapers [1]–[3]), our comments on materials and printing are largely only cursory.

At the outset, note that the tabulations in Tables 1-10 are not for benchmarking – benchmarking would not be meaningful because of the diversity of and permutations in the processing, different intended applications, etc.For completeness, note that a number of data are our estimates based on the other reported

data in the pertinent references, and are indicated with the symbol '*'.

On the basis of Tables 1-10, we make the following comments. For digital circuits in Tables 1-4, our first comment is that the reported parameters of digital circuits are largely very rudimentary parameters, i.e., the most advanced/complete parameters are unreported. For example, very few papers report the noise margin of their inverters, and out of the ten studies on digital gates, only one group provided energy per operation (not indicated in Table 1). Second, as expected (vide infra), most printed digital circuits are based on uni-polar p-type transistors (row 3 in Table 1). Not unexpectedly, the ensuing noise margin is low.For example, in the case of a p-type-only inverter with a diode-connected load (see Fig. 8(a) later), the output signal swing degrades, i.e., the output is unable to be pulled to V_{DD}, thereby compromising the noise margin.

Third, as expected, the speed of printed digital circuits is very slow. For example, the highest frequency of the reported ring oscillators is 80kHz compared to 10s of GHz in state-of-the-art silicon ring oscillators. Further, also as expected, the area is significantly larger than their silicon counterparts.Fourth, I_{ON}/I_{OFF}, an imperative parameter in digital circuits, is generally low (typically $10^3 - 10^4$) in Printed Electronics – several orders of magnitude lower than silicon (typically $\sim 10^8$). This renders Printed Electronics digital circuits unreliable because the 'on' and 'off' states are less rigorously defined, and the noise margin suffers.

Fifth, there are a number of reported inverters based on Additive and Subtractive processes. As expected, as the complexity of the digital circuits increases, from simple inverters to ring oscillators to gates to 'complex' microprocessors, the number of reported circuits realized is increasingly based on Subtractive processes. This is largely because the Subtractive processes offer higher carrier mobility, higher resolutions and smaller process variations. Nevertheless, as delineated earlier, the shortcomings of Subtractive processes over Fully-Additive processes are substantial, particularly cost, complexity of printing and infrastructure, non-green, etc. Sixth, congruous to the said fifth, digital circuits realized by Subtractive processes in general feature superior performance over their Fully-Additive realized counterparts. For instance, the fastest oscillation frequency amongst the ring oscillators tabulated in Table 2 is 80kHz [36] which is realized by a Subtractive process. Conversely, the highest oscillating frequency of Fully-Additive printed ring oscillators is $\sim$150Hz [30], [33].

Seventh, a comprehensive cell library, embodying a number of logic gates, is an imperative constituent of the design flow process for realizing complex digital systems. Table 3 tabulates the reported Printed Electronics digital logic gates where the number of reported work is not only exiguous but the range of the various gates types is limited – highly incomplete for a comprehensive cell library. Eighth, compared to silicon, the performance and functionality of Printed Electronics digital circuits in Tables 1-3 remain rudimentary. Arguably, a representative state-of-the-art digital circuit in Printed Electronics is a microprocessor tabulated in Table 4– as delineated earlier, it is contentious to classify these realizationsas 'printed'. Nevertheless, these 'printed' microprocessors reportedly featured an impressive transistor count of $>$3,000; a transistor count that beyond 'state-of-the-art' Printed Electronics. This is comparable to the 2,300-transistor Intel 4004, the first silicon microprocessor [83] realized in 1971 – approximately five decades ago. Although the clock rate (2.1kHz) of this 'printed' microprocessor is very impressive in the context of Printed Electronics, it is significantly slower than the 92kHz clock rate of Intel's 4004.

Ninth, in the perspective of low cost for Printed Electronics – hence Fully-Additive (vis-à-vis Subtractive) and the use of low-cost plastic films (e.g., PET where the maximum processing temperature is 120 °C) – there are very few reported processes capable of printing at least a ring-oscillator. Tenth, further to said ninth, the performance of these printed digital circuits is very modest, including very low speed and high voltage operation.

Consider now the analog circuits in Tables 5-6 where in the perspective of analog circuits, amplifiers are the most rudimentary circuits [84], while the comparators are also common. Our comments are as follow. First, similar to reported digital Printed Electronics circuits, the reported parameters of the printed analog circuits are rudimentary where 'advanced' parameters are unreported. For example, out of the eleven papers on amplifiers, only one group provided the distortion parameter and none provided the output noise level of their printed amplifiers. To-date, it appears that there is few, if any, reported work that cite other important non-linearity parameters such as Total Harmonic Distortion + Noise (THD+N), Intermodulation Distortion (IMD), Slew Rate, Power Supply Rejection Ratio (PSRR), etc. Second, as expected and although not tabulated in Tables 5-6, most of the printed analog circuits are based on uni-polar p-type transistors. This limitation poses difficult design issues that are otherwise easily resolved with complementary device, including low gain due to the lack of high impedance current mirror loads, voltage level shifting, etc.; see Section 5 later.

Third, as expected, the open-loop gain and gain-bandwidth of printed amplifiers are very low. For example, the highest open-loop gain of the printed amplifiers is a low 36dB while open-loop gains exceeding 100dB are common in their silicon counterparts – over 4 orders of magnitude higher. Also, the highest gain-bandwidth of printed amplifiers is 18kHz while their silicon counterparts routinely report $>$10MHz – approximately 3 orders of magnitude higher; if there is no need for stability (arising from Miller Capacitance), the gain-bandwidth of silicon amplifiers can be significantly higher than 100s MHz. From a circuits and systems perspective, the lack of high open-loop gains to obtain predictable, consistent and low distortion transfer functions is a serious shortcoming for analog circuit design; see Section 5 later.In the comparator, the input sensitivity is low and the input offset voltage high. For the only comparator [64] that reported its input sensitivity, the input sensitivity is a poor 0.2V and lowest offset voltage is a high 0.2V. By comparison, silicon-based comparators easily resolve μV (input sensitivity) and their offset is often $<$1mV. Fourth, as the transistor count in the printed amplifiers and comparators is low, the ensuing amplifiers are simple

architectures. For example, most of the amplifier architectures are reportedlysingle stage differential amplifiers.

Fifth, there are a number of reported amplifiers based on Additive and Subtractive processes. As expected, in general, amplifiers based on Subtractive processes feature higher performance over their Additive process counterparts. For example, the highest open-loop gain amplifier [34] and the widest gain-bandwidth amplifier [55] are both based on the Subtractive process; note the shortcomings of Subtractive processes compared to Fully-Additive processes. As in the case of the digital circuits, this is largely because the Subtractive processes offer higher carrier mobility, higher resolutions and smaller process variations. Sixth, in view of the spirit of low-cost Printed Electronics – hence Fully-Additive and the use of low-cost plastic films (e.g., PET whose maximum processing temperature is 120 °C) – there are very few reported circuits that are printed with processes whose maximum temperature is 'low', $\leq$120C.

Tables 7-8 tabulate Printed Electronics mixed-signal circuits – Digital-to-Analog Converters and Analog-to-Digital Converters. On the basis of these tables, we make the following comments. First, there are only a few reported mixed-signal circuits. This is probably attributed to the difficulty of mixed signals because they embody both digital and analog circuits.Second, similar to printed digital and analog circuits, the reported parameters of the Printed Electronics mixed-signal circuits are likewise very rudimentary. For example, out of the six reported work, only two provided the power consumption. Third, the resolution of reported mixed signal circuits is very modest. In the case of converters on rigid substrates, the highest reported resolution is 6 bits. In the case of the converters on flexible substrates, the resolution is even lower, 4 bits. This low resolution can probably be attributed to the need for precise matching between transistors and passive devices (e.g., capacitors, and resistors); see Sections 4 and 5 later. By comparison, their silicon counterparts routinely report very high resolutions, e.g., 24 bit resolutions using sigma delta methods. Fourth, further to said third, the speed of Printed Electronics mixed-signal circuits is very low. For instance, the highest speed is a low 100s samples/s conversion rate compared to that exceeding 1 GHz (yet with high 12-bit resolutions) in silicon, usually embodying time interleaving methods.

Subsequent to the limited Printed Electronics digital, analog and mixed signal circuits, it is not unexpected that there are only a limited number of Printed Electronics-only realized systems. These are tabulated in Tables 9-10 which are respectively Printed Electronics realized Radio Frequency Identification tags (RFIDs)and other Printed Electronics-realized systems, including e-skin, OLED display with backplane, and a flexible microphone array for audio source separation. On the basis of these tables, we make the following comments.First, despite that the paucity of Printed Electronics systems, the diversity of applications is wide; see Section 3. This is not unexpected, as delineated earlier, because of the unique attributes offered by Printed Electronics, particularly its thin form factor, and mechanical flexibility.Second, Printed Electronics systems have limited signal processing capabilities – i.e., its 'intelligence' is rudimentary. For instance, the signal sensing circuit used in the e-skin [77] is simple ring oscillator that changes with pressure sensed by a pressure sensor. In our view, the rudimentary intelligence may not necessarily be limiting if the functionality is sufficient. In the e-skin example, the natural transduction process in sensing pressure is indeed a change in the frequency of the electrical impulses from the skin to the brain – the change in frequency of a ring oscillator.Third, it is interesting that of all Printed Electronics systems, the RFID is most prevalent. This is probably because of its thin flexible form-factor attributes offer over rigid RFIDs, e.g., for RFIDs placed on curvilinear surfaces. Nevertheless, we note that all Printed Electronics RFIDs are near-field RFIDs, and far-field RFIDs remain unreported. We attribute this to the operating frequency of near-field RFIDs being significantly lower than that of the far-field RFIDs, e.g., typically 128kHz and 13.56MHz of the former against $>$100MHz, e.g., 2.45GHz, of the latter. Note that these frequencies pertain to printed diodes (rectifiers) that may be realized as a diode or a diode-connected TFT.

In summary, the sophistication or intelligence of Printed Electronics circuits is modest and significantly inferior to their silicon counterparts – Printed Electronics is complementary to silicon because of its unique flexible form factor, etc. We will now review the application space of Printed Electronicsand this depicts how its unique attributes may be exploited and conversely, in the perspective of Printed Electronics circuits, the enormity of the challenges.

III. Application Space and Functional Modules of Printed Electronics

The application space and functional modules of Printed Electronics and Flexible Hybrid Electronics are similar and ideally, the Printed Electronics solution is preferred as a significantly lower cost and greener solution. Nevertheless, where considerable signal processing is needed, it is likely that a Flexible Hybrid Electronics solution is more appropriate.

There are a number of whitepapers [1]–[6] from variousconsortia, including OE-A, iNMEI, ITRS, PSMA, OIDA, FlexTech, CPEIA, etc., that outline the application space and clusters of applications. For example, the application clusters in OE-A's roadmap comprises five clusters: OLED Lighting, Organic Photovoltaics, Flexible and OLED Display, Electronics and Components, and Integrated Smart Systems; while CPEIA's roadmap comprises six clusters: Secure Printing, Defense, Packaging, Health and Wellness, Marketing and Commerce, and Consumer Electronics. In general, the clusters of applications by the different consortia are largely the same but named or classified slightly differently or they overlap. Our review on the application space will be succinct.

In OE-A's roadmap, printed circuits are mostly grouped as 'printed logic chips' whose applications are largely under the Electronics and Components, and Integrated Smart Systems application clusters. Of particular interest, the 2013 OE-A whitepaper [85] projected that 'printed logic chips' will be available in large volumes only from 2017-2019. This projection has now been postponed by two years to 2019-2022 in the latest 2015 OE-A whitepaper [3]. This is congruous to

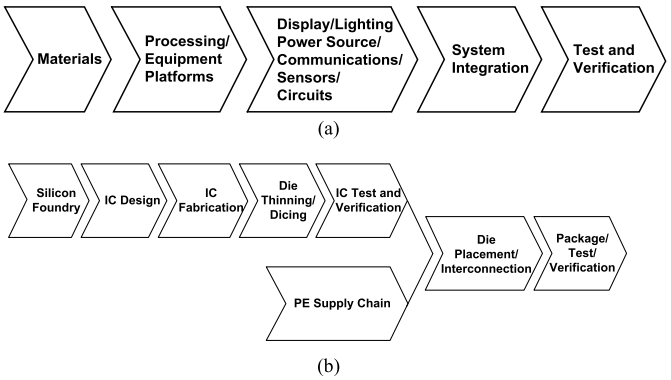


Fig. 5. Supply Chain of (a) Printed Electronics (PE) and (b) FlexibleHybrid Electronics.

the general view that Printed Electronics largely remains an emerging field, and many formidable challenges remain; see Sections 4 and 5.

At this juncture, other than OLED displays, the Printed Electronics 'killer application' remains largely unidentified, and as in many emerging technologies, the 'killer application' can be very surprising. Nevertheless, it is likely that in all application clusters, analog and digital signal processing is required to realize intelligence – it is expected that the intelligence realized by Printed Electronics will be modest-to-moderate and strategic (such as to maintain signal integrity in a large area) as silicon easily provides substantially higher signal processing/intelligence. Even 'non-intelligent' products are expected to embody some 'intelligence' e.g., OLED lightning is expected to self-calibrate its lumens output to provide consistent lighting as the light output efficiency of its OLEDs degrades over time. In short, there is a need for at least some intelligence in virtually all Printed Electronics products – hence the need for analog, digital and mixed-signal Printed Electronics circuits.

IV. Supply Chain and Challenges

Fig. 5(a) and (b) respectively depicts the supply chain of Printed Electronics and Flexible Hybrid Electronics. As Flexible Hybrid Electronics embodies both silicon (usually thinned or very small dies) and Printed Electronics, its supply chain would embody both silicon and Printed Electronics supply chains, and then combined with die placement and package, test and verification. The details of each constituent and overall supply chain of Printed Electronics are discussed elsewhere and in numerous industry whitepapers, including OE-A [3], iNEMI [1], IDTechEx [2], etc., and their challenges are well recognized. However, as the perspectives from a circuits and systems view point is either largely cursory or lacking, we will now review Printed Electronics from this perspective, including its overall supply chain and each constituent chain therein, the interdependencies between the individual constituent chains, and challenges to Printed Electronics circuit design and realization – including functionality, design-ability and manufacturability.

The key electrical performance parameters of printed elements and to a large degree the ensuing circuits is ascertained in the first two constituent chains, 'Materials' and Printing ('Processing Equipment Platforms'). For Materials, the key challenges include:

- Charge carrier mobility. High carrier mobilities are desired for higher speed TFTs and their ensuing circuits. In most cases, mobilities are <1 cm^2/Vs – although many groups reported TFTs with much higher mobilities, they are largely for a single or very few carefully 'manicured' TFTs. By comparison, the carrier mobility of silicon is $>10^3$cm^2/Vs or higher.
- Complementary devices. The p-type semiconductor is prevalent while the n-type is less common. This was already evident in our review of printed circuitstabulated in Tables 1-10 that most circuits embody only unipolar p-type TFTs; designs in [108] and [109] are a few examples of complementary TFTs. Designing circuits with unipolar devices only are challenging in terms of gain, noise margin, voltage level shifting, etc.; see Section 5. Further, until of late, n-type semiconductors typically suffer from several orders of magnitude lower mobility than p-type semiconductors – the converse of silicon.
- Solution processibility. There are several aspects. First, there is a need for more formulations that are non-toxic, hence 'Green'. Second, these formulations should provide for combined high mobility and high uniformity. The uniformity is imperative in circuits because this in part defines the variations of and the matching between printed elements; see Section 5. The variations should be small because the performance of circuits needs to be designed to the worst-case variations. The matching between printed elements is important because the transfer function of many circuits is defined by the ratio of the elements. The matching between a pair of TFTs is also critical in many circuits such as the differential amplifier. Third, these should be reproducible in industrial quantities.
- Efficiency. For photovoltaics andpower-related applications, it is desirable that the energy conversion, energy storage, brightness, conductivity of the conductor or electrolyte, etc., be high.
- Environmental stability. The materials should environmentally stable for sufficient operational lifetime of the Printed Electronics device. The environmental stability also in part defines the variations of printed devices where for the Printed Electronics device, the worst-case variations would need to be accommodatedthroughout its lifetime. Innately environmentally stable materials would mitigate the barrier requirements of the barrier encapsulation, potentially reducing the cost and weight of the Printed Electronics device. It is also often required for the barriers to be transparent (e.g., for photovoltaics), low-cost and mechanically flexible.

Fig. 4 earlier summarized the different printing processes (Processing/equipment platforms), including their general classification and their resolutions and printing throughput. The key challenges of the second constituent supply chain are closely related to the first constituent chain, and include:

- Resolution. Congruous with silicon, ever-smaller minimum feature size is desired as the parasitics are

smaller, etc., yielding higher speedTFTs and the ensuing circuits. The resolution of most printing processes is between 5μm-100μm. The desire for high resolution applies to the full range of active and passive printed elements.

- Registration. This refers to the accuracy of overlaying layers when printing the different layers. It is desired that the registration is accurate, and this becomes increasing critical in high resolution printing. If the registration is poor, the variations of the printed elements undesirably increase, particularly TFTs.
- Uniformity and variations. It is desirable that the printing is uniform and defect-free. As discussed earlier, uniformity is imperative for low variations. For TFTs, the imperative variations include carrier mobility, threshold voltage, Ion/Ioff, etc.; see Section 5 later. In general, large variations and poor matching between TFTs (and low carrier mobility) are the most formidable challenges to Printed Electronics circuits.
- Throughput. It is desirable that the printing has high throughput (quick printing). In general, reel-to-reel printing (R2R in Fig. 4) that features high throughput is desirable.
- Range of printed elements. To allow full circuit functionality, all electronic elements should be printable on the same substrate, including active (p-type and n-type TFTs) and passive (resistors, capacitors, inductors, interconnects, antennas, etc.) electronic elements. The quality of these elements should be high, for example, high Q inductors, high capacitance per unit area and low leakage for capacitors, low resistivity per square for conductors, a comprehensive range of resistivities for resistors, etc.
- Low operating voltage. The printed TFTs should be operable at low supply voltages (VDD). Many printed TFTs operate with VDD exceeding 20V, and it is desirable that they operate in the same voltage supply as silicon, typically $\sim$1V-3.3V.
- Types of TFTs. Most TFTs are not only unipolar but are also depletion-mode. While depletion-mode is desirable in some applications where the TFTs are always 'on', they require a negative voltage to turn 'off'. The need for a negative supply complicates the overall system design. It is desirable that both enhancement-mode and depletion-mode TFTs are available – in addition to complementary type devices, p-type and n-type.
- Cost. As low-cost is one of the most imperative attributes of Printed Electronics devices, it is likewise imperative that the overall cost of printing is low, both the printing process and infrastructure.

To put the aforesaid challenges of printing in perspective, particularly the need for the most cost-effective printing to meet the requirements of a given Printed Electronics application, we summarize in Table 11 the general features of the various printing processes in Fig. 4. Note that these are very generalized features of the various processes where because of the large diversity of the various printing methods, there are many exceptions.Other than the classification of Subtractive and Additive, there are other classifications with respect to different features, such as pattern type, contact mode, analog or digital, and scalability.

TABLE XI
FEATURE COMPARISON OF VARIOUS PATTERNING PROCESSES

Printing Process*	Subtractive /Additive	Pattern type	Contact	Analog/ digital	Scalable
Photolithography	Subtractive	Indirect	Photolitho-graphy	Analog	No
Photolithography R2R	Subtractive	Indirect	Photolitho-graphy	Analog	Yes
Laser ablation	Subtractive	Indirect	Non-contact	Digital	Partially
Laser ablation R2R	Subtractive	Indirect	Non-contact	Digital	Yes
Imprinting	Subtractive	Indirect	Contact	Analog	Yes
Nanoimprint lithography	Subtractive	Indirect	Contact	Analog	Yes
Inkjet	Additive	Direct	Non-contact	Digital	Partially
Aerosol jet	Additive	Direct	Non-contact	Digital	Partially
e-jet (electro-hydrodynamic)	Additive	Direct	Non-contact	Digital	No
Flatbed screen	Additive	Direct	Usually contact	Analog	Yes
Rotary screen	Additive	Direct	Contact	Analog	Yes
Flexography	Additive	Direct	Contact	Analog	Yes
Gravure	Additive	Direct	Contact	Analog	Yes
Gravure offset (Pad)	Additive	Direct	Contact	Analog	Yes
Offset lithography	Additive	Direct	Contact	Analog	Yes
Soft lithography (e.g., micro contact)	Additive	Direct	Contact	Analog	Partially

In terms of contact mode, the printing processes may be classified as contact printing and non-contact printing. In most printing processes (such as flexography and gravure printing), physical contact is needed between the underlying material or substrate and the materials to be printed. This contact can cause several undesired effects, such as contamination, and perturbation of the physical structure of the underlying layer. A few printing processes (mainly jet printing methods, such as inkjet printing, and aerosol jet printing) are able to print materials with no physical contact with the underlying material or substrate.

The printing processes may also be classified as either analog and digital printing processes. Analog processes (such as screen, flexography, and gravure printing) typically use physical masks/masters for the layer patterning while digital processes (such as inkjet and aerosol jet printing) usually do not. Scalability is another attribute that can be used for classifying the printing processes. Scalability is important because there are impressive reported work on materials and printing but they are difficult to scale up. The most scalable processes are probably the reel-to-reel processes which may feature high throughput and large formats. Another imperative consideration is processing temperature – this is not classified here due to the overly diverse processing within each classification. Although there is no definitive definition to 'low-temperature', a reasonable definition of low-temperature is $\leq$120C as this is maximum temperature tolerated by cheap PET (polyethylene terephthalate)substrates.

In general, there are tradeoffs between the different attributes of the various processes. For instance, Additive processes generally feature high throughput but suffer from relatively poor resolution, while Subtractive processes feature higher resolution but generally suffer from low throughput. High throughput is imperative for low-cost. *Ideally, the printing is Fully-Additive, All-Air, Low-Temperature, Non-Contacting, Digital, Scalable and with high throughput* – resembling a low-cost, green, print anywhere, on-demand, and scalable graphics-based 'printing press' Printed Electronics process. Although there is no 'ideal' process, the closest 'ideal' printing process is arguably the inkjet but there are limitations, including nozzle reliability and high throughput. It is hence not surprising that inkjet has received the most interest for prototyping, and in the research setting.

The first two constituent supply chains have a profound effect on the third constituent supply chain – the circuits-related constituent chain embodying Display/Lighting/Power Source/ Communications/Sensors/Circuits.The real challenge here is how Printed Electronics circuits can be designed in view of the aforesaid challenges in the first two constituent supply chains. Essentially, if the specification of the desired application is higher than that the intrinsic properties of the printing technology, the designer has two options. The first is to wait for the printing technology to improve. The second – we advocate this – is to attempt new design methodologies (beyond contemporary design methodologies; see Section 5), including circuit design with co-design and co-optimization with materials and printing technology. The challenges in this third constituent chain for design methodologies include:

- Complexity. At this juncture, the complexity ('intelligence') of printed circuits remains modest; see Tables 1-10. This modest complexity is not unexpected given the challenges in the preceding two constituent supply chains. It is desirable that it would be possible to realize relatively sophisticated printed circuitsand for functionality, and applied strategically where a silicon solution is inappropriate.
- Speed and frequency. As the resolutions are large and carrier mobilities are low, the ensuing speed and frequency of printed circuits are low. At this juncture,the frequency of digital, analog, mixed-signal, and radio frequency circuits is usually at low kHz. For added functionality, it is desirable for printed circuits to operate at higher speeds and frequencies to expand their application space.
- Variations. The variations are significantly more severe than silicon, including CMOS circuits operating in the 'difficult' deep subthreshold [86], [87] region, e.g., VDD = 150mV. At nominal operating conditions, the typical carrier mobility and threshold voltage variations of reported Fully-Additive processes [14], [31], [88], [9], [90] on flexible substrates are $\pm 30\%$ and ± 1V respectively, while those of reported Subtractive processes [36], [91] are typically lower, at $\pm 20\%$ and ± 0.7V respectively. These large variations are only due to process, and would increase substantially with temperature and voltage variations (as PVT variations in silicon), and with ageing. Circuit designs would need to accommodate these large variations, ideally without heavy penalties such as hardware, power, area, etc., overheads. From a manufacturability perspective, unless circuit designs can accommodate these variations, the Printed Electronics devices cannot be manufactured with an adequate quality control.
- Bending. When the substrate with printed elements is bent, the characteristics of the printed elements would vary unless the substrate is very thin [92] or another substrate layer [32] of equal thickness is deposited over the top of the original substrate. Unfortunately both solutions have their shortcomings – extremely thin substrates are overly frangible and fragile, while the added deposited substrate increases the cost and thickness of the overall substrate. The variations due to bending is difficult because the radius of the bending may not be known,would need to be rigorously characterized. Given the variations from processing, PVT, ageing and bending, the collective variations may be intractable – this is arguably the most formidable challenge of Printed Electronics.
- Process Development Kit (PDK). At this juncture, PDKs for Printed Electronics are largely nascent [88], [107]. From a design-ability perspective, the PDK is a critical constituent of Computer-Aided-Design/Electronic-Design-Automation tools for a given fabrication technology. It largely embodies the models of the device (characteristics), and a set of layout design rules that define the minimum dimensions for printed devices and minimum distance between them. The PDK is imperative in modern circuits/systems design – for both silicon and Printed Electronics where it facilitates circuits/systems design including the prediction (by Monte-Carlo simulations) of the performance of the designs under various conditions. At present, the unavailability of mature PDKs is a major disconnect between the Printed Electronics processing community and the Circuits and Systems communities. In short, it is imperative that PDKs become available, including models encompassing all variations, ageing, when the substrate is bent at different radii, etc.

The fourth constituent supply chain is System Integration and pertains to integrating all components that enables the Printed Electronics device. The last constituent supply chain is Test and Verification, and the challenges include:

- Characterization. To guarantee product performance, the characterization of electronic devices should be in-line (after printing) and should be high throughput for low cost.
- Standards. Several associations have published standards for Printed Electronics, including the IPC's (Institute of Printed Circuits) IPC/JPCA-4921 -4591 and -2291); IEC's (International Electrotechnical Commission) TC119 technical committee; and IEEE's 1620-2008 and 160.1-2012. Nevertheless, these standards and regulations for Printed Electronics have yet to be completely finalized. The standards and regulations for silicon are only partially applicable but difficult for Printed

Electronics because they do not address the specifics and applications of Printed Electronics. In short, there is a need for standards specifically for Printed Electronics.

In summary, there are formidable challenges in each constituent chain and the entire supply chain of Printed Electronics, including from functionality, design-ability and manufacturability perspectives. These challenges are strongly inter-related – the need for and the opportunity ofco-design and co-optimization between circuit design and the other constituent supply chains.

V. Circuits and Systems Design for Printed Electronics

The formidable challenges to Printed Electronics circuit design, include the severe (possibly intractable) variability of printed TFTs, low carrier mobility, poor resolution, until of late the availability of *p*-type only, lack of PDKs, etc. At the outset here, it is instructive to appreciate that Printed Electronics circuits are not designed to compete with silicon but instead complementary thereto where its competitive attributes can be exploited. Given the modesty of Printed Electronics circuits and its unique form factor, it would be prudent that their circuit application is strategic or where a silicon solution is inappropriate, e.g. in large area applications [78].

Most of these challenges are not new to circuit designers as they resemble the early days of MOS in the 1980s and more recently, to deep subthreshold circuit designs [86], [87] in silicon. Although these issues have been discussed extensively in literature [93], the extent of the challenges of Printed Electronics is more formidable, particularly thesevere, possible intractably, variations and low carrier mobility. These are some of the reasons as to why most printed circuits are digital [94], albeit relatively simple logic gates, as evident from Tables 1-10 earlier.Inthis section, we will review why contemporary circuit design philosophies and methodologies for silicon are often inadequate to address these challenges. To this end, wewill present several esoteric design philosophies and methodologies that may, although contentiously, accommodate the aforesaid challenges, and discuss their merits and shortcomings.

A. Analog Circuits: Contemporary Designs, Esoteric Designs and Co-Design/Co-Optimizations

In contemporary analog circuit design, the most basic building block is the silicon op-amp and one of the basic (and adopted) design philosophies is negative feedback. By means of negative feedback [84], a predictable, repeatable, low distortion, low noise (including rejecting power supply noise) closed-loop transfer function is obtained. The fundamental requirement for negative feedback is high open-loop gain (and gain-bandwidth) of the op-amp where the open-loop gain needs to be significantly larger (typically >10x) than the closed-loop gain in the frequency range of interest. Put simply, the higher the open-loop gain, the lesser the error in the closed-loop transfer function.

Another imperative parameter for analog circuits is the matching between two transistors [28], [84]. For the current mirror that is employed to steer currents in an analog circuit and to provide current gain, the current ratio between two branches of the current mirror is determined by their transistor aspect ratios. As the variations of TFTs are high, the matching between two transistors is poor, leading to an imprecise output current and ensuing poorly defined current gain or output. This poor matching is also acute in differential-input circuits [84]; differential-input circuits are prevalent both in analog and digital circuits. Without good matching, the Common-Mode-Rejection-Ratio (the ratio between the amplification of differential signals over common-mode signals) is poor resulting in poor rejection of common-mode signals which are largely noise.

However, as printed TFTs are very slow, the printed amplifiers commensurably suffer from very low gain and gain-bandwidth(see Table 5). Consequently, the contemporary negative feedback design philosophy involving a high gain and gain-bandwidth op-amp is inapplicable. This inapplicability presents a design conundrum in analog design as many applications require well-defined low-noise transfer functions, including precise transfer functions for conditioning circuits for amplifying low-level electronic signals from printed sensors.

In view of the inapplicability of negative feedback, the analog Printed Electronics circuits designer can refer back to 'classical antiquated' analog circuit designs such as the pre-op-amp era where transistors were few and strategically used. Other approaches include where feedback is limited and localized [84], contemporary open-loop deigns such as current-mode circuits [95] and in high-frequency radio frequency circuit blocks, e.g., LTE power amplifiers, etc.

We will now review the design and realization of Printed Electronics differential amplifiers to address four critical challenges – (i) increasing gain (and gain bandwidth), (ii) common-mode sensitivity (to threshold voltage variations), (iii) matching between two transistors, and (iv) bending of the substrate. This review will illustrate the efficacy of combining esoteric design methodologies and co-design/co-optimizations between the first three chains, Materials, Printing and Circuit Design (and Layout). For completeness, it is important to note that other than high gain, another important consideration is the common-mode sensitivity of the amplifier due to variations in the threshold voltage (typically $\sim \pm 1$V) due to process variations; this is not often discussed in literature due to the nascence of Printed Electronics circuits.

Consider first the circuit design methodologies to obtain higher gain. One of the most common methods to increase the gain of an amplifier is to employ the cascode technique [84]. In general, this is avoided because this technique requires a higher V_{DD} voltage rail; refer to Challenges under Printing in Section 4. For an amplifier encompassing only unipolar (typically *p*-type only) TFTs but with both enhancement and depletion modes, relatively high gain may be achieved by having a depletion-mode transistor as the load with its source-gate terminals shorted (zero V_{GS}) and the enhancement-mode TFT as the common source amplifier, a common design approach in the late 1970s and early 1980s [96], [97]. Nevertheless, many printing processes are unable to print both depletion and enhancement-mode TFTs. If a particular mode of TFTs (either enhancement-mode-only or depletion-mode-only)

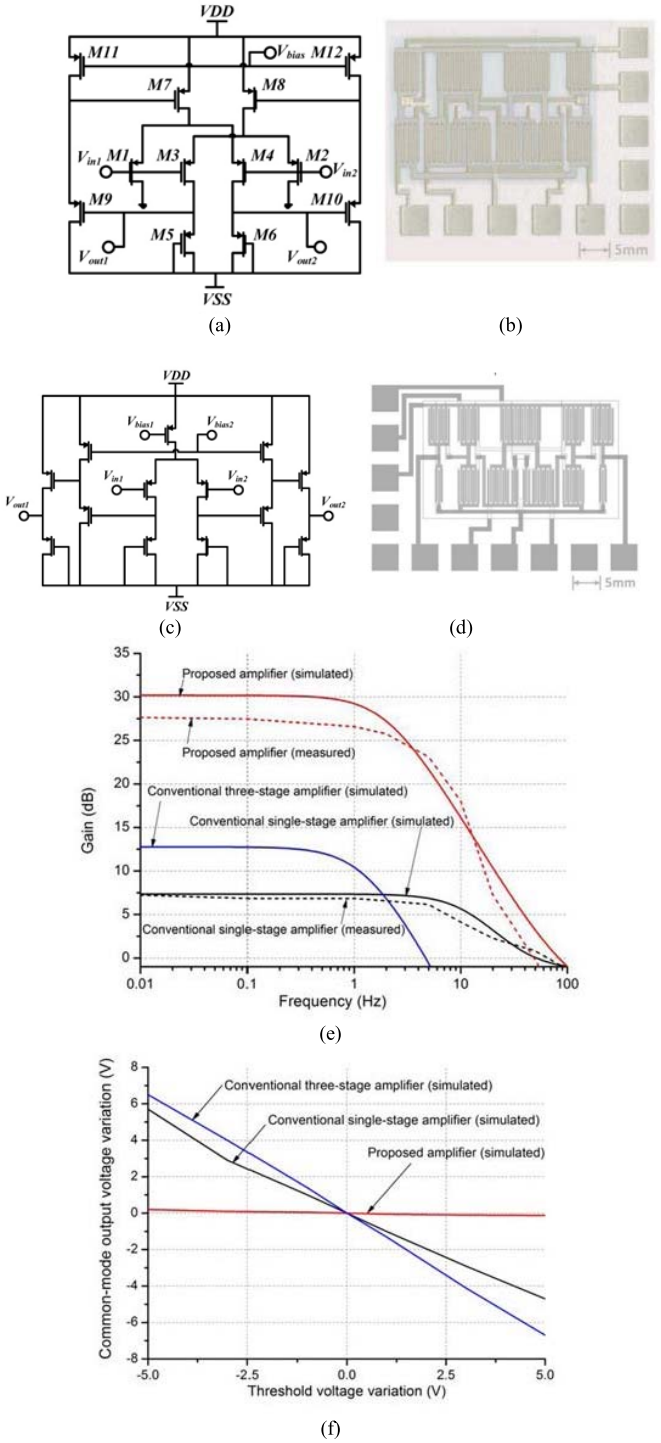


Fig. 6. (a) Differential amplifier embodying positive-cum-negative feedback, and (b) its microphotograph; (c)Conventional amplifier, and (d) its layout; (e) Frequency magnitude response, and (f) Common-mode output voltage against threshold voltage variations [14].

TFTs is available only, relatively high gain may be achieved by means of positive feedback to maintain a fixed V_{GS} [59], [98] or simply zero-V_{GS} connected transistors (transistors in the cut-off region) as the active load. Note that from a practical perspective, the employment of zero-V_{GS} connected transistors results in high amplifier sensitivity (including gain and output common-mode voltage, etc.) to process variations. This is because the impedance of zero-V_{GS} connected transistors is very sensitive to process variations. In some cases, diode-connected transistors are preferred to serve as the active load to mitigate the effects of process variations although the gain is degraded. Note that although positive feedback is very effective, this is at the cost of phase margin which may in turn result in instability. In general, positive feedback is not used silicon in linear analog designs, but is applicable in Printed Electronics with caveats.

Consider a esoteric design [14] embodying both positive-cum-negative feedback paths to simultaneously increase the gain (and gain bandwidth) and reduce the common-mode sensitivity. The schematic and microphotograph are respectively depicted in Figs. 6(a) and (b). The printing process is a Fully-Additive Air-Air Low-Temperature screen printing process. In this amplifier, the positive feedback path serves to significantly increase the gain whilst the negative feedback path reduces the output common-mode sensitivity of the amplifier. The efficacy of the positive-cum-negative feedback, this amplifier was benchmarked against the conventional amplifier (without feedback) whose schematic and layout are depicted in Figs. 6(c) and (d) respectively.

The magnitude frequency responses and the output common-mode variations of the two amplifiers are respectively depicted in Figs. 6(e) and (f). For completeness, these plots also include that of the conventional simple single-stage amplifier and all three amplifiers are based on the same printing process. The efficacy the positive-cum-negative feedback is apparent. First, from Fig. 6(e), arising from positive feedback, the gain of the positive-cum-negative amplifier is ∼27dB, and is significantly higher than that of the conventional 3-stage and single-stage amplifiers, whose gain is ∼13dB and ∼8dB respectively, yet without compromising the gain-bandwidth or incurring hardware/printed area penalty. Second, from Fig. 6(f), the application of negative feedback significantly reduces the output common-mode voltage sensitivity of the amplifier to the process variations. As a case in point, for 5V threshold voltage variation, the output common-mode variation for the positive-cum-negative feedback amplifier is a mere 0.3V vis-à-vis 6.5 and 5.6V respectively for the conventional 3-stage and single-stage amplifiers.

Consider now the challenge arising from the poor matching between two transistors due to process variations and how this can be mitigated byco-design/co-optimization between the first three constituent supply chains, Materials, Printing and Circuit Layout. There is considerable published work on various materials and their effect on variations. In one of these [28], it was shown thata Fully-Additive All-Air Low-Temperature process based on a dual-solvent TIPS-Pentacene/Polystyrene blend with careful processing reduced the variations of carrier mobility and threshold voltage from ±30% and ±1V in a TIPS-Pentacene-only process to ±4.9% and ±0.43V. From a circuit perspective, this substantially reduced the variations of the oscillation frequency of a ring oscillator from ±13.5% to ±1.9%, and the gain variations of a simple differential amplifier from ±23.6% to ±2.6%. For the matching between two transistors the variations are also reduced significantly from 48.4% to ±7.2% for the same simple layout. This already significantly improved matching can be improved with careful

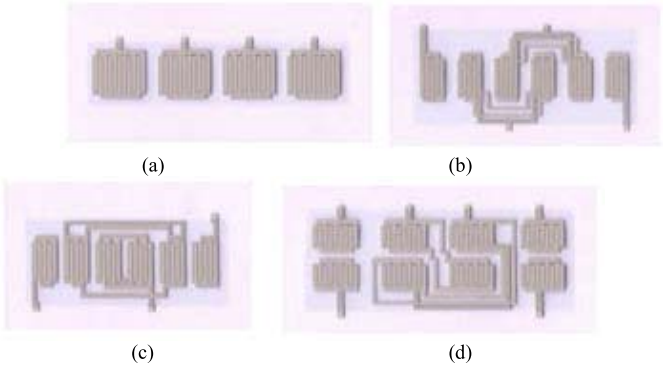


Fig. 7. Micrographs of the printed transistors: (a) Simple layout, (b) Interdigitation, (c) Common Centroid, and (d) 2D Common Centroid layout.

layout [28] – as in silicon layouts. By means of adopting more complex layouts from Simple → Interdigitation → Common Centroid → 2D Common Centroid, depicted in Figure 7, the matching between two transistors is markedly improved from 7.2% → 5.3% → 2.8% → 2.1% but with an area penalty of 0% → 53% → 36% → 65%. In short, the combined co-design/co-optimization is efficacious.

The co-design/co-optimization between the three supply chains, Materials, Printing and Circuit design may also be applied to efficaciously reduce the difficult challenge arising from variations due to bending. A reported innovative method [99] involved exploiting the fact that when a substrate is bent, the top surface and bottom surface experience opposing stresses. For example, when a substrate is bent concavely, its top surface experiences concavely-stress while the bottom surface experiences the opposing convexly-stress. To neutralize the overall bending stress, one half of a given printed element is printed on the top surface while the other half is printed on the bottom surface. An example is depicted in Figure 8 for a diode-connected inverter embodying only p-type TFTs.

Fig. 8(a) depicts the conventional design where the two transistors are printed on the top side of the substrate. When the substrate is bent either concavely or convexly, both transistors, being on the same top surface, experience the largely same stress and their variations increase – higher variations as the radius of bending reduces. Fig 8(b) depicts the reported self-compensated design [99] involving a co-optimization between printing and circuit layout. In particular, the top M_1 transistor in Fig. 8(a) is now two halves of M_1 in Fig. 8(b) where one half is printed on the top and the other printed on the bottom of the substrate. M_2 is likewise two halves. Fig. 8(c) depicts the microphotograph of the top surface of the substrate where one half of M_1 and M_2 are printed on. When the substrate is bent, one half of M_1 and M_2 will experience concave stress while the other half of M_1 and M_2 will experience the opposing convex stress, thereby largely cancelling the effect of bending. This innovative self-compensation means was shown to be highly efficacious – more than 100x reduction in variations due to bending.

B. Digital Designs: Esoteric Designs

The complete design space for digital design and their signaling protocols is depicted in Fig.9. At the highest level

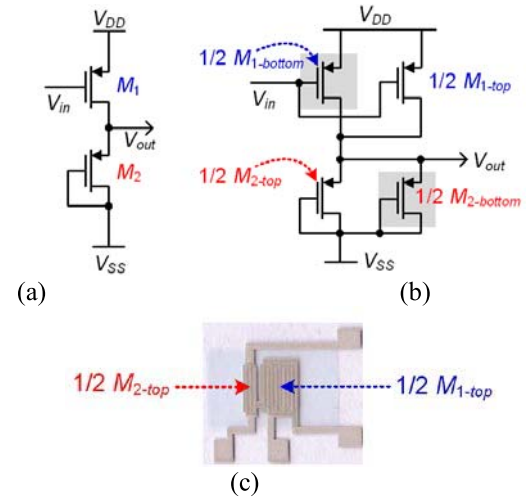


Fig. 8. Schematics of the diode-connected inverter: (a) Conventional design, (b) Design with self-compensation for bending;and (c) Micrograph of the half inverter (top surface) [99].

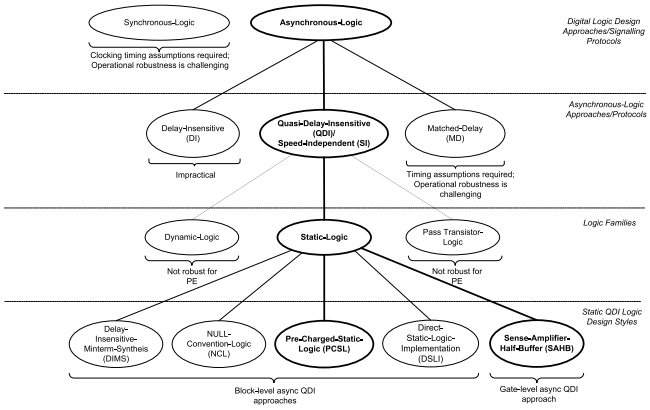
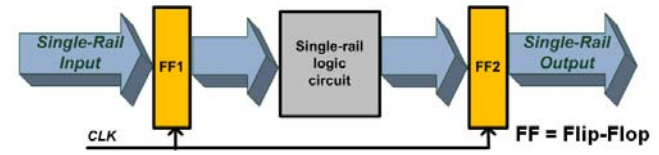


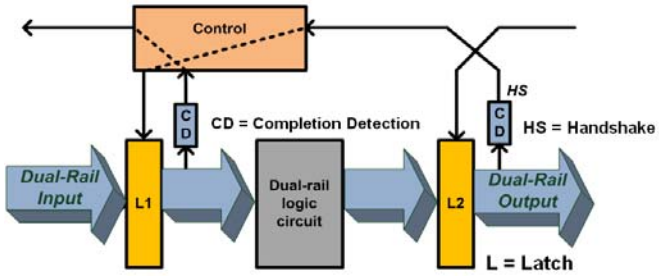
Fig. 9. Classification of digital design approaches/signaling protocols.

of design, there are two digital design philosophies [86], [93], [101], [103], i.e., digital signaling/ synchronization protocols – the near-universally practiced synchronous-logic and the esoteric asynchronous-logic (also known as 'self-timed' logic). In the perspective of contemporary and emerging digital circuit design, ITRS [100] projects that asynchronous-logic will gain increasing acceptance and this is in part to accommodate the ever-increasing PVT variations expected of emerging silicon semiconductor technologies. Interesting, because of the ever-increasing PVT variations, the clocking rate of digital circuits has largely stalled despite the higher speed offered by the increasingly advanced (smaller feature) silicon processes. Nevertheless, in the perspective of circuit design, as the variations in commercial silicon are rigorously characterized in their Process Development Kits, including all four corners of operation, it is relatively straightforward to design circuits to accommodate the variations. This is not the case in Printed Electronics where the variations are not typically rigorously quantified and possibly intractable.

The evolution in digital circuit designs towards addressing large and ever-increasing process variations certainly bodes well for both deep subthreshold designs [86], [87] in silicon and for Printed Electronics, both with large variations.



(a)



	D.T	*D.F*
No Data	'0'	'0'
Valid Data '0'	'0'	'1'
Valid Data '1'	'1'	'0'
Invalid	'1'	'1'

(b)

Fig. 10. Generic block diagram of a (a) Synchronous-logic stage, and an (b) Asynchronous Quasi-Delay-Insensitive stage and Table of Dual-Rail Logic.

In Fig.9, it has been argued [87], [93], [102]–[105] that the approaches/protocols in bold can accommodate severe and intractable variations,but there are tradeoff in terms of hardware, power dissipation and IC area.

In Fig. 9, at the highest level of design, the ubiquitous near-universally practiced synchronous-logic protocols are largely inappropriate for Printed Electronics. We will now explain this on the basis of design philosophies and their idiosyncrasies, by means of the generic block diagram of the synchronous-logic stage, particularly the modality of its data synchronization, depicted in Fig. 10(a). We will thereafter describe its asynchronous-logic counterpart in Figure 10(b).

Fig. 10(a) depicts the synchronous-logic protocol embodying the *single-rail* logic circuit for data computation, and flip-flops ('FF1' and 'FF2') for data registration where the FFs are controlled/timed by a global clock signal ('*CLK*'). Single-rail is a logic representation of a binary data bit involving a single wire (and ground reference) with its associated low and high voltage levels being typically logic '0' (also data '0') and logic '1' (also data '1') respectively. In other words, as the logic levels represent valid data, the computation delay of a single-rail logic circuit (i.e., the delay to produce a valid data) cannot be derived from its output, thereby requiring its data synchronization to be performed independently with an assumption of the computation delay. Consequently, for error-free operation, the data synchronization period of *CLK* needs to be set longer than the worst-case computation delay of the single-rail logic circuit therein. Further, this worst-case delay (hence the safety margin) has to be ascertained/assumed for the entire digital circuit/system (encompassing all its constituent stages) and under all specified operating conditions – i.e., the global (the entire circuits/system under the same clock) worst-case timing.

Simply stated, synchronous-logic [87], [93], [102]–[105] assumes that the worst-case delay is known and the delays of all modules therein are set to the worst of the worst-case - the ***slowest of the worst-case.*** As delineated earlier, as silicon is rigorously characterized, these delays can be likewise rigorously ascertained and to guarantee error-free operation, some delay margins, usually conservative, are allowed for. As the large variations of Printed Electronics are not rigorously characterized and possibly intractable, the delays cannot be rigorously ascertained. This would hence lead to the possibility of erroneous operation. The most direct way of reducing the probability of erroneous operation to increase the delay margin. This however subsequently leads to the already slow operation to even slower operation, yet error-free operation is not guaranteed.

Consider now the asynchronous-logic stage depicted in Fig. 10(b), more specifically that embodying the Quasi-Delay-Insensitive (QDI) protocol. In Fig. 9, this is the second level approaches of the complete digital design space. For logic style, the static-logic logic family is necessary for robustness. Finally, of the logic design styles, there are five possible design styles to realize QDI. The Pre-Charged Static Logic [102], [87] and the Sense-Amplifier Half Buffer [103], [104] design styles was shown to be able to accommodate the very high variations in silicon digital systems operating in deep subthreshold (∼150mV). Interesting, the application of asynchronous-logic to realize a 32k-transistor 'printed' microprocessor was reported over a decade ago [49].

There are several salient differences between the synchronous- and asynchronous-logic design philosophies. The first is the replacement of the *global* clock signal ('*CLK*') of the former with a *local* handshake signal of the latter ('HS'). Particularly, for data registration, the FFs in the synchronous-logic protocol timed by a global clock (to the slowest of the worst-case for the worst-case conditions) are replaced by latches 'timed' by a local handshake signal ('L1' and 'L2' that are self-timed according to the prevailing conditions – the delay is not assumed), hence potentially substantially faster.

Another salient difference is the embodiment of a multi-rail logic circuit, typically dual-rail logic depicted and tabulated in Fig. 10(b), for data computation. Dual-rail refers to a logic representation where a binary data bit involves two wires (Data True ('*D.T*') and Data False ('*D.F*'); and a reference) with their associated voltage levels. In this fashion, data validity (and conversely its absence) is innately encoded therein. By means of a completion detection circuit ('CD'), the computation delay of a dual-rail logic circuit is physically ascertained under the prevailing conditions – including under any variations, i.e., there is no assumption on the variations. As data synchronization is subsequently performed following the completion detection by the local handshake signal ('*HS*'), no delay safety margin is thus required. In other words, the accommodation of computation delay is idiosyncratic of the QDI handshake protocol. Hence, the ensuing error-free operation is unconditional (save the isochronic fork timing [105], [106] which is easily satisfied).

In short, from a robustness point of view, the asynchronous-logic QDI circuit/system lends itself naturally to Printed Electronics (and deep subthreshold operation in silicon) whose variations are very large/intractable because it innately adapts to the prevailing conditions. Another advantage is that because it is 'self-timed', it operates as fast as possible to said conditions. This potentially leads to substantially faster operation (and potentially lower power/energy) than the conventional synchronous-logic which must be timed to the slowest worst-case delay under the worst-case conditions (plus some timing margin).

The advantages of asynchronous-logic nevertheless come at a cost – hardware overheads in terms of transistor count (and power for the same operating condition without any margins [87], [104]). This overhead arises from its dual-rail data encoding and completion detection, and a1.5x-2x hardware overhead is not uncommon. These overheads can nevertheless be mitigated by clever designs, including the reported Pre-Charged-Static-Logic (PCSL) [87], [102] and the Sense-Amplifier-Half-Buffer (SAHB) [103], [106] for implementing QDI circuits respectively at the block level and the gate level.Both the PCSL and SAHB were shown to be $>$5x better than the more established DIMS, NCL and DSLI in Fig.9.To further reduce the overheads, the reported 'Pseudo-QDI' protocol [106] was shown to be able to reduce hardware associated with completion detection. In one example, this reduced the overall hardware by 1.34x.

In summary, contemporary circuit design methodologies for silicon (whose process variations are rigorous quantified) are largely inapplicable for Printed Electronics (whose process variations are not rigorously quantified, possibly intractable). This includes the contemporary negative feedback and the synchronous-logic design philosophy respectively in analog and digital designs. Circuit designs beyond contemporary methodologies, with co-design and co-optimization between the different constituent supply chains would be necessary to address thechallenges posed by Printed Electronics – presenting tremendous opportunities for the Circuits and Systems and Solid-State communities.

VI. Conclusions

This review has provided a comprehensive and critical overview of Printed Electronics with emphasis from a circuits and systems perspective. The often touted attractive attributes of Printed/Organic Electronics present many formidable, mostly unresolved, challenges in all constituent supply chains of the entire supply chain of Printed Electronics. Our tabulation and review of state-of-the art printed analog, mixed-signal, and digital circuits depicted that they are largely rudimentary, and consequently, the degree of intelligence of Printed Electronics at this juncture modest. Given the substantially superior silicon transistor performance, it was argued that Printed Electronics circuits be used strategically and advantageously where a silicon solution would be inappropriate or inapplicable. Our review of printed circuits was also viewed in the perspective of the application space of Printed Electronics and its entire supply chain. The challenges in each constituent chain thereof were delineated in the perspective of circuit and systems, and these challenges were shown to be indeed formidable. Contemporary circuit design philosophies for analog and digital silicon circuits were shown to be often inadequate, arguing the real need for novel and possibly esoteric design methodologies and the co-design and co-optimization between circuit design and the other constituents of the supply chain. These challenges present tremendous and exciting opportunities for the Circuits and Systems and Solid-State communities for realizing intelligent Printed/Organic Electronics products for the 'Fourth Industrial Revolution'.

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