Power Consumption of Integrated Low-Power Receivers

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***Abstract*—With the advent of Internet of Things (IoT) it has become clear that radio-frequency (RF) designers have to be aware of power constraints, e.g., in the design of simplistic ultra-low power receivers often used as wake-up radios (WuRs). The objective of this work, one of the first systematic studies of power bounds for RF-systems, is to provide an overview and intuitive feel for how power consumption and sensitivity relates for low-power receivers. This was done by setting up basic circuit schematics for different radio receiver architectures to find analytical expressions for their output signal-to-noise ratio including power consumption, bandwidth, sensitivity, and carrier frequency. The analytical expressions and optimizations of the circuits give us relations between dc-energy-per-bit and receiver sensitivity, which can be compared to recent published low-power receivers. The parameter set used in the analysis is meant to reflect typical values for an integrated 90 nm complementary metal–oxide–semiconductor fabrication processes, and typical small sized RF lumped components.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), Internet of things (IoT), low noise, low-power, receiver, wake-up radio (WuR).**

I. Introduction

POWER has for a long time been the dominant design constraint for digital electronics. Among the motives we find the need to reduce cost for cooling, cost for power, and prolonged time between charge of mobile devices. In analog electronic design, and especially radio-frequency (RF) electronic design, the drive to reduce power has not been the same. Traditional RF electronic design has been more about getting better performance from devices. However, along with the development of personal mobile communication also RF designers have become increasingly aware of the power issue. RF electronics have gradually become more integrated on ASIC together with the digital electronics. Thus, being subject to the same fabrication processes, mainly complementary metal–oxide–semiconductor (CMOS), and to the same scaling rules. With the ongoing realization of the vision of Internet of Things (IoT) it has become even more obvious that RF designers have to be aware of power constraints [1].

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Besides physical blocks and devices, a radio system consists of a medium access (MAC) protocol controlling and scheduling the communication. Here, duty cycling is a simple way to reduce average power consumption of the receiver, but at the cost of added latency and a requirement of good synchronization. Another approach to reduce power consumption is to minimize functionality during idle periods; meaning that high data rates are transferred with more power hungry devices using complex modulation, while simplistic ultra-low power receivers function as wake-up radios (WuR) during the idle time.

Sensors within the IoT have to survive on a single battery during their projected lifetime, or they must live on available harvested energy in their surroundings [2]. It would be virtually impossible to change batteries on each device in the considered swarm of connected items. For the most slimmed down sensors, a WuR or similar simplistic radio would function as the solitary link provider.

The designer of modern RF receivers needs to be aware of requirements driving power consumption, namely baseband bandwidth, sensitivity, and also carrier frequency and interference [3]. The motivation of this work, one of the first systematic studies of power bounds for RF-systems, is to provide an overview of the first two of these mentioned requirements (baseband bandwidth and sensitivity) and to provide an intuitive picture of their relations to power consumption. Different receiver architectures are compared and their technical challenges are discussed. The set of available low-power receiver architectures is rather limited. We will here handle the tuned RF receiver (TRF), with and without a preceding low noise amplifier (LNA), and the superheterodyne receiver. The regenerative and super-regenerative receiver are also used for low-power applications, but will not be treated analytically, although being part of our survey. (There are no evidence they should be exceptionally better performing than the mentioned receivers.) The circuits being treated here are basic, and certainly other power saving schemes may be added on top, such as current reusing stacks like the LMV-cell (LNA-mixer-VCO) [4] or AMF-cell (amplifier-mixer-filter) [5], or methods for duty-cycling [6].

In a survey of recent published low-power receivers (see Fig. 1) the consumed dc-energy to receive one bit, the energy-per-bit measure, is plotted versus the radio sensitivity. The sensitivity is defined as the RF power needed to reach a raw bit error rate (BER), before redundant coding and error corrections, of $\mathrm{BER} = 10^{-3}$. In Fig. 1, a lower bound for the attainable energy consumption per received bit is discernible. One of our objectives is to find the fundamental reason for this energy-per-bit bound by studying basic receiver circuits.

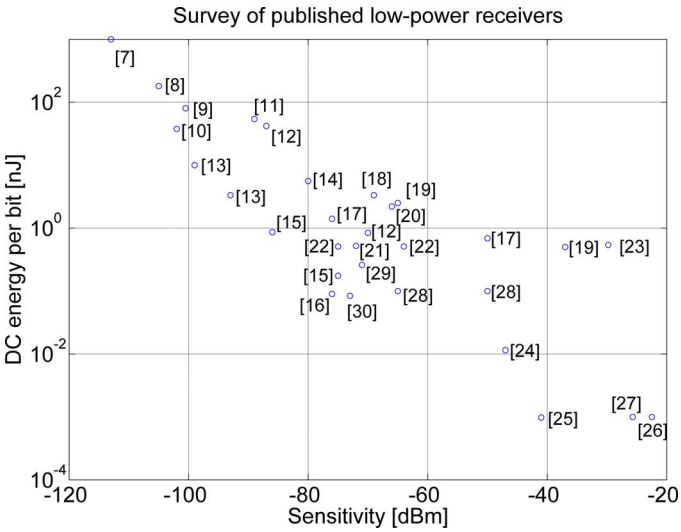

Fig. 1. Survey of recent published low-power receivers. References in graph [7]–[30].

We will describe the parameter set used in Section II and the TRF in Section III. In Section IV, we extend the study to superheterodyne receivers. We then finish with a discussion in Section V and a conclusion in Section VI.

II. Description of Parameter Set and Analysis

In this paper, we take on a different analysis approach; we set up circuit schematics for different receivers to find analytical expressions for their output signal-to-noise ratio (SNR). The minimum output SNR for reliable detection is assumed to be 12 dB [21], and we assume ASK is being used. We may here note that the receivers compiled in the survey use either on–off keying (OOK), impulse-radio UWB-pulse position modulation (IR-UWB-PPM), or frequency shift keying (FSK). The OOK and IR-UWB-PPM modulation techniques are both special cases of ASK. While FSK and ASK theoretically present the same bit error rate for a given SNR, the different demodulator implementations may differ in their response.

The component values, or the parameter set, we use in the following analysis is meant to reflect typical values for integrated CMOS fabrication processes, and typical small sized RF lumped components. Normally the number of discrete components is a strong driver of cost, so we look for single chip solutions with a minimum number of external components.

We have chosen 90 nm CMOS as reference technology, using the same basic parameters as used in [31] (minimum capacitance $C_{\min} = 1$ fF and effective voltage $V_0 = 75$ mV). It is worth to point out that the choice of fabrication process has a limited influence on analog design, with the minimum capacitance $C_{\min}$ being the most important parameter [31].

On-chip inductors rarely reach higher inductance value than 10 nH or a better Q than 5 [32]. Available external inductors display a Q of around 35 if they simultaneously must have a serial resonance above the carrier frequency we here look into. Further, the loading capacitance of an ASIC bond pad end up at around 400 fF when ESD protection is included. However, here we assume that we may reduce the load to 75 fF, reflecting the ongoing development of RF ESD clamps [33].

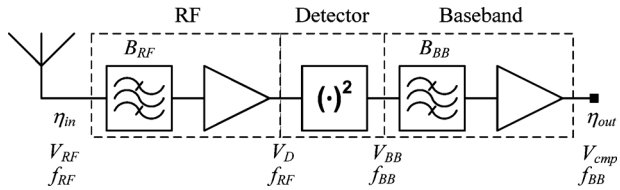

Fig. 2. Tuned RF receiver. SNR is symbolized with η.

We assume the baseband noise bandwidth B_{BB} to be twice the bit rate of the receiver (i.e., a bit rate of 250 kb/s requires a baseband bandwidth of $B_{BB} = 500$ kHz). Furthermore, we assume temperature to be $T = 300$ K. Finally, we use a supply voltage of 1 V (supply voltage may be as low as 0.5 V, but it will not change the conclusions in this paper as long as stacking of circuit blocks for current reuse is not considered).

III. Tuned RF Receiver

A block schematic of a TRF is found in Fig. 2. In the TRF the received signal is band-pass filtered (B_{RF}) around the intended carrier frequency f_{RF} to reduce impact from out of band interfering signals. The RF-filter of a WuR usually is broadband, to make it robust against process variations and to add a minimum of loss. The antenna itself is likely to be resonant and may for some applications provide sufficient selectivity. Electrically small size antennas have a narrow bandwidth and a more isotropic radiation pattern, which is desirable in many WuR applications. However, these properties come together with a reduced antenna efficiency. Some reported envelope detector based low-power receivers use off-chip SAW or BAW filters for improved selectivity [9], [10], [18], [19], [29]. The inclusion of an RF pre-amplifier is optional, and depends on the targeted receiver sensitivity. Amplification of the signal before detection increase sensitivity, but has a substantial impact on the power budget since RF gain is expensive from our power perspective.

The detector converts the modulated RF signal to a baseband signal, and here we assume that ASK modulation is being used. The conversion gain from peak RF input voltage amplitude V_D to output dc voltage V_{BB} of the detector is

$$G_D = \frac{V_{BB}}{V_D} = \frac{V_D}{4V_0} \tag{1}$$

where V_0 is the effective voltage found in [3] and [31]. Unwanted harmonics produced by detector nonlinearities are filtered out by a baseband filter with bandwidth B_{BB}. Finally, before digitization, the signal is amplified in a baseband amplifier stage. The signal digitizer can be composed of a comparator and an averaging filter as reported in [27].

A. Low-Power Envelope Detector With Baseband Amplifier

The most basic implementation of the TRF is an envelope detector followed by a baseband amplifier (see Fig. 3). Basically this is an integrated version of the vintage crystal radio, where the incoming radio signal voltage V_D drives a detector transistor M2 instead of a crystal diode. The outgoing detector current i_s is filtered by a detector capacitor C_d before being amplified

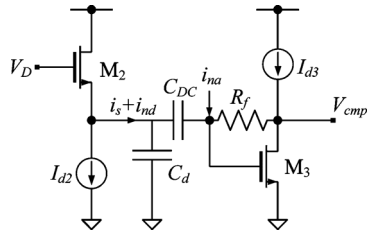

Fig. 3. RF-detector and transimpedance amplifier (TIA).

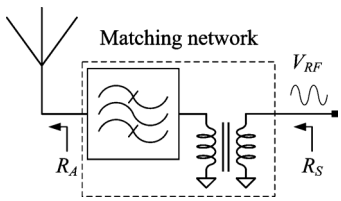

Fig. 4. RF-transformer with input impedance R_A and output impedance R_S and passive voltage gain $G_T = \sqrt{R_S/R_A}$. Transformer also work as a matching network and a filter.

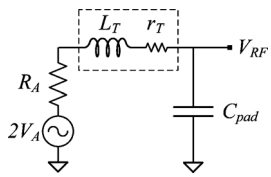

Fig. 5. RF-transformer with external inductor in series with chip RF input port.

in a transimpedance amplifier consisting of transistor M3 and feedback resistor R_f. Capacitor C_d also acts as a low impedance path to ground for the radio signal. The outgoing voltage V_{cmp} is digitized in a comparator, or by an ADC. Bias currents for the transistors are I_{d2} and I_{d3}.

With an up-transforming network between the antenna and the detector the sensitivity can be improved. A passive up-transformer works by trading current amplitude for voltage amplitude and thus increase a low antenna impedance (compared to the detector input impedance), R_A, to a higher value, R_S (see Fig. 4). With a sufficiently small detector transistor the input impedance is high with a low capacitance, so the MOS gate input will not limit the achievable transformation ratio, but rather will the losses in the transformer circuitry. This is illustrated with the straightforward impedance transformer circuit consisting of an external inductor in series with the chip RF input port (see Fig. 5). The external inductor with inductance L_T has a finite Q represented by a series resistance r_T. Matching is achieved at resonance if we choose r_T to be equal to antenna resistance R_A. The voltage at the chip input is $V_{RF} = QV_A$, and the passive voltage gain becomes $G_T = Q$. With an RF port pad capacitance $C_{\rm pad} = 75$ fF and a target resonance frequency of 2.5 GHz the inductance L_T becomes 54 nH. Now, with an antenna impedance of 50 Ω the inductor Q equates to a number roughly half the assumed achievable value of 35 in our parameter set. However, this mismatch is readily solved by reducing antenna impedance by a factor of two since small sized antennas in any case are known to have a low radiation resistance [34], thus leading to antenna impedance $R_A = 25\ \Omega$ and a Q of 35.

For high carrier frequencies a transmission-line transformer is a feasible alternative to a lumped transformer, with the advantage of adding no external components. Here microwave substrate materials offer low dielectric loss and a low spread in material parameter values. An example of a wake-up receiver built according to the principle of passive transformation on a low cost FR4 substrate is found in [24].

If V_{RF} is the voltage output from the transformer at perfect match we have $V_D = V_{RF}$.

Output SNR for the receiver in Fig. 3 can be expressed as

$$\eta_{\rm out} = \frac{i_s^2}{i_{nd}^2 + i_{na}^2} \tag{2}$$

with the signal current from the detector being[3]

$$i_s = I_{d2}\frac{V_D^2}{4V_0^2}. \tag{3}$$

The noise current from the detector output originating from M2 channel conductance g_{m2} is

$$i_{nd}^2 = 4\gamma kTB_{BB}g_{m2} \tag{4}$$

and the equivalent input noise current from the baseband amplifier is [31]

$$i_{na}^2 = \frac{16\pi^2\gamma kTC_d^2B_{BB}^3}{3g_{m3}} \tag{5}$$

with γ being the transistor noise parameter and k being the Boltzmann constant. Inserting (3), (4), and (5) into (2) we get an expression for SNR including transistor transconductances g_{m2} and g_{m3}. Combining this result with the following relation between transconductance and bias current I_d

$$g_m = \frac{I_d}{V_0} \tag{6}$$

we obtain the following for outgoing SNR:

$$\eta_{\rm out} = \frac{\left(\frac{I_{d2}V_D^2}{(4V_0^2)}\right)^2}{\frac{4\gamma kTB_{BB}I_{d2}}{V_0} + \frac{16\pi^2kT\gamma C_d^2B_{BB}^3}{\frac{3I_{d3}}{V_0}}}. \tag{7}$$

The transistor noise parameter γ is henceforth approximated with $\gamma = 1$, for better readability of expressions.

The optimum distribution of the two bias currents I_{d2} and I_{d3} in this receiver depends on targeted sensitivity, and the relation may be better perceived if we instead look at the inverse of (7)

$$\frac{1}{\eta_{\rm out}} = \frac{64kTB_{BB}V_0^4}{V_D^4}\left(\frac{1}{I_{d2}V_0} + \frac{4\pi^2C_d^2B_{BB}^2V_0}{3I_{d3}I_{d2}^2}\right). \tag{8}$$

Here, we have two terms that are being functions of the bias currents, dominating the SNR calculation within different intervals of sensitivity. The goal for a designer is to find a distribution of bias currents with minimum total current, $I_{\rm tot} = I_{d2} + I_{d3}$, while still passing the SNR threshold resulting in a BER $= 10^{-3}$. If we look at the two terms in (8) isolated

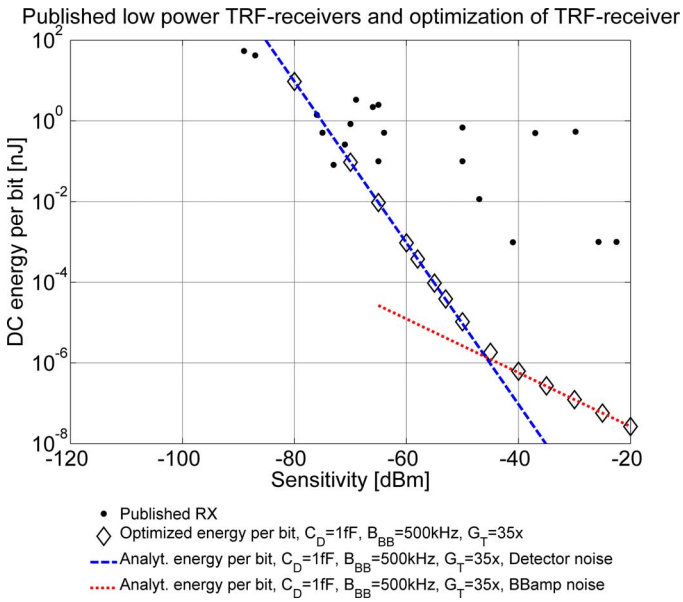

Fig. 6. Baseband amplifier and detector dominate the power budget at different sensitivity intervals. Blue dashed line is analytically calculated energy-per-bit performance considering detector noise only, while red dotted line is analytically calculated energy-per-bit performance considering baseband amplifier noise only. Black diamonds are optimized performance considering both detector and baseband amplifier noise. TRF receiver data from Fig. 1 is plotted for comparison. Curves are calculated with (8) using $C_d = 1$ fF and are independent of baseband bandwidth B_{BB}. Available RF power (sensitivity) is calculated from peak RF voltage using the series transformer in Fig. 5 with $Q = 35$, and an antenna impedance $R_A = 25\ \Omega$.

one at a time, the expected behavior of an overall optimization may be foreseen. The first term of (8), dominates the power budget for higher sensitivities, and is plotted as energy-per-bit in Fig. 6 with the total bias current going through the detector ($I_{d2} = I_{\rm tot}$). The RF sensitivity in Fig. 6 is calculated with $G_T = 35$ and $R_A = 25\ \Omega$. The second term of (8) dominates the power budget at low sensitivities, and it can be showed that this term is minimized when $I_{d3} = I_{\rm tot}/3$. In Fig. 6 the second term is plotted as energy-per-bit with this optimized current distribution.

The overall power optimization of the receiver is graphically presented in Fig. 6. The optimized curve makes a smooth transition between the two sensitivity intervals. The energy-per-bit performance for this receiver circuit is independent of baseband bandwidth. When the first term in (8) dominate SNR, $\eta_{\rm out}$ is proportional to $I_{\rm tot}/B_{BB}$ (energy-per-bit). With the second term dominating $\eta_{\rm out}$ is proportional to $I_{\rm tot}^3/B_{BB}^3$ (the cube of energy-per-bit).

B. TRF With Fully Integrated LNA

Both output voltage and output current from the envelope detector in Fig. 3 are approximately proportional to the square of the input signal voltage. It is clear that boosting V_{RF} with a pre-amplifier, beyond what is possible with a passive impedance transformer, would improve the receiver sensitivity drastically. However, it is not obvious at what level of sensitivity the pre-amplifier pays off in our power budget.

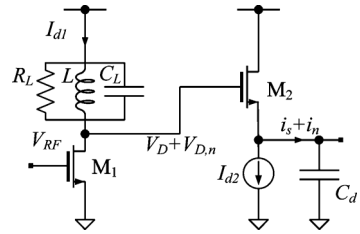

Fig. 7. RF-detector and LNA with amplification G_{RF}.

The pre-amplifier is often referred to as a LNA, and low levels of noise are costly to achieve. Thus, we must carefully consider what level of noise being acceptable.

1) Resonant Load: In Fig. 7 a TRF with LNA is depicted. The baseband amplifier is skipped as it does not affect the power-noise relation for higher sensitivities. By analyzing the circuit we may find out if it is relevant or not to use a pre-amplifier from a power budget perspective. The choice is "hard" in the sense that we have to choose between two configurations; the LNA will not become transparent as we reduce its supply current, rather it will eventually attenuate the signal and ruin our receiver performance.

The LNA has a resonant load providing narrow band amplification at carrier angular frequency $\omega_{RF} = 2\pi f_{RF}$, and thus it also offer some RF filtering. The expression for the RF gain with a resonant load having quality factor Q_L is

$$G_{RF} = g_{m1}R_L = \frac{g_{m1}Q_L}{\omega_{RF}C_{L1}} \tag{9}$$

where g_{m1} is the transconductance, R_L is the load impedance, and C_{L1} is the capacitive load from subsequent stages and eventual tuning capacitors.

Referring to Fig. 7 we set up an expression for output SNR of the complete TRF receiver with the LNA included

$$\eta_{\rm out} = \frac{i_s^2}{i_n^2} = \frac{i_s^2}{i_{nd}^2 + i_{nc}^2} \tag{10}$$

where i_s is the signal current, i_{nd} is the detector transistor M2 channel noise, and i_{nc} is converted RF noise from preceding stages.

From (1), (3), and (6) we construct a converting transconductance for the detector of $g_D = g_{m2}G_D = (I_{d2}V_D)/(4V_0^2)$. Now, with the detector voltage $V_D = G_{RF}V_{RF}$ appearing over the detector input, the signal current becomes

$$i_s = V_D g_D \tag{11}$$

while the converted noise from the LNA is

$$i_{nc}^2 = 8V_{D,n}^2 g_D^2 \tag{12}$$

with $V_{D,n}^2 = 4kTB_{BB}g_{m1}R_L^2$ (see Appendix A).

The channel noise from detector transistor M2 is given by (4), and with that we arrive at a final expression for output SNR

$$\eta_{\rm out} = \frac{V_D^2 g_D^2}{4kTB_{BB}g_{m2} + 8V_{D,n}^2 g_D^2}. \tag{13}$$

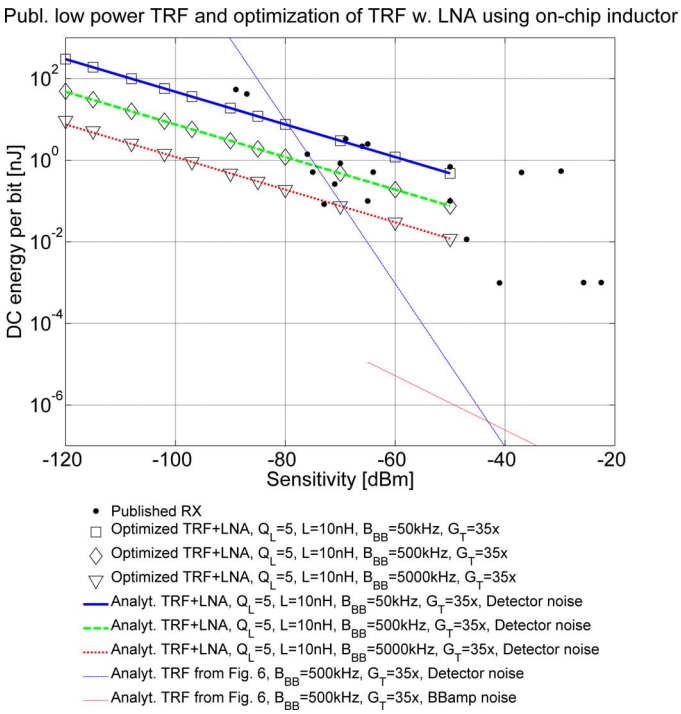

Fig. 8. For higher sensitivities it is beneficial to introduce an LNA. Blue solid, green dashed, and red dotted lines are analytically calculated energy-per-bit performance for LNA with detector at bandwidths $B_{BB} = 50$ kHz, $B_{BB} = 500$ kHz, and $B_{BB} = 5000$ kHz, respectively, considering detector noise. Black square, diamond, and triangle are optimized performance considering both LNA and detector noise for bandwidths $B_{BB} = 50$ kHz, $B_{BB} = 500$ kHz, and $B_{BB} = 5000$ kHz, respectively. Analytically calculated curves from Fig. 6 and TRF receiver data from Fig. 1 are plotted for comparison. These curves were attained with (14) using $L = 10$ nH and $Q_L = 5$ and the same transformer setup as for Fig. 6. Curves are bandwidth dependent, a k times wider baseband bandwidth B_{BB} needs to be compensated with only $k^{1/5}$ larger total bias current, thus the energy-per-bit is actually reduced with a factor $k^{4/5}$.

Using (6) we again get an expression for the inverse of the outgoing receiver SNR as a function of biasing currents

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}}{V_{RF}^2}\left(2\frac{V_0^7(\omega_{RF}C_{L1})^4}{I_{d2}I_{d1}^4V_{RF}^2Q_L^4} + \frac{V_0}{I_{d1}}\right). \quad (14)$$

We identify two different terms dominating the power budget at different sensitivity intervals. With typical on-chip low Q inductors and for reasonable sensitivities the first term, representing detector noise, will dominate over the second term, representing converted noise from the LNA transistor M1. We will get back to the second term in Section III-C where we look into higher Q values available with external inductors.

It can be shown that the bias current distribution that minimize the first term is $I_{d1} = 4/5I_{\text{tot}}$, where $I_{\text{tot}} = I_{d1} + I_{d2}$. In Fig. 8, the energy-per-bit slope with this current distribution is plotted on top of the curves from Fig. 6 for comparison. The result depend on baseband bandwidth in this case, where three different bandwidths have been plotted, B_{BB} =50, 500, and 5000 kHz, respectively. The improvement with an LNA is significant for higher sensitivities, while at lower sensitivities the LNA becomes superfluous. The sensitivity level where the pre-amplifier pays off depends on targeted bandwidth (i.e., bit rate).

At higher sensitivity levels it is noted that we have to take antenna noise into account in our calculations. The antenna noise temperature depends on loss mechanisms and on the brightness of the objects being covered by the antenna beam. We assume an indoor environment with room temperature objects all around (no cold sky), resulting in an antenna source temperature of $T_A = 300$ K. In our SNR calculation the source temperature, multiplied with baseband bandwidth B_{BB}, impose a fundamental limit for the sensitivity. Antenna noise is included by modifying (14) with the addition of a term R_S within brackets

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}}{V_{RF}^2}\left(2\frac{V_0^7(\omega_{RF}C_{L1})^4}{I_{d2}I_{d1}^4V_{RF}^2Q_L^4} + \frac{V_0}{I_{d1}} + R_S\right). \quad (15)$$

The maximum achievable sensitivity with antenna noise included is -92.8 dBm at a baseband bandwidth of $B_{BB} = 500$ kHz.

2) Resistive Load: With a resonant load the amplifier performance is limited by the inductance and the Q-value that is possible to achieve with on-chip inductors. The achievable inductance value also imposes a lower limit on the capacitive load if resonance should be attained. If we instead look at a pure resistive load the capacitance can be minimized $C_{L1} = C_{\min}$. We can now easily modify (14) with Q set to unity

$$G_{RF} = g_{m1}R_L = \frac{g_{m1}}{\omega_{RF}C_{L1}} \quad (16)$$

where we have used the bandwidth requirement $R_L = 1/(\omega_{RF}C_{L1})$ limiting the load resistor size [31]. We get

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}}{V_{RF}^2}\left(2\frac{V_0^7(\omega_{RF}C_{\min})^4}{I_{d2}I_{d1}^4V_{RF}^2} + \frac{V_0}{I_{d1}}\right). \quad (17)$$

The result with a resistive load is plotted in Fig. 9. A possible concern when using a resistive load is the voltage headroom. This problem may be managed by shunting the bias current through a PMOS current generator in parallel with the load resistor. The resistive load may be a resistor or a NMOS transistor.

C. TRF With Integrated LNA Using External Inductance

The parameter values used in Section III-B and for Fig. 8 corresponded to a typical integrated LNA. If we have the opportunity to place the inductance of the resonant LNA outside the chip, some advantages can be noted. First, we may increase the inductance value, giving higher load impedance. Second, the Q of an external inductor is normally better due to larger size and a better isolation from lossy substrate material. However, we also note some complications with this procedure. The typical bond pad parasitic capacitance limits the size of applicable inductors (since resonance frequency of the amplifier load is $\omega_0 = 1/\sqrt{LC}$). Further, the process of bonding and contacting external components complicates the implementation and make it technically challenging. It drives cost and introduces a number of new parameters that has to be controlled to reduce spread. Examples of such parameters are the dielectric constant of PCB substrate, transmission line dimensions, and bond wire lengths. To be able to assess the use of internal and external inductors

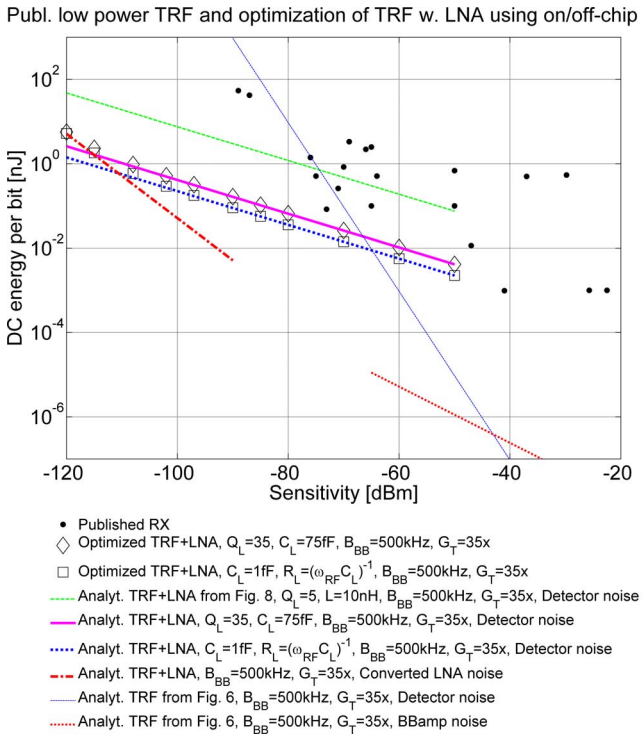

Fig. 9. Comparing LNAs with various types of loads. Analytically calculated results considering detector noise only are: blue dotted line for resistive load with minimum $C_L = 1$ fF, green dashed line for on-chip inductance $L = 10$ nH $Q_L = 5$, and magenta solid line for off-chip inductance with $Q_L = 35$ in resonance with on-chip ESD capacitive load. Red doted–dashed line is analytically calculated result considering converted LNA noise only. Black squares and diamonds are optimized performance considering both LNA and detector noise, using resistive load with minimum $C_L = 1$ fF, and using off-chip inductance with $Q_L = 35$, respectively. Analytically calculated curves from Fig. 6 and TRF receiver data from Fig. 1 are plotted for comparison. LNA with resistive on-chip load has a better energy-per-bit performance than its inductive on-chip counterpart. External high Q inductors bonded to the chip may improve the power budget. However, in this plot we see that the improvement is impaired by the parasitic capacitive loading from the bonding pad, and that the on-chip resistive load is a better choice. Curves were attained using (14) and (17), without noise from the source resistance R_S using $B_{BB} = 500$ kHz and same transformer setup as in Fig. 6. Energy-per-bit has the same slope for all three types of load, except for the highest sensitivities where the second term in (14) and (17), converted LNA noise (by detector), becomes evident. Including noise from R_S, i.e., antenna noise, leads to a sensitivity limit of -92.8 dBm ($B_{BB} = 500$ kHz).

in the LNA we have in Fig. 9 plotted analytical curves for amplifiers using $Q = 35$ on top of the previous attained analytical results with internal inductance and with resistive load. The overall power consumption is reduced with higher Q, and the LNA continues to contribute down to lower sensitivities. However, we also see that an external inductance cannot compete with an on-chip resistive load.

In Fig. 9 we see the second term in (14) become visible for higher sensitivities. This term represents noise from the LNA transistor being converted by the detector, and it is noted that its energy-per-bit slope is bandwidth independent. However, its relevance is limited since it is normally screened by antenna noise. It is here relevant to also mention active inductors as an alternative to passive inductors [32]. The voltage gain of an LNA with an active inductor with transconductance g_m and a capacitive load C_L, can be shown to be $A_V = (g_m/(\omega C_L))^2$. If we look for a gain of say $A_V = 10$, this corresponds to a transconductance of 50 μS with the minimum capacitance $C_L = C_{\min}$ at the frequency 2.5 GHz. A resistive load requires a $\sqrt{A_V} = \sqrt{10}$ times larger conductance under the same conditions, equating to 157 μS. Taking into account the added noise associated with active inductors the net improvement is rather small.

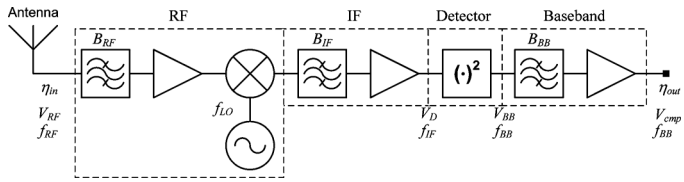

Fig. 10. Superheterodyne receiver (SHET).

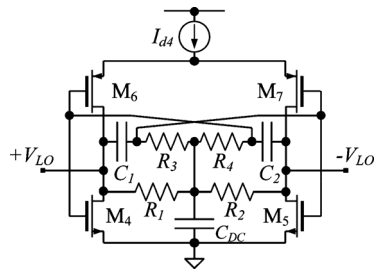

Fig. 11. *RC*-oscillator.

IV. Superheterodyne Receiver

One of the most widely used radio receiver architectures is the superheterodyne, depicted in Fig. 10. It differs from the TRF by a down-converting stage that reduces signal frequency before the actual detection take place. Among the primacies of the superheterodyne we find a high sensitivity and a well controlled channel filtering. Further, amplification at the intermediate frequency (IF) requires less dc-power compared to amplification at RF. On the other hand, the down-converting mixer stage needs to be driven by a local oscillator (LO) constantly draining the power supply. The superheterodyne receiver may be tuned to different RF channels by changing the LO frequency. A negative consequence of this tuning ability is that the superheterodyne is sensitive to LO frequency instabilities, but this problem can be mitigated by using a more tolerant IF-stage design such as the uncertain-IF receiver [21]. In this paper we look at a simplistic incarnation of the superheterodyne using a single down conversion stage, in opposition to high performance dual conversion implementations [35].

We have studied oscillator realizations using *RC*-tank circuit and *LC*-tank circuit (see Figs. 11 and 12). The *RC*-oscillator has the advantage over the *LC*-oscillator of being easier to integrate on chip, since it has no large inductor consuming expensive silicon area. One major drawback is that the lossy *RC*-network implies a higher power consumption and lower Q leading to increased phase noise as compared to an *LC*-oscillator.

The investigated circuits in Figs. 11 and 12 are both bandpass filter based oscillator designs. Published experimental results for these types of oscillators show very good performance in terms of phase noise and power consumption [31], [36], [37].

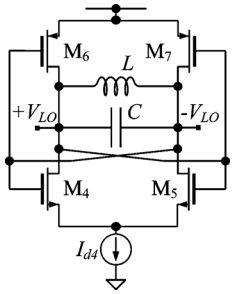

Fig. 12. *LC*-oscillator.

TABLE I
ESTIMATED CRITICAL CURRENTS FOR OSCILLATOR IMPLEMENTATIONS

Implementation	Resonant tank parameters	I_{crit} [μA]
RC on-chip	C =1 fF, $R = 63.7$ kΩ	23.6
LC on-chip	$C = 400$ fF, $L = 10$ nH, $Q = 5$	637
LC off-chip	$C = 75$ fF, $L = 54$ nH, $Q = 35$	16.8

In the *RC*-oscillator an *RC*-network determines the oscillating frequency by shifting the phase of the signal in a feedback loop. With design equations from [37] and $C_1 = C_2 = C_{\min}$ we get resistor values $R_1 = R_2 = R_3 = R_4 = 1/(\omega_{LO} C_{\min})$, where ω_{LO} is the LO angular frequency. The required transconductance for oscillation is $g_m = 3/R_1 = 3\omega_{LO} C_{\min}$, and it is delivered by two complementary transistors using the same bias current. A differential output voltage is provided by having two oscillator branches doubling the bias current. The estimated critical current for oscillation at 2.5 GHz is $I_{\rm crit} = 23.6$ μA. We have arrived to this value by setting the effective voltage at full scale, $V_0 = 0.5$ V, which is required for a good voltage swing.

The result for the *RC*-oscillator can be compared to the LC-oscillator with a load of $R_L = Q/(\omega_{LO} C)$, and a transconductance $g_m = \omega_{LO} C/Q$ again delivered by two complementary transistors. When using an internal inductor with $L = 10$ nH and $Q = 5$ we are forced to have $C = 400$ fF to reach resonance at 2.5 GHz. The estimated critical current summed over the two branches is $I_{\rm crit} = 637$ μA. If instead external inductors with a high Q are used the capacitive load from the bonding pads, $C = 75$ fF, forces the inductance value to $L = 54$ nH. With $Q = 35$ we get a current consumption of $I_{\rm crit} = 16.8$ μA summed over the two branches. An overview of the oscillator bias currents is found in Table I.

A popular mixer implementation is the Gilbert cell [38], offering both frequency conversion and signal gain. However, we have here decided to look at passive voltage switching mixers since they need no power supply, are robust, and also are well suited for CMOS implementation [39].

If we use a double balanced mixer it should be feeded by a differential RF signal. An external balun could be used for differentiation of the signal. Basically the balun is a modified version of the transformer in Fig. 4. Examples of transmission-line baluns are the 180° hybrid and the wide band Marchand balun [40]. A double balanced mixer has a differential output. Accordingly the following IF-amplifier should be differential. Here, we want to compare the single ended TRF receivers analyzed so far with a single ended superheterodyne. A single balanced mixer, Fig. 13, can be used to produce a single ended output, but it still

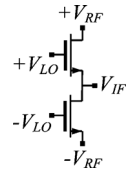

Fig. 13. Single balanced mixer.

have to be feeded by a differential signal. As a matter of fact, the relation between SNR and dc-power is the same for single ended and differential amplifier topologies [31].

Since the IF-amplifier works at a fraction of the carrier frequency it may use a pure resistive load for broadband gain. A broadband IF-amplifier relax the requirements for precise tuning of the LO frequency [21], but it also reduces the ability to reject interfering signals by narrow band channel filters. For the IF gain we have[31]

$$G_{IF} = g_{m1} R_L = \frac{g_{m1}}{\omega_{IF} C_{L1}} \tag{18}$$

where we have used the bandwidth requirement $R_L = 1/(\omega_{IF} C_{L1})$ limiting the load resistor. C_{L1} is the capacitive load of the IF-amplifier.

The output IF voltage from a mixer with conversion gain g_c is

$$V_{IF} = V_{RF} g_c \tag{19}$$

and after IF amplification we find the detector input voltage to be

$$V_D = V_{IF} G_{IF} = V_{IF} \frac{g_{m1}}{\omega_{IF} C_{L1}} = \frac{V_{RF} g_c g_{m1}}{\omega_{IF} C_{L1}}. \tag{20}$$

Using the converting conductance g_D of the detector we get the signal current to be

$$i_s = g_D V_D = g_{m2} \frac{V_D^2}{4V_0} = g_{m2} \frac{V_{RF}^2 g_c^2 g_{m1}^2}{\omega_{IF}^2 C_{L1}^2 4V_0}. \tag{21}$$

Following the previous scheme using (10) to express SNR, the next step is to find the noise currents.

In the superheterodyne the converted noise current $i_{nc}^2 = 8 g_D^2 V_{D,n}^2$ also will include IF-amplifier noise. The noise voltage being converted in the detector is

$$V_{D,n}^2 = V_{IF,n}^2 g_{m1}^2 R_L^2 + 4kTB_{BB} g_{m1} R_L^2 + 4kTB_{BB} R_L. \tag{22}$$

Further, the passive mixer will add noise, which may be modelled by adding the switching transistor channel resistance r_{ds} noise voltage to the source resistance noise voltage being converted in the mixer

$$V_{IF,n}^2 = 4kTB_{BB}(R_S g_c^2 + r_{ds}). \tag{23}$$

Thus, the detector converted noise current becomes

$$i_{nc}^2 = 8 g_D^2 \left(4kTB_{BB}(R_S g_c^2 + r_{ds}) G_{IF}^2 + \right. \\ \left. + \frac{4kTB_{BB} G_{IF}^2}{g_{m1}} + 4kTB_{BB} R_L \right). \tag{24}$$

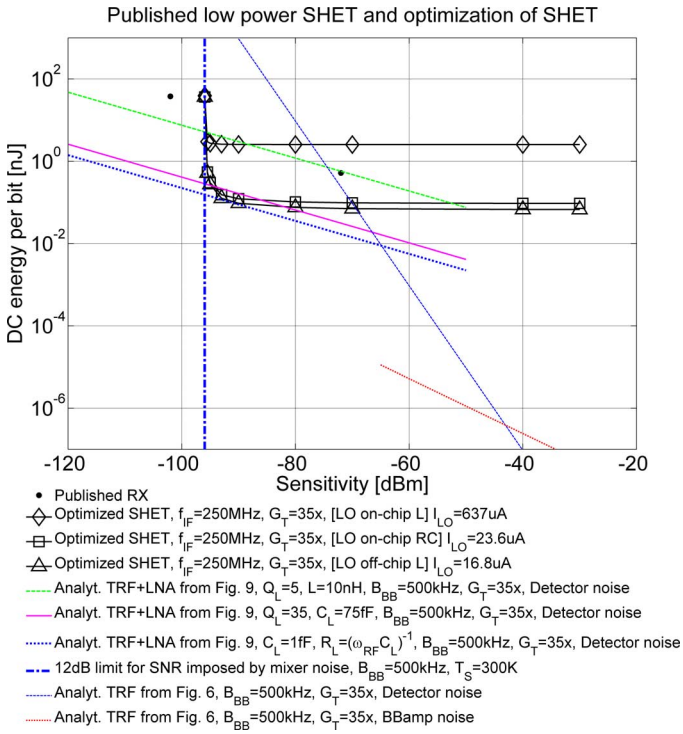

Fig. 14. With the addition of a mixer in front of the detector a superheterodyne is created. Optimizations of (26) with different LO implementations are plotted on top of the analytical result for the TRF, all using $B_{BB} = 500$ kHz and transformer setup as in Fig. 6. Optimizations of superheterodyne with $f_{IF} = 250$ kHz and different LO implementations are plotted as black diamond, square, and triangle. Diamond is for an on-chip inductance *LC*-oscillator, square is for on-chip *RC*-oscillator, and triangle is for off-chip inductance *LC*-oscillator. Vertical blue doted–dashed line marks 12 dB limit for SNR imposed by mixer noise at temperature $T = 300$ K. Analytically calculated curves from Figs. 6 and 9, and superheterodyne receiver data from Fig. 1 are plotted for comparison. Overall the energy-per-bit for the superheterodyne is inferior to the TRF. Oscillator power is kept to a minimum using small mixer switch transistors, but the channel resistance introduce a fixed noise (similar to antenna noise). LO supply power adds a floor to the energy-per-bit for the lower sensitivities.

Here, we assume the signal voltage to be larger than noise voltage, so noise folded around the carrier is much larger than any noise self mixing component. The total noise current including i_{nd}^2 from (4) is,

$$i_n^2 = 4kTB_{BB}\left(g_{m2} + 8g_D^2\left((R_S g_c^2 + \right.\right. \\ \left.\left. + r_{ds})G_{IF}^2 + \frac{G_{IF}^2}{g_{m1}} + R_L\right)\right). \quad (25)$$

Finally, we arrive to the sought SNR expression with the help of (10), and include bias current relations

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}}{V_{RF}^2 g_c^2}\left(2\frac{V_0^7(\omega_{IF}C_{L1})^4}{I_{d2}I_{d1}^4 V_{RF}^2 g_c^2} + R_S g_c^2 \right. \\ \left. + r_{ds} + \frac{V_0}{I_{d1}} + \frac{V_0^2\omega_{IF}C_{L1}}{I_{d1}^2}\right). \quad (26)$$

A graphical presentation of optimization of energy-per-bit performance using (26) is found in Fig. 14 for the different LO implementations. The power budget of the superheterodyne just touches the performance of previous analyzed receivers within a small sensitivity interval where the more power efficient IF amplification pays off compared to RF amplification. We see that the sensitivity is limited upwards by the mixer channel resistance, similar to the effect of antenna noise. At lower sensitivities the LO dominates the power consumption. In the graph minimum switching transistors have been used, with $r_{ds} = 6\ \text{kOhm}$. If we instead used 20 times wider transistors the sensitivity would be improved by 13 dB at the cost of an increased capacitive LO load of about 5 fF. With an *LC*-oscillator the increased capacitive load could be absorbed, for free, by the tank circuit. While for *RC*-oscillator the load would increase LO power consumption. In any case the mixer noise is masked by the previously discussed antenna noise at -92.8 dBm.

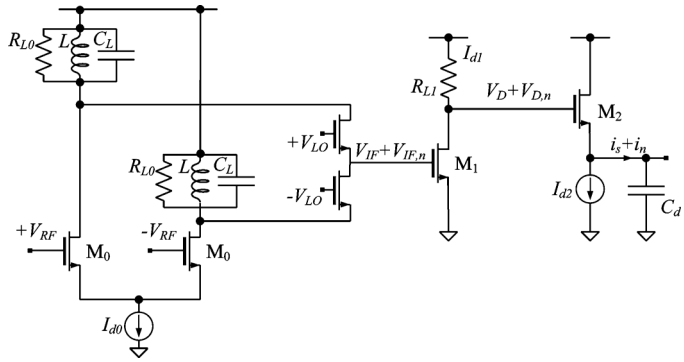

Fig. 15. LNA, mixer, and IF-amplifier followed by detector.

A. Superheterodyne With LNA

As with the TRF receiver we want to investigate if the power budget of the superheterodyne can be improved at higher sensitivities by the insertion of an LNA. With enough gain in the LNA the mixer noise will be swamped together with the detector noise.

A circuit diagram for a superheterodyne with a preceding LNA is found in Fig. 15. The loading resistance (or equivalent resistance of the resonant circuit) is R_{L0} for the LNA and R_{L1} for the IF-amplifier. Still following the scheme using (10) to find output SNR we modify (19) by introducing RF gain G_{RF} from an LNA

$$V_{IF} = V_{RF}G_{RF}g_c. \quad (27)$$

We restate the equation for RF gain (9) to follow symbols used in Fig. 15

$$G_{RF} = \frac{g_{m0}Q_L}{\omega_{RF}C_{L0}} \quad (28)$$

where g_{m0} is the transconductance of M0 and C_{L0} is the capacitive load from subsequent stages and possible tuning capacitors. With (27) and (28) we get a new V_{IF} to be used with (20). The signal current i_s can be found, as before, with the use of (11).

Now the only major modification we have to do before we can find the total SNR is to express noise coming out of the mixer at IF being a result of the LNA, the mixer, and the source resistance

$$V_{IF,n}^2 = 4kTB_{BB}(G_{RF}^2 R_S g_c^2 + g_{m0}R_{L0}^2 g_c^2 + r_{ds}). \quad (29)$$

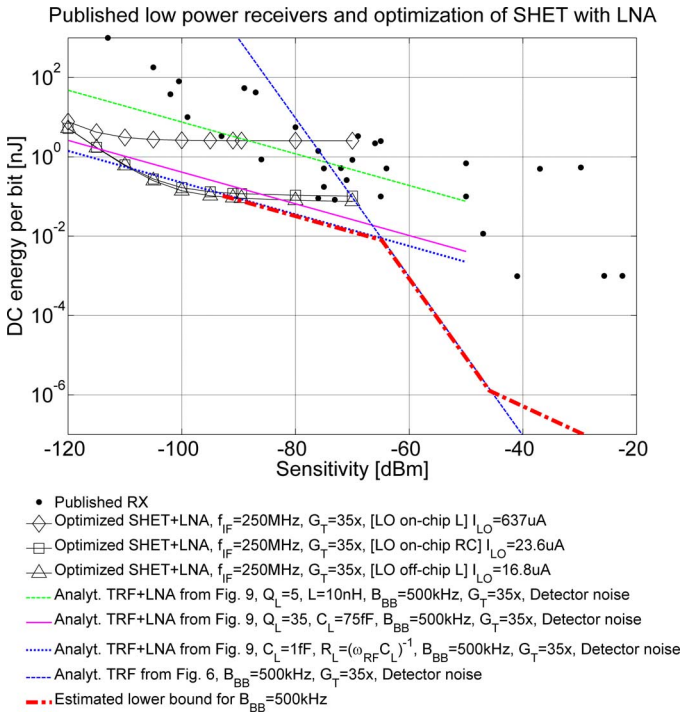

Fig. 16. Impact of mixer noise is reduced by the use of an LNA. Optimizations of LNA enhanced superheterodyne with $f_{IF} = 250$ kHz and using different LO implementations are plotted as black diamond, square, and triangle. Diamond is for a on-chip inductance *LC*-oscillator, square is for on-chip *RC*-oscillator, and triangle is for off-chip inductance *LC*-oscillator. Red dotted–dashed line is our best estimate of the lower bound to power consumption at baseband bandwidth $B_{BB} = 500$ kHz for any receiver architecture (the line stops at the antenna noise limit). All receivers data from Fig. 1 is plotted for comparison. LO supply power add a lower floor on energy-per-bit performance at low sensitivities. With wider baseband bandwidths, B_{BB}, this floor will be pushed downwards.

The first term is source noise, middle term is LNA noise, and last term is mixer noise. The above described noise at IF is amplified in the IF-amplifier and the noise from the amplifier itself is added as in (22). As before the inherent detector noise current i_{nd}^2 is found with (4), and converted noise is found with $i_{nc}^2 = 8g_D^2 V_{D,n}^2$. With (10) we find the inverted SNR for the complete superheterodyne receiver with LNA

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}}{V_{RF}^2 G_{RF}^2 g_c^2 G_{IF}^2}\left(2\frac{V_0^2}{g_{m2}V_{RF}^2 G_{RF}^2 G_{IF}^2 g_c^2} + G_{IF}^2\left(R_S G_{RF}^2 g_c^2 + g_{m0}R_{L0}^2 g_c^2 + r_{ds}\right) + \frac{G_{IF}^2}{g_{m1}} + R_{L1}\right). \tag{30}$$

With bias current relations we have

$$\frac{1}{\eta_{\text{out}}} = \frac{32kTB_{BB}\omega_{RF}^2 C_{L0}^2 V_0^2}{V_{RF}^2 g_c^2 Q_L^2 I_{d0}^2}\left(2\frac{V_0^9 \omega_{RF}^2 C_{L0}^2 \omega_{IF}^4 C_{L1}^4}{I_{d2}I_{d1}^4 I_{d0}^2 Q_L^2 g_c^2 V_{RF}^2} + \frac{R_S I_{d0}^2 Q_L^2 g_c^2}{\omega_{RF}^2 C_{L0}^2 V_0^2} + \frac{I_{d0}Q_L^2 g_c^2}{\omega_{RF}^2 C_{L0}^2 V_0} + \frac{V_0}{I_{d1}} + r_{ds} + \frac{V_0^2 \omega_{IF} C_{L1}}{I_{d1}^2}\right) \tag{31}$$

where C_{L1} is the capacitive load of the IF-amplifier.

A graphical presentation of optimization of energy-per-bit performance using (31) is found in Fig. 16 for the different LO implementations. The optimization of energy-per-bit of the superheterodyne with an internal LNA with resistive load just touches the performance for the TRF also using an internal LNA. The resistive load is attained by setting $Q = 1$ and $C_{L0} = C_{\min}$ in (31). The mixer noise is overcome by the LNA as predicted and the LO supply power add a lower floor on energy-per-bit at low sensitivities.

V. Discussion

At higher receiver sensitivities we see larger currents running through the devices. To keep the effective voltage V_0 low transistors must be made wider. The input impedance will decrease and change the matching properties. This effect is not included in this analysis.

RF properties also have an impact on the choice between single ended and differential topology. If we cannot assume the balun preceding the RF gain stage to have a differential amplitude being doubled due to losses, the SNR improvement of the combined balun and differential amplifier will not be proportional to the doubled bias current.

We have assumed that RF noise bandwidth is much larger than baseband bandwidths, $B_{RF} \gg B_{BB}$. This is true for most wake-up receivers, where bit rates usually are low. However, we have not included noise folding in the mixer, assuming RF bandwidth B_{RF} to be smaller than LO-RF frequency separation.

The efficiency of the IF-amplifier would be improved with a lower IF, but this requires higher LO frequency and increased LO power consumption. An overall improvement is expected anyway, since a fractional change of the IF will correspond to a considerable lower fractional change in LO frequency. However, with a reduced LO-RF separation the LO frequency stability become increasingly important. Frequency stability and phase noise can be improved by the use of phase locked loops, but this requires external reference devices (crystals) and higher power consumption.

The impact of mixer noise can either be reduced by larger switching transistors or by inserting an LNA. Both choices come at a cost of power, since LO power consumption increase with the larger load from switches. On the whole, the superheterodyne offer a complicated trade off in power distribution, while offering little or no extra performance over the less complicated TRF.

Our analysis does not take into consideration the use of cascade amplifier stages. An amplifier block may consist of multiple $K+1$ stages in a chain, where gain factors are multiplied and bias currents are summed. Only the first stage in the cascade has to be optimized for noise, with say a current I_{dn}. Subsequent stages may instead be optimized for maximum gain. If we assume equal amplification in each subsequent stage of the cascade, and each stage has a gain proportional to their individual bias current I_{dk}, then the total amplification of the subsequent cascade is proportional to I_{dk}^K and the total bias current is $I_d = KI_{dk}$. If we modify our expressions for gain according to this we have

$$G = \frac{I_{dn}}{V_0}R_L\frac{I_{dk}^K}{V_0^K}R_L^K = \frac{I_{dn}I_{dk}^K R_L^{(K+1)}}{V_0^{K+1}}. \tag{32}$$

This extension of our analysis would result in somewhat lower bounds but will not change our general conclusions. The threshold for a total gain G where it is appropriate to switch

from a design with $N-1$ stages to a design with N stages in a cascade is

$$G = \left(\frac{N}{N-1}\right)^{N^2-N}. \tag{33}$$

Thus a two stage amplifier should be considered when the total voltage gain exceeds $4\times$. The TRF receiver has its amplification concentrated to the LNA, and the here treated receivers use a maximum gain of $G = 20\times$ before the antenna noise limits the sensitivity. With this level of gain it is justified with three amplifier stages in the LNA. With a growing number of stages and with higher sensitivity the inherent noise of the amplifiers will become evident. This noise, represented by the second term in (14) and (17), and visible as the dotted-dashed red line for a single stage LNA in Fig. 9, will be amplified by all the subsequent stages.

An extension of this analysis with parameters for selectivity would require the addition of at least some first-order relations between filter losses, filter bandwidth, filter roll-off function, filter order, and Q-value of resonators. This added complexity would be needed for both RF-filters and IF-filters but could be a next step in the direction of finding more complete, but yet intuitive designer tools for low-power radio systems.

VI. Conclusion

We have investigated the relation between power consumption and sensitivity for low-power receivers with the goal to understand the lower bound of energy per bit received of such systems. The investigation was limited to one carrier frequency, 2.5 GHz, bandwidths of 50–5000 kHz and a typical 90 nm CMOS process and did not consider selectivity. We found that a simple envelope detector is preferred for low sensitivities (above input RF power about -70 dBm). For higher sensitivities an envelope detector preceded by an LNA is preferred. In no case the more complicated superheterodyne solution offers a clear benefit. The lower bound of energy per bit is controlled both by transistor performance and passive device performance, and for the conditions examined inductor passives are beneficial for antenna impedance transformation only. Our predicted lower bounds are one order of magnitude lower than the best published data for high sensitivities considering carrier frequencies above 500 MHz, and several orders of magnitude lower for low sensitivities over all carrier frequencies. We believe that the presented method for power bound predictions can be extended to include all kinds of RF systems and also include other performance measures as selectivity, linearity, etc.

Appendix
Signal and Noise Conversion in the Detector

In [41] we find an analysis for conversion of signal and noise in a detector. Input SNR to the detector is the ratio between incoming root mean square (rms) RF voltage and incoming rms noise voltage from the source resistance R_S at temperature T over bandwidth B_{RF}

$$\eta_{in} = \frac{\frac{E_0^2}{2}}{4R_S kTB_{RF}} \tag{34}$$

where E_0 is the RF signal amplitude.

The available RF power is

$$P_{av} = \frac{E_0^2}{8R_S} \tag{35}$$

and available noise power is kTB_{RF}. The RF bandwidth is in our case much wider than the baseband bandwidth, $B_{RF} \gg B_{BB}$, and from [41] we have

$$\eta_{\text{out}} = \frac{c^2\left(\frac{E_0^2}{2}\right)^2}{2c^2(4R_S kTB_{RF})^2\frac{B_{BB}}{B_{RF}} + 2E_0^2c^2(4R_S kTB_{RF})\frac{B_{BB}}{B_{RF}}} \tag{36}$$

where c is a conversion coefficient for a quadratic detector. When comparing with our analysis we identify $E_0 = V_D$, $c = 1/(2V_0)$, and $c^2(E_0^2/2)^2 = V_{BB}^2$. The first term of the denominator in (36) is the noise self-mixing component, which we assume to be small and thus is ignored in our further analysis. The second term is noise converted in the detector by the carrier, which with our definitions becomes

$$V_{BBn}^2 = 2E_0^2c^2(4R_S kTB_{BB}) = 8G_D^2(4R_S kTB_{BB}). \tag{37}$$

We now can find the noise current from the detector being a result of incoming noise converted by the carrier

$$i_{nc}^2 = V_{BBn}^2 g_{m2}^2 = 8G_D^2(4R_S kTB_{BB})g_{m2}^2 \tag{38}$$

where g_{m2} is the transconductance of the detector transistor M2. With the converting transconductance $g_D = g_{m2}G_D$ we get

$$i_{nc}^2 = 8(4R_S kTB_{BB})g_D^2. \tag{39}$$

Here, $(4R_S kTB_{BB})$ represents the noise voltage from previous stages. The detector output signal voltage is $V_{BB} = V_D G_D$

Acknowledgment

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References

[1] J. Rabaey, M. Ammer, J. J. L. da Silva, D. Patel, and S. Roundy, "Picoradio supports ad hoc ultra-low power wireless networking," *Computer*, vol. 33, no. 7, pp. 42–48, Jul. 2000.

[2] J. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," *IEEE Pervasive Comput.*, vol. 4, no. 1, pp. 18–27, Jan.-Mar. 2005.

[3] E. Nilsson and C. Svensson, "Envelope detector sensitivity and blocking characteristics," in *Proc. 20th Eur. Conf. Circuit Theory Design*, Aug. 2011, pp. 773–776.

[4] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello, "Single-stage low-power quadrature RF receiver front-end: The LMV cell," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2832–2841, Dec. 2006.
[5] A. Heragu, D. Ruffieux, and C. Enz, "A low power BAW resonator based 2.4-GHz receiver with bandwidth tunable channel selection filter at RF," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1343–1356, Jun. 2013.
[6] N. Mazloum and O. Edfors, "DCW-MAC: An energy efficient medium access scheme using duty-cycled low-power wake-up receivers," in *Proc. IEEE Veh. Technol. Conf.*, 2011, pp. 1–5.
[7] A. Vouilloz, M. Declercq, and C. Dehollain, "A low-power CMOS super-regenerative receiver at 1 GHz," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 440–451, Mar. 2001.
[8] N. Joehl, C. Dehollain, P. Favre, P. Deval, and M. Declerq, "A low-power 1-GHz super-regenerative transceiver with time-shared PLL control," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1025–1031, Jul. 2001.
[9] B. Otis, Y. H. Chee, and J. Rabaey, "A 400 μW-RX, 1.6 mW-TX super-regenerative transceiver for wireless sensor networks," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2005, vol. 1, pp. 396–606.
[10] A. Wong, G. Kathiresan, C. Chan, O. Eljamaly, O. Omeni, D. McDonagh, A. Burdett, and C. Toumazou, "A 1 V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1511–1521, Jul. 2008.
[11] A. Gerosa, S. Solda, A. Bevilacqua, D. Vogrig, and A. Neviani, "An energy-detector for noncoherent impulse-radio UWB receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 1030–1040, May 2009.
[12] S. Solda, M. Caruso, A. Bevilacqua, A. Gerosa, D. Vogrig, and A. Neviani, "A 5 Mb/s UWB-IR transceiver front-end for wireless sensor networks in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1636–1647, Jul. 2011.
[13] J. Bohorquez, A. Chandrakasan, and J. Dawson, "A 350 μW CMOS MSK transmitter and 400 μW OOK super-regenerative receiver for medical implant communications," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1248–1259, Apr. 2009.
[14] J.-Y. Chen, M. P. Flynn, and J. P. Hayes, "A fully integrated auto-calibrated super-regenerative receiver in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, Sep. 2007.
[15] J. Ayers, K. Mayaram, and T. Fiez, "An ultralow-power receiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1759–1769, Sep. 2010.
[16] K. Kim, S. Yun, S. Lee, and S. Nam, "Low-power CMOS super-regenerative receiver with a digitally self-quenching loop," *IEEE Microwave Wireless Compon. Lett.*, vol. 22, no. 9, pp. 486–488, 2012.
[17] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, Z. N. Aldworth, T. L. Daniel, J. Voldman, J. G. Hildebrand, and A. P. Chandrakasan, "A pulsed UWB receiver SoC for insect motion control," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 153–166, Jan. 2010.
[18] P. Kolinko and L. Larson, "Passive RF receiver design for wireless sensor networks," in *IEEE/MTT-S Int. Microwave Symp.*, Jun. 3–8, 2007, pp. 567–570.
[19] D. Daly and A. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.
[20] M. Crepaldi, C. Li, K. Dronson, J. Fernandes, and P. Kinget, "An ultra-low-power interference-robust IR-UWB transceiver chipset using self-synchronizing OOK modulation," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 226–227.
[21] N. M. Pletcher, S. Gambini, and J. M. Rabaey, "A 52 μW wake-up receiver with -72 dBm sensitivity using an uncertain-IF architechture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.
[22] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. de Groot, "A 2.4 GHz/915 MHz 51 μW wake-up receiver with offset and noise suppression," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 9, 2010, pp. 222–224.
[23] Y.-I. Kwon, S.-G. Park, T.-J. Park, K.-S. Cho, and H.-Y. Lee, "An ultra low-power CMOS transceiver using various low-power techniques for LR-WPAN applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 2, pp. 324–336, Feb. 2012.
[24] E. Nilsson and C. Svensson, "Ultra low power wake-up radio using envelope detector and transmission line voltage transformer," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 3, no. 1, pp. 5–12, Mar. 2013.
[25] N. Roberts and D. Wentzloff, "A 98 nw wake-up radio for wireless body area networks," in *Proc. IEEE Radio Freq. Integrat. Circuits Symp.*, 2012, pp. 373–376.
[26] C. De Roover and M. Steyaert, "Energy supply and ULP detection circuits for an RFID localization system in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1273–1285, Jul. 2010.
[27] J.-P. Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2193–2202, Nov. 2005.
[28] K.-W. Cheng, X. Liu, and M. Je, "A 2.4/5.8 GHz 10 μW wake-up receiver with $-65/-50$ dBm sensitivity using direct active RF detection," in *Proc. IEEE Asian Solid State Circuits Conf.*, 2012, pp. 337–340.
[29] C. Hambeck, S. Mahlknecht, and T. Herndl, "A 2.4 μW wake-up receiver for wireless sensor nodes with -71 dBm sensitivity," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2011, pp. 534–537.
[30] J. Bae, L. Yan, and H.-J. Yoo, "A low energy injection-locked FSK transceiver with frequency-to-amplitude conversion for body sensor applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 928–937, Apr. 2011.
[31] C. Svensson and J. J. Wikner, "Power consumption of analog circuits: A tutorial," *Analog Integrated Circuits Signal Process.*, vol. 65, Nov. 2010.
[32] J. Wight, J. Long, L. Carley, and T. Riley, "On-die synthesized inductors: Boon or bane?," *IEEE Microwave Mag.*, vol. 11, no. 3, pp. 95–104, May 2010.
[33] J.-Y. Park, D.-W. Kim, Y.-S. Son, J.-C. Ha, J.-K. Song, C.-S. Jang, and W.-Y. Jung, "Low-capacitance low-voltage triggered SCR ESD clamp using nMOS with asymmetric drain for RF ICs," *IEEE Trans. Microwave Theory Tech.*, vol. 59, no. 2, pp. 360–367, Feb. 2011.
[34] G. Breed, "Basic principles of electrically small antennas," *High Frequency Electron.*, vol. 6, no. 2, 2007.
[35] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2004.
[36] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1018–1024, Jul. 2001.
[37] S. W. Park and E. Sanchez-Sinencio, "RF oscillator based on a passive RC bandpass filter," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3092–3101, Nov. 2009.
[38] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. 3, no. 4, pp. 365–373, Dec. 1968.
[39] T. Lee, "CMOS RF integrated circuits: Past, present and future (invited)," in *Proc. 29th Eur. Microwave Conf.*, 1999, vol. 1, pp. 12–19.
[40] S. Basu and S. Maas, "Design and performance of a planar star mixer," *IEEE Trans. Microwave Theory Tech.*, vol. 41, no. 11, pp. 2028–2030, 1993.
[41] T. Orhaug and B. Höglund, *Rymdkommunikationsteknik*, 5th ed. Göteborg, Sweden: Chalmers tekniska högskola, 1974.

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