Ultra Low Power Wake-Up Radio Using Envelope Detector and Transmission Line Voltage Transformer

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***Abstract*—An ultra-low power wake-up radio receiver using no oscillators is described. The radio utilizes an envelope detector followed by a baseband amplifier and is fabricated in a 130-nm complementary metal–oxide–semiconductor process. The receiver is preceded by a passive radio-frequency voltage transformer, also providing 50 Ω antenna matching, fabricated as transmission lines on the FR4 chip carrier. A sensitivity of −47 dBm with 200 kb/s on–off keying modulation is measured at a current consumption of 2.3 μA from a 1 V supply. No trimming is used. The receiver accepts a −13 dBm continuous wave blocking signal, or modulated blockers 6 dB below the sensitivity limit, with no loss of sensitivity.**

***Index Terms*—Blocking signal, complementary metal–oxide–semiconductor (CMOS), envelope detector sensitivity, radio-frequency identification (RFID), ultra low power, wake-up radio, wireless sensor networks.**

I. Introduction

THE RESEARCH on low-power radio technology is motivated by the needs from several application areas. Among these application areas are distributed wireless sensor networks, which may include chemical security monitoring [1], buried sensors for buildings and structure health [2], biotelemetry [3], [4], or surveillance in logistic chains [5]. These types of networks are sometimes referred to as Internet of Things (IoT), ubiquitous computing, or simply as radio-frequency identification (RFID). A common requirement is the need for ultra low power receiver solutions. The network node lifetime is determined by its power consumption and its battery capacity. Energy scavenging from mechanical vibrations, thermal gradients, or electromagnetic fields could increase the lifetime or eliminate the need for batteries. Exclusion of batteries may drastically change the service required to maintain the network, but with available radio technology this will also severely reduce the communication range for the nodes. A common accepted dc power consumption level where energy scavenging is feasible for a node is around 100 μW [6].

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Two different network extremes can be defined, the event driven network and the Wake-Up driven network. The event driven network active power is set by the power consumption of the sensor (computational power included). Here, it is the sensor which activates the communication sessions [7] at predefined events. In Wake-Up driven networks, the communication sessions are initiated over the air interface, and it is the radio receiver active-power that sets the power consumption [8]. Note that for a Wake-Up radio it is not the power required transferring one bit of information being important, but rather the active power needed to continuously be aware. The Wake-Up network is typically based on one central reader and several "slave" nodes, where the dedicated master is supplied with "unlimited" power.

Wirelessly powered sensor networks have gained lot of interest being independent from external energy sources other than the transmitted radio energy. These systems are often limited in range by the power scavenge efficiency rather than by the receiver sensitivity [2], [9]–[11]. By reducing the needed receiver power consumption both the range and time to wake up would improve.

Duty cycling of the receiver is a straight forward solution to reduce average power consumption but lead to longer wake up time and a need for a good clock to time the rendezvous. Further, the clock has to be stable over temperature and time, or it has to periodically perform costly calibration sequences [12], [13]. Different medium access control (MAC) protocols have also been proposed in cross-level design efforts to relax clock accuracy requirements and improve overall network efficiency, and thereby increase network lifetime [14], [15].

Several proposed Wake-Up solutions are based on external detecting devices, such as Schottky diodes [16]–[18]. A successful Wake-Up radio solution has to be low cost and preferably work as an intellectual property (IP) block to be included in several applications. This implies a single chip design in a commercially available complementary metal–oxide–semiconductor (CMOS) process, and a use of low-cost materials [8]. Further, the design needs to be robust in terms of process parameters variations, as well as environment variations and radio interference [19]–[21]. Among the proposed receiver architectures for Wake-Up radios we find the super regenerative receiver. This architecture use positive feedback to increase gain at radio frequencies to reach a better sensitivity. Although the super regenerator is suitable for efficient energy per bit communication at high speeds, its active power makes it inefficient as a pure Wake-Up receiver [22]–[24]. A better suited, and previously used, receiver architecture is the tuned RF receiver (see Fig. 1). The tuned RF receiver performs envelope

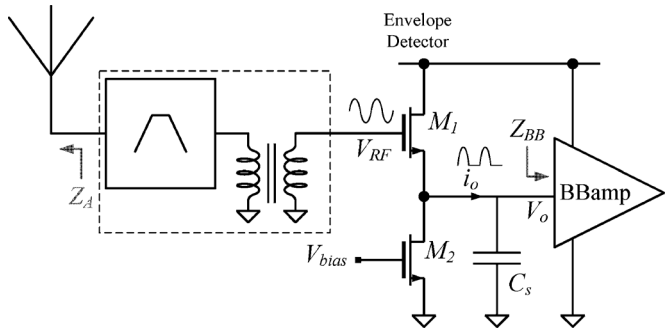

Fig. 1. Tuned RF receiver. The dashed line surrounds functional blocks being implemented as an external transmission line voltage transformer in this work.

detection at the carrier frequency without any prior frequency conversion. Thus, energy consuming local oscillators and mixers are avoided, but at the cost of sensitivity and selectivity. In the tuned RF receiver selectivity is instead enabled by a preceding RF-filter. The receiver in this paper is a tuned RF receiver without any oscillators, neither in the RF chain nor in the baseband stages. No external components are used, except for a transmission line voltage transformer on a FR4 laminate carrying the RF-ASIC. The transformer works both as an RF filter and as an impedance transformer, increasing the output voltage at a given input power.

II. Oscillator Free Architecture

The Wake-Up radio has the single purpose to recognize a predetermined ID-code bit pattern in the air and the chosen architecture is focused on simplicity. It uses no oscillators, and no control or calibration loops as phased locked loops or super regenerative solutions. This enables short startup time and avoidance of lock-in processes adding to overall power consumption [25].

As much as possible of the radio functionality should be handled over to the interrogator or reader (the term "reader" emanates from the RFID community and is a bit misleading here since we only use downlink communication). A very small amount of data will be sent at each wake up session, only a few hundred bits long ID-code. We use on–off keying modulation of the carrier; although this is spectral inefficient it is motivated by the short transmission bursts and the simplification of the receiver design. A carrier frequency of 2450 MHz (ISM) offers a good compromise between size and range, and an ability to see "around" obstacles.

A. Envelope Detection

The incoming RF carrier drives a diode, or other rectifying component. The envelope detector self mixing efficiency falls off as the carrier power decrease. Thus, the sensitivity for a tuned RF receiver is moderate compared to the super heterodyne with a mixer always being driven by a strong LO signal. However, the typical applications for the Wake-Up receivers requires only rather short transmission range, up to about 10 m [22]. A reduction in active power achieved by excluding the local oscillator is well motivated.

The envelope detector folds the modulated spectrum around the carrier f_0 down to baseband frequency f_m (see Fig. 2). The

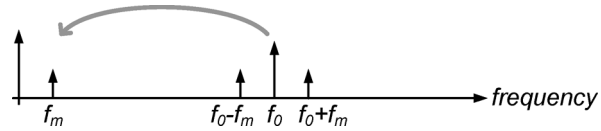

Fig. 2. Envelope detection.

baseband output voltage V_m from the envelope detector is proportional to the square of the input amplitude of the RF carrier V_{RF}

$$V_m \propto V_{\mathrm{RF}}^2. \tag{1}$$

A subthreshold biased MOST envelope detector as described in [20] will have a noise current limiting its output signal-to-noise ratio (SNR) and its sensitivity. From [20] we get

$$\mathrm{SNR} = \frac{g_m V_{\mathrm{RF}}^4}{64kTV_0^2B}. \tag{2}$$

Here, g_m is transistor transconductance, kT is available thermal energy, $V_0 = nkT/q$ with n being transistor ideality factor and q the unit charge, and B is detector bandwidth. It is clear that boosting V_{RF} with a pre-amplifier in front of the detector would improve the sensitivity drastically. It is worth to note that it is the carrier amplitude that is important, rather than carrier power, and that voltage amplification can be achieved passively by a transformer. The input impedance of a MOST detector is, for narrow band transformation, so high that the achievable transformation ratio or transformer output impedance R_S, is setting the performance. The transformer output voltage amplitude at an available input power P_{av} is found by

$$V_{\mathrm{RF}} = \sqrt{8P_{\mathrm{av}}R_S}. \tag{3}$$

The maximum achievable output impedance depends on technology parameter limitations and losses. It is difficult to get efficient voltage transformation with on-chip inductors, the large inductances needed would occupy large die area and have too low resonant frequencies. Lumped off-chip inductors would add to the component count cost and occupy valuable bonding pad resources for terminals. Further, the transmission lines and bond wires used to connect the inductor have to be taken into account during design, and they prove to be difficult to control. Distributed passive transformer may be a simple way to get around the problem without adding components. High Q-values are available with modern laminate materials, even a low cost material as FR4 will suffice.

The output from the detector is amplified to ensure safe switching in a digitizer. As the detector output at weak input carrier levels fall of very quickly the baseband processing must be designed for low noise performance. A low baseband bandwidth enables subthreshold biased transistors to be used in the design and ensure low power consumption.

An expression for the total noise figure of a tuned RF receiver is given in [8]

$$F_{\mathrm{tot}} = 2F_{\mathrm{amp}} + \frac{N_{\mathrm{LF}}k_{\mathrm{dc}}^2}{N_{\mathrm{src}}A_v^2k^2} + \frac{N_{o,D}}{N_{\mathrm{src}}A_v^2k^2}. \tag{4}$$

Here, $F_{\rm amp}$ and A_v is the noise figure and voltage gain, respectively, of the preamplifier, $N_{\rm LF}$ is low-frequency noise at the output of the preamplifier, k and $k_{\rm dc}^2$ is the conversion gain and linear transfer function respectively of the detector, $N_{o,D}$ is the output noise from the envelope detector, and finally, $N_{\rm src}$ is the noise power of the source resistance. Both noise figure $F_{\rm amp}$ and low frequency noise $N_{\rm LF}$ of our passive voltage transformer will be very small compared to the envelope detector noise contribution. Thus, we may simplify (4) to

$$F_{\rm tot} \approx \frac{N_{o,D}}{N_{\rm src} A_v^2 k^2}. \tag{5}$$

With a given minimum acceptable $\mathrm{SNR}_{\rm min}$ the minimum detectable power sensitivity of the receiver may now be calculated by

$$P_{\rm sens} = kTBF_{\rm tot}\mathrm{SNR}_{\rm min}. \tag{6}$$

Using (2) together with the targeted parameters of this work, $\mathrm{SNR}_{\rm min} = 12$ dB, $V_0 = 50$ mV, $B = 200$ kHz, and with a detector current $I_d = 1$ μA (using $g_m = I_d/V_0$), the sensitivity may be calculated to about 3.2 mV. Corresponding signal power for the calculated sensitivity voltage depend on voltage transformer efficiency and ratio. When detector noise dominates the noise budget of the receiver, as in this work, it is beneficial to reach for a higher voltage transformer ratio, corresponding to a larger transformer output impedance. With a transformer input impedance of 50 Ω and an output impedance of 2000 Ω, the sensitivity will be about -56 dBm, while an output impedance of 300 Ω results in about -48 dBm.

B. ID Code Correlation

The baseband digital signal processing requires a baseband clock. Although this clock will run at a significant lower frequency than the local oscillator it will consume energy, and require external resonating elements such as crystals, or capacitors, and a periodical re-synchronization such as a phase locked loop. The baseband clock can instead be embedded in the transmitted data. If no phase locked loop or other flywheel function is included the clock must be transferred together with each data bit. Manchester coding enables this by coding each ID-code bit with a transition; the bit value "1" is coded with a "01"-transition, and bit value "0" is coded with a "10"-transition [26]. The cost is a doubled edge rate but the gain is, again, a simplified design. The actual bandwidth of the baseband signal is not increased but shifted upwards, reducing the impact of 1/f-noise [27]. Thus, the baseband signal will be dc-free and the baseband circuitry would not need to have any dc-gain.

A self-clocked correlator (see Fig. 3), compares the received data with the stored ID. Data would be shifted in to a shift register by the recovered clock encoded in the Manchester data. A short preamble bit pattern is used to trigger the clock recovery circuit and to start the correlation. This would reduce the activity of the digital logic and save spending of dynamic energy. A hardware implementation of the demodulator can be made with low power building blocks, where the only always aware

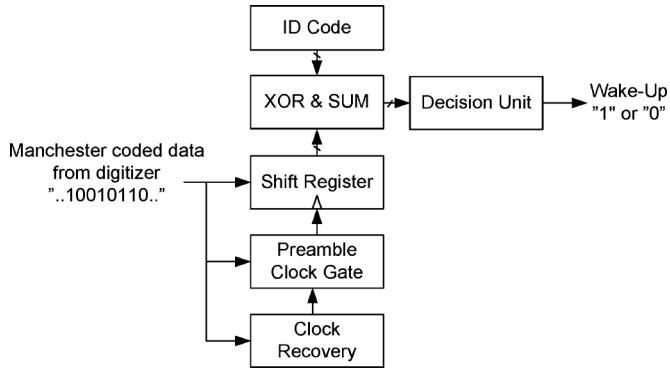

Fig. 3. Self-clocked correlator block diagram.

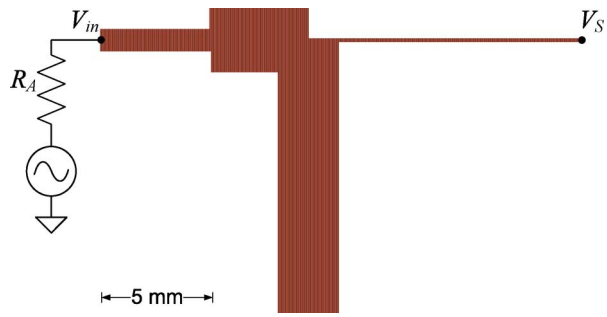

Fig. 4. RF voltage transformer metal pattern layout on 0.508-mm-thick FR4.

part is the clock recovery circuit. It can be designed for very low power, and would consist of an edge detector followed by a monostable multivibrator and pulse shaping inverters. We believe that the analog parts of the receiver will dominate the complete receiver power budget.

The length of the ID-code typically is around 100 bits. The EPC transponder Class 1 use 96 bits for its ID [28]. After Manchester encoding and addition of preamble the result is around 200 bits to transfer over the air interface. One thousand units may be addressed within 1 s with a bit rate of 200 kb/s.

III. Circuit Design

A test chip was designed with an envelope detector, a baseband amplifier, and a buffer amplifier. An RF voltage transformer was placed on the FR4 printed circuit board (PCB) carrying the die. The receiver was designed for 1 V bias to enable a low power design. For the same purpose all devices are operating in moderate or weak inversion.

A. RF Voltage Transformer

The matching network was designed for a 0.508-mm-thick FR4 laminate (see Figs. 4 and 5), and consists of a 50-Ω transmission line leading to a single stub combined with a transmission line. Further, a bias network (not depicted in Figs. 4 or 5) for biasing of the detector via the RF input pad was attached to the transformer.

A narrow band circuit model of the transformer and antenna is seen in Fig. 6. The antenna impedance R_A as seen from the detector input through the matching circuit may be modelled as a source resistance R_S in parallel with an inductance L_S. The equivalent source resistance is about $R_S = 1.84$ kΩ

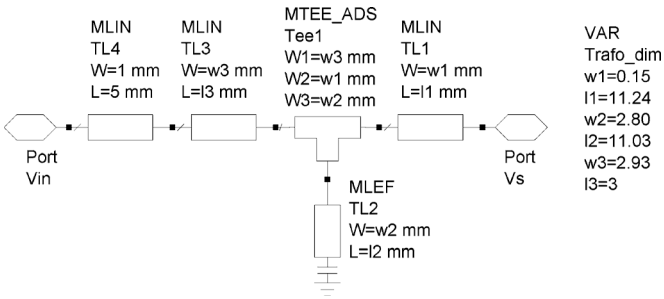

Fig. 5. Simulation model geometry parameters for RF voltage transformer.

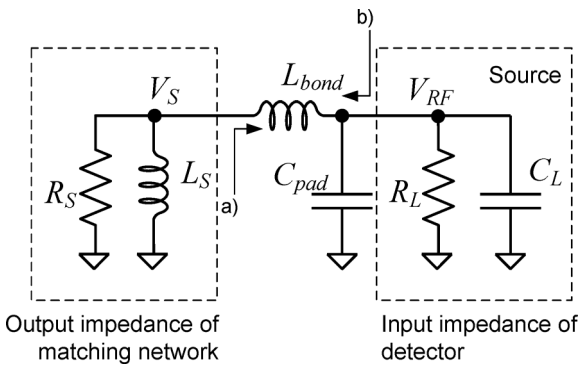

Fig. 6. Narrow band circuit model of antenna, transformer, and detector.

and the inductance is $L_S = 9.33$ nH. Looking into the detector (from the chip input pad) we see the pad capacitance (including electrostatic discharge (ESD) protection), the transistor gate capacitance, and bias resistor in parallel ($C_{\rm pad}, R_L$, and C_L). Placed between the detector input and the matching network is the bonding wire $L_{\rm bond}$. If we now look into the detector through the bond wire, view a) in Fig. 6, the detector impedance $(R_L//X_{CL})$ is transformed downwards. The equivalent loading in this case is 13.5 kΩ in parallel with 421 fF. The tank circuit formed by equivalent inductor L_S and the loading capacitance of 421 fF has a resonance frequency of 2.5 GHz.

The circuit simulation of the design was verified with momentum EM simulations in ADS. Momentum EM simulations take into account metal losses, dielectric losses, and unintended coupling between circuit elements. Minor tuning was needed to reach performance. A final design of the matching network included biasing network, detector transistor, pad, and ESD loading capacitance.

B. Envelope Detector

The detector is depicted in Fig. 7 [20]. NMOS transistor M1 is the rectifying component and NMOS transistor, M2, is a constant current bias source. The bias current is set to 1 μA by keeping $V_{\rm bias} = 235$ mV. M1 is driven in subthreshold region for an efficient nonlinear response. An on-chip resistor could be used to connect the gate of M1 to VDD, but we chose to bias the gate of M1 via the RF input pad for greater flexibility. Since bias current is kept stable by M2, the drain-source bias voltage over M1 will decrease for strong input signals.

Broad band input impedance of the detector depend on the gate capacitance, but in our case the total capacitive load from the input pad and the ESD protection diodes dominate. The size

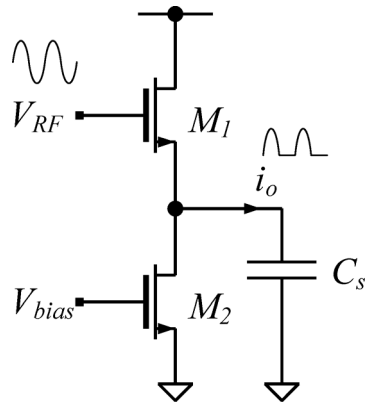

Fig. 7. Envelope detector.

of M1 is set by a complicated tradeoff between output amplitude, power consumption, noise, and RF bandwidth. A large transistor can handle a larger current, and still be in subthreshold region, leading to stronger output amplitude. While a small transistor load the transformer with less capacitance, leading to a higher potential transformation ratio. Power consumption restricts the upper bound of the size of M1, while 1/f-noise restricts the lower bound on the size of both M1 and M2. The output capacitor C_S acts as bypass for the RF signal to ground and as a lowpass filter together with the output resistance R_O. Output resistance of the detector is

$$R_O = \frac{1}{g_{m1} + g_{do2}} \tag{7}$$

where g_{m1} is the transconductance of M1 and g_{do2} is the channel conductance of M2. The detector output current charge the filter capacitor and the voltage will vary along with the modulation signal. We use a dc-free Manchester coded baseband signal and further filtering will take place in the baseband amplifier. The output capacitor should be kept small (1 pF) to save expensive die area. DC level fluctuations from the detector are blocked out from the baseband amplifier by a dc-block capacitor.

C. Baseband Amplifier

The resulting baseband signal voltage over the output capacitance must be amplified and further filtered for secure level switching at the digitizer. This is performed by two amplifier stages connected in series (see Fig. 8). The stages are based on differential feedback cascode stages. Each stage amplifies about 30 dB (see Fig. 9) and they are not optimized for linearity. The output voltage dc-level from the last stage can be controlled by $V_{\rm ref}$ and may in turn control the bias point of a following digitizer.

The detector signal is very weak and we do not want the baseband amplifier to dominate the noise budget. Therefore, the baseband amplifiers have to be designed for low noise performance. The largest noise contributor is the input transistor M1 of the first amplifier stage. The noise voltage is $V_n = \sqrt{4kT\gamma B/g_m}$, where γ is the noise coefficient of the transistor, and B is the bandwidth. The goal is to have a SNR better than 10 dB, the smallest estimated amplitude from the envelope detector is $V_m = 0.13$ mV and the bandwidth is

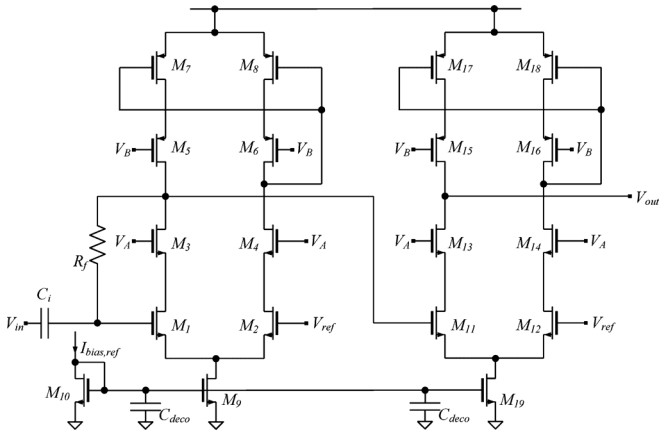

Fig. 8. Baseband amplifier.

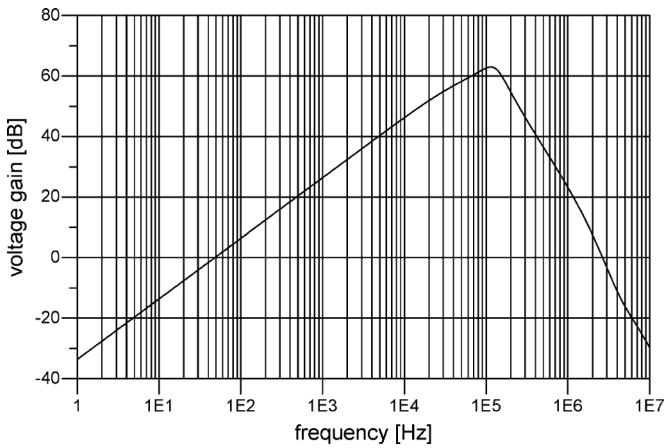

Fig. 9. Baseband amplifier simulated gain.

$B = 100$ kHz. The lowest acceptable g_m of M1 can be found by

$$V_n = \sqrt{4kT\gamma B/g_m} \leq \frac{V_m}{\sqrt{2}\sqrt{10}} \tag{8}$$

$$g_m \geq \frac{8kT\gamma B10}{V_m^2} = 1.9 \quad \mu S, \quad (\gamma = 1). \tag{9}$$

This transconductance give us the lowest acceptable bias current of the amplifier.

Our design is optimized for a bit rate of 200 kb/s. The filter topology chosen have a bandpass characteristic and require a high resistive path, R_f, and a dc-blocking capacitor C_i. The high resistance in the feedback ensures a high input impedance towards the detector. The resistor R_f is set to 65 MΩ, and is implemented with a subthreshold biased MOST using the channel resistance. The channel resistivity has an exponential dependence to the gate voltage and the gate bias needs effective decoupling for low noise performance.

The lowest frequency component in the Manchester coded baseband signal is $f_{\text{low}} = f_{\text{bitrate}}/4$, and with $f_{\text{bitrate}} = 200$ kb/s over the air we get $f_{\text{low}} = 50$ kHz. The highest frequency through the baseband amplifier is $f_{\text{high}} = 3 \cdot f_{\text{bitrate}}/2 = 300$ kHz, where we keep the third overtone for sharper transitions in the bit stream.

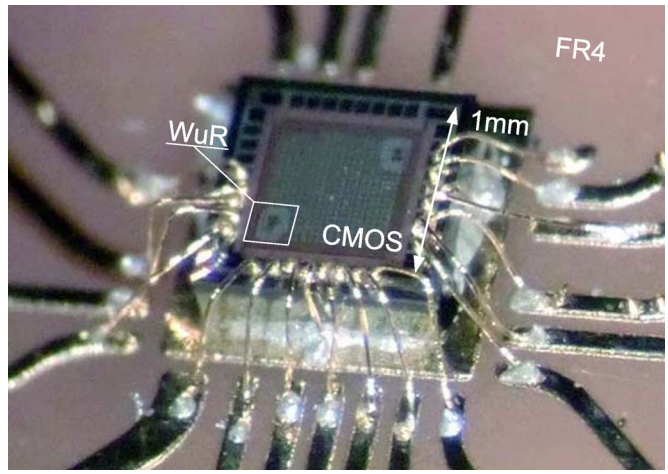

Fig. 10. Die photograph of WuR mounted on FR4 carrier substrate.

For simplicity reasons, we did not include bias circuitry in the present design. The bias circuitry for the baseband amplifier needs to be carefully designed to limit the impact of process and temperature variations. Still, we expect a relatively low sensitivity to variations, as we can have a dc blocker at the output and as the frequency characteristic is not very steep.

D. Buffer Amplifier

A source follower amplifier was added to the design as buffer for measurement purposes. The buffer amplifier adds no voltage gain to signal but is capable to drive larger currents and isolates the baseband amplifier from the capacitive and resistive loading of the bonding pad and measurement equipment. The buffer was biased with $V_{dd} = 2.5$ V and use double oxide gate thickness transistors. The buffer amplifier has a 3-dB bandwidth of 7 MHz.

IV. Measurement Results

The receiver was fabricated in a 130-nm CMOS process with MIM capacitors. No external components are used other than an etched transformer in the FR4 carrier PCB. The integrated circuitry (see Fig. 10) is fitted within an area of around 7000 μm^2 and is hence suited to be used as an IP-block being placed in a die corner, or near the die edge, of a general ASIC. The total current consumption of the detector and baseband amplifier is 2.3 μA.

Demodulation of the baseband signal is realized in MATLAB for bit error rate (BER) measurement. Baseband sampling frequency is 800 kHz and data is processed in sequences with a length of 10^4 bits. For better precision several sequences are used. After being digitized the signal is normalized between 0 and 1 and passed to a Schmitt-trigger. A following monostable multivibrator secures a pulse-width of four samples.

A. Input Matching

The input matching of the Wake-Up of radio was measured at the transformer input terminal (see Fig. 11). Compared to simulations the frequency response was shifted 67 MHz upwards.

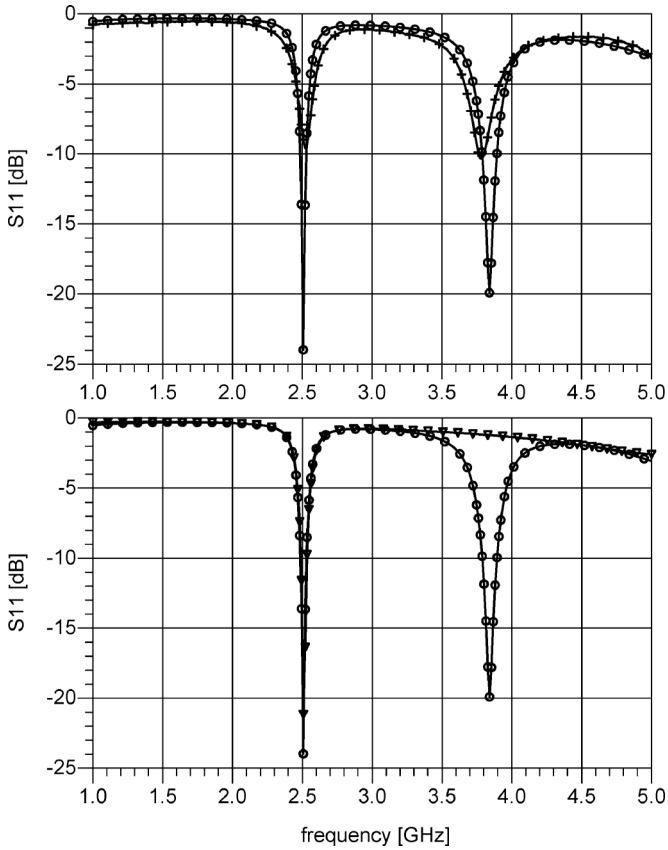

Fig. 11. Upper: Measured (cross) and simulated (circle) input matching with transformer and bias network. Lower: Comparison of simulations of RF-transformer standing alone (triangle) and RF-transformer including the bias network implemented on the experimental FR4 and used during measurements (circle).

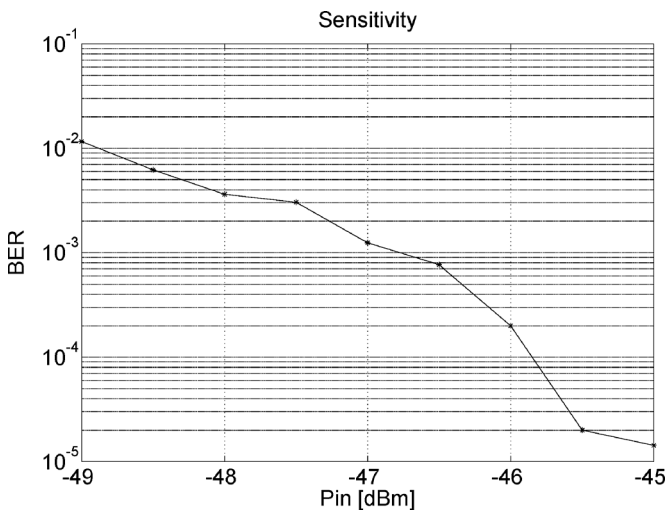

Fig. 12. Measured BER at $f_{\rm in} = 2450$ MHz.

The shift is probably caused by errors in the model of the input pad capacitance and the bond wire inductance.

The spurious response at 3.75 GHz is a result of the external bias network attached to the transformer (see Fig. 11). No significant sensitivity was measured at 3.75 GHz. The return loss of -9 dB is somewhat high, but will not affect the sensitivity as the detector is voltage sensitive rather than power sensitive.

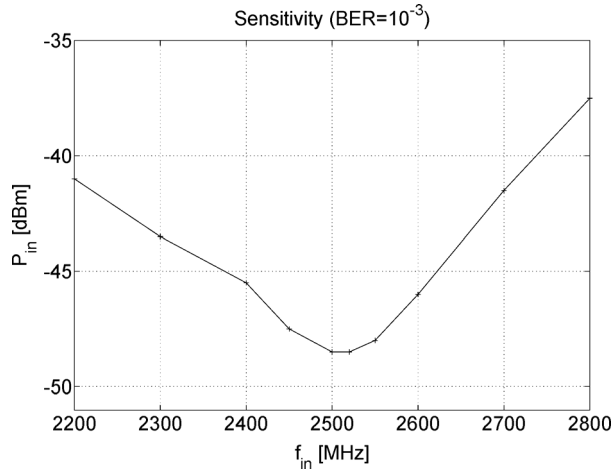

Fig. 13. Measured sensitivity bandwidth.

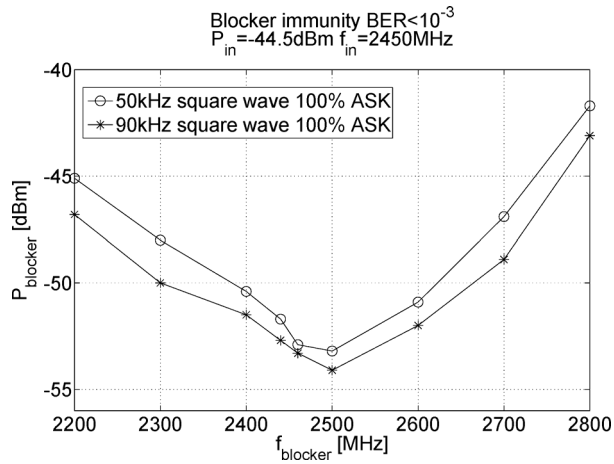

Fig. 14. Measured immunity to modulated blocker signal.

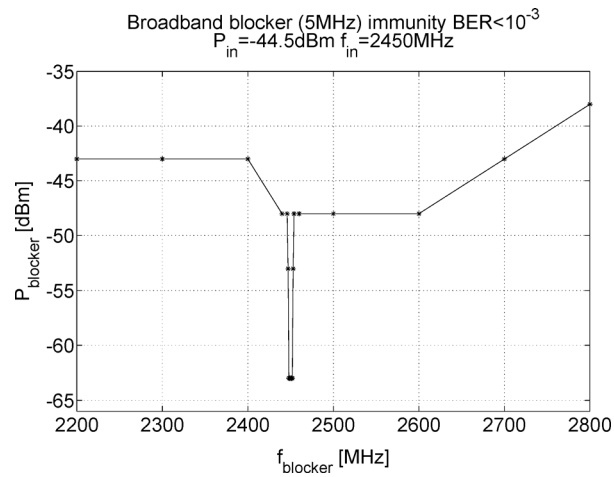

Fig. 15. Measured immunity to broadband 64QAM modulated blocker signal (simulating WLAN).

B. Sensitivity

Receiver sensitivity was measured with a 2450 MHz carrier signal modulated with 100% ASK (see Fig. 12). The RF bandwidth is found in Fig. 13, where the lowest input power resulting

TABLE I
COMPARISON OF RECENT PUBLISHED IMPLEMENTED LOW POWER RADIOS

	[22]	[30]	[8]	[27]	[16]	[18]	[31]	This work
Technology	CMOS 180nm	BAW match, CMOS 90nm	BAW match, CMOS 90nm	Off-chip ind., CMOS 90nm	Schottky, μCtrl	Schottky, μCtrl	CMOS 180nm	FR4 match, CMOS 130nm
Frequency [MHz]	2400	1900	2000	2400	868	860	2400	2450
nJ/bit	0.86	1.6	0.52	0.51	1350	-	0.55	0.023
Bit rate [kbps]	250	40	100	100	0.75	9.6	1.95	200
Sensitivity [dBm]	-86	-50	-72	-64	4.37	-35	-29.8	-47
Power [μW]	215	65	52	51	12.5	10.8	1.08	2.3

in $\mathrm{BER} = 10^{-3}$ has been plotted against the carrier frequency. The best sensitivity, $P_{\mathrm{in}} = -48.5$ dBm, is found at $f_{\mathrm{in}} = 2520$ MHz, corresponding well to the best matching response from the transformer.

Slow variations in amplitude and dc-level at the output of the baseband amplifier have been measured and verified by simulations. The amplifier is designed for ultra low power and low noise, but must not load the detector output with too low impedance. This limits the size of the input transistor and thereby the 1/f-noise performance of the amplifier [29].

C. Interference Immunity

Immunity to interfering radio signals is important for Wake-Up radios. The proposed design is very resilient to sources with a modulation spectrum outside the baseband amplifier bandwidth. Further, the use of a passive transformer for voltage amplification makes the design robust against saturation and signal intermodulation caused by any overdrive of active components. A continuous wave blocker signal with a level of -13 dBm only 1 MHz below the carrier frequency did not swamp the sensitivity of the radio. During these measurements the modulated carrier signal, at 2450 MHz, was fixed at a power 3 dB above the required level for a $\mathrm{BER} = 10^{-3}$ without interference.

The result from the same set up, but with a modulated blocker, is presented in Fig. 14. Two different baseband signals were used to modulate the blocker, a 50-kHz and a 90-kHz square wave, respectively. As long as the modulated interferer power was roughly 6 dB below the sensitivity limit level the Wake-Up radio was not blocked.

A particularly important blocker is a WLAN signal, also utilizing the ISM band. We, therefore, tested the effect of a WLAN signal, simulated as a 64QAM modulated signal with 5-MHz bandwidth (see Fig. 15). We note that for WLAN signal we can accept up to -48 dBm blocker power without loss of sensitivity (except when the blocker is located within 2.5 MHz from the wanted carrier). The reason is that the baseband amplifier catches only a limited part of the 5-MHz WLAN spectrum, so not only the RF selectivity but also the baseband selectivity helps to suppress blockers.

V. DISCUSSION

The present design aims at very low power consumption at acceptable sensitivity for a continuously aware wake-up receiver. We therefore chosen an architecture based on an envelope detector and a passive RF voltage gain, limiting the sensitivity to about -50 dBm [20].

Aiming for a better sensitivity would require higher voltage transformation ratio, higher detector transconductance (and current consumption), or the addition of an LNA between the transformer and the detector (also increasing current consumption). Higher voltage transformation ratio is difficult to achieve due to limitations set by transformer manufacturing and materials. Higher detector transconductance is very expensive in power consumption, as the transconductance needed is proportional to the inverse square of power sensitivity [see (2)] and the current consumption is proportional to the transconductance. The addition of an LNA between the voltage transformer and the detector can be expected to improve the sensitivity with limited power consumption increase but at the cost of lower immunity to blockers (briefly discussed in [20]).

In Table I we compare the present design with recently published implemented designs with power consumption below 400 μW. This comparison is not perfect; in some cases (including the present one), the digital power consumption is not included, and in others it is included. Still, we believe that the combination of -47 dBm sensitivity and 2.3 μW power consumption is the best achieved until date. Designs with better sensitivity all consume more than 20 times the power of the present one.

VI. CONCLUSION

In [20] we estimate the reachable sensitivity of a detector consuming 1 μW to be approximately -50 dBm. This estimate was based on a detector interfaced with a high impedance antenna and without baseband amplifier. Measurements and simulations indicate that, with present basic baseband signal processing, the sensitivity is actually -47 dBm, limited by 1/f-noise in the baseband amplifier. With an extended filtering a sensitivity better than -50 dBm should be possible. However, our primary goal here is to show the possibilities with a simple and robust oscillator-free Wake-Up radio. The proposed design offers a robust and trim-free solution easily implemented in a ordinary CMOS process without adding any external lumped components.

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