Guest Editorial
Dynamical Neuro-AI Learning Systems: Devices, Circuits, Architecture and Algorithms

THIS Special Issue of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) is dedicated to demonstrating the latest research progress on dynamical neuro-artificial intelligence (AI) learning systems that bridge the gap between devices, circuits, architectures, and algorithms. The growing demand for AI has spurred the development of systems that: 1) co-localize computation and memory; 2) enhance circuits and devices optimized for operations prevalent in deep learning; and 3) implement lightweight and compressed machine learning models thereby achieving greater accuracy with less resources.

More exploratory approaches to optimizing machine learning harness dynamical devices, circuits, and systems. Dynamical systems model the natural dynamics of real-world environments. Current neural network algorithms rely heavily on abstracted models of synapses, neurons, and learning rules where biological details are stripped away. Integrating the dynamics seen in biological synapses and neurons could give us insights on the energy efficiency of these richer models and can help drive the network accelerators to a higher level of efficiency.

This Special Issue aims at providing a comprehensive perspective on the state of research in the field of dynamical neuro-AI systems from a cross-stack abstraction lens, through a selection of recent contributions. The 23 papers in this issue went through a rigorous review process, and can be cataloged into the following themes as we move up the abstraction layers: 1) devices; 2) analog and mixed-signal circuits; 3) digital design and computer architecture; and 4) algorithms. Unique to the field of neuromorphic computing and neuro-AI, many accepted papers are heavily influenced by dynamical systems theory, neuroscience, or otherwise span these various circuits and systems abstractions.

I. DEVICES

Neuromorphic devices, which mimic the neural structure of the human brain, are pivotal in advancing neuro-AI systems, as they offer highly efficient computational paradigms that significantly enhance efficiency. However, it is often challenging to integrate emerging devices with larger scale systems, but with memristive computing making its way into commercial and open-source technology processes, the first three papers in the Special Issue bridge the gap between devices and algorithms.

In [A1], Rasetto et al. demonstrate how a three-terminal memristor can enhance the accuracy of hierarchical time-surface architectures without being affected by device stochasticity. The dynamics of the device including the short-term plasticity contributes to the higher classification accuracy.

In [A2], Hritom et al. present an optimized current-controlled memristive synapse circuit, achieving up to 82% energy savings and significant improvements in reliability and precision, and in [A3], Avedillo et al. explore how neuromorphic devices can solve NP-hard problems.

II. ANALOG- AND MIXED-SIGNAL CIRCUITS

Analog- and mixed-signal circuits play a pivotal role in neuromorphic computing and dynamical neuro-AI systems by facilitating the emulation of biological brain functions which enables hardware to process more efficient and/or realistic computational models. These circuits enhance the adaptability of neuro-AI systems, enabling them to perform complex computations with lower power consumption and lower response latencies, which can be useful in advanced cognitive and learning capabilities.

The first few papers focus on pure analog design systems, and in [A4], Liu et al. introduce a nonlinear neuron model, implemented in a small-scale CMOS chip, and mimics complex biological neural behaviors and demonstrates real-world application in controlling a robotic dog's locomotion.

In [A5], Bhattacharyya et al. introduce efficient digital approximations for simulating coupled Hodgkin–Huxley (HH) neurons, employing floating-point and fixed-point arithmetic for large SNN simulations. This implementation provides a pathway toward analog computation using biorealistic neuron models in computational and neuromorphic systems.

In [A6], Yayla et al. introduce local thresholding approximation (LTA), which significantly reduces area, energy, and latency in analog computing-based binarized neural network accelerators by efficiently utilizing analog comparators.

In [A7], Smith et al. present a novel silicon soma circuit design that combines current and voltage feedback to efficiently convert subthreshold current to pulse frequency while significantly reducing thermal sensitivity and area requirements, enabling the Braindrop neuromorphic system to be used at a high level of abstraction.

We move into the mixed-signal domain, with the paper by James et al. [A8], that incorporates synaptic stochasticity to enhance a neural network's accuracy in various classification tasks and evaluate its advantages over conventional approaches in terms of power and device variation resilience.

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In [A9], Jiang et al. present a hybrid multicore spiking neural network (SNN) chip integrating 60K ReRAM synapses and 480 digital neurons. The design achieves high synaptic density and energy efficiency, supports multiple neuron models, and demonstrates good performance in MNIST dataset recognition.

In [A10], Jiang et al. present a 40-nm RRAM compute-in-memory (CIM) accelerator for SNNs, featuring charge-pump-based leaky-integrate-and-fire neurons and a split-train-merged-inference algorithm, which enhances energy and area efficiency for intelligent edge devices.

III. Digital Design and Computer Architecture

The significance of digital design and computer architecture in neuro-AI and neuromorphic systems is profound, primarily due to the maturity of digital design flows. This maturity allows for the efficient implementation, testing, and optimization of complex neural algorithms and architectures, ensuring reliable and scalable neuromorphic systems. Digital design offers precise control and flexibility, enabling the creation of sophisticated neuro-AI models that can mimic the human brain's functionality more accurately. In [A11], Alhartomi et al. use distributed arithmetic and circulant/block-circulant matrix-vector multiplications, to optimize LSTMs in FPGA implementations.

In [A12], Ottati et al. provide an analysis of the optimal use cases, and the shortfalls, of spike-based computation in digital platforms. It concludes that static data is unlikely to be the domain where spikes will shine, due to the lack of a temporal dimension and that dynamical data and online learning are more promising avenues to explore.

In [A13], Kim et al. present an optimized processor that combines CNN and SNN achieving state-of-the-art energy efficiency on ImageNet classification. The fourth paper by Wang and Fong [A14] proposes a method to map model parameters to reduce data movement, with case studies demonstrating up to 30% faster execution in DNN benchmarks.

In [A15], Buechel et al. propose a novel programming approach for analog in-memory computing cores, utilizing gradient descent to minimize matrix–vector multiplication error, enhancing inference accuracy and eliminating the need for high-resolution ADCs.

In [A16], Aliyev et al. introduce a flexible, sparsity-aware hardware design for SNNs, along with a simulation framework, demonstrating up to 76% reduction in hardware resources and 31.25× speed increase. In [A17], Bhattacharjee et al. optimize hybrid in-memory computing devices for efficient and accurate deep neural network inference, achieving significant improvements in performance and energy efficiency over baseline models.

IV. Algorithms

At the top of the stack are the software, algorithms, and applications of neuro-AI and neuromorphic systems, where the first two papers by Azghadi et al. [A18] and Chang and Ho [A19] offer new ways to train SNNs that are optimized for energy-efficient computation.

In [A20], Jeong and Ye discover learnable activation functions optimized for digital processing, and in [A21], Srivatsav et al. leverage the AER protocol's inherent temporal features for computation.

In [A22], introduces a dynamic two-stage inference framework for brain-inspired hyperdimensional computing, effectively balancing accuracy and efficiency in IoT applications, demonstrating significant energy and time savings with minimal accuracy loss on benchmark datasets. In [A23], Jeong and Yoo present a method for training SNNs to address limited memory in neuromorphic processors, demonstrating high accuracy.

Jason K. Eshraghian, *Corresponding Guest Editor*
Department of Electrical and Computer Engineering
University of California, Santa Cruz
Santa Cruz, CA 95064 USA

Arindam Basu, *Guest Editor*
Department of Electrical Engineering
City University of Hong Kong
Hong Kong

Corey Lammie, *Guest Editor*
IBM Research - Zurich,
8803 Zurich, Switzerland

Shih-Chii Liu, *Guest Editor*
Institute of Neuroinformatics
University of Zurich and ETH Zurich
8092 Zurich, Switzerland

Priydarshini Panda, *Guest Editor*
Department of Electrical Engineering
Yale University
New Haven, CT 06520 USA

Appendix: Related Articles

[A1] M. Rasetto, Q. Wan, H. Akolkar, F. Xiong, B. Shi, and R. Benosman, "Building time-surfaces by exploiting the complex volatility of an ECRAM memristor," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 877–888, Dec. 2023.

[A2] H. Das, R. D. Febbo, C. P. Rizzo, N. N. Chakraborty, J. S. Plank, and G. S. Rose, "Optimizations for a current-controlled memristor-based neuromorphic synapse design," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 889–900, Dec. 2023.

[A3] M. J. Avedillo, M. Jiménez, C. Delacour, A. Todri-Sanial, B. Linares-Barranco, and J. Núñez, "Operating coupled VO_2-based oscillators for solving ising models," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 901–913, Dec. 2023.

[A4] K. Liu, S. Hashemkhani, J. Rubin, and R. Kubendran, "BioNN: Biomimetic neural networks on hardware using nonlinear multi-timescale mixed-feedback control for neuromodulatory bursting rhythms," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 914–926, Dec. 2023.

[A5] S. Bhattacharyya, P. R. Ayyappan, and J. O. Hasler, "Towards scalable digital modeling of networks of biorealistic silicon neurons," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 927–939, Dec. 2023.

[A6] M. Yayla, F. Frustaci, F. Spagnolo, J.-J. Chen, and H. Amrouch, "Unlocking efficiency in BNNs: Global by local thresholding for analog-based HW accelerators," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 940–955, Dec. 2023.

[A7] B. V. Benjamin, R. L. Smith, and K. A. Boahen, "A low thermal sensitivity subthreshold-current to pulse-frequency converter for neuromorphic chips," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 956–964, Dec. 2023.

[A8] V. V. Nair, C. Reghuvaran, D. John, B. Choubey, and A. James, "ESSM: Extended synaptic sampling machine with stochastic echo state neuro-memristive circuits," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 965–974, Dec. 2023.

[A9] H. Jiang et al., "Multicore spiking neuromorphic chip in 180-nm with ReRAM synapses and digital neurons," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 975–985, Dec. 2023.

[A10] J. Jiang et al., "Tempo-CIM: A RRAM compute-in-memory neuromorphic accelerator with area-efficient LIF neuron and split-train-merged-inference algorithm for edge AI application," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 986–999, Dec. 2023.

[A11] M. A. Alhartomi et al., "Low-area and low-power VLSI architectures for long short-term memory networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1000–1014, Dec. 2023.

[A12] F. Ottati et al., "To spike or not to spike: A digital hardware perspective on deep learning acceleration," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1015–1025, Dec. 2023.

[A13] S. Kim and H. J. Yoo, "C-DNN V2: Complementary deep-neural-network processor with full-adder/OR-based reduction tree and reconfigurable spatial weight reuse," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1026–1039, Dec. 2023.

[A14] Y. Wang and X. Fong, "Benchmarking DNN mapping methods for the in-memory computing accelerators," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1040–1051, Dec. 2023.

[A15] J. Büchel et al., "Programming weights to analog in-memory computing cores by direct minimization of the matrix-vector multiplication error," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1052–1061, Dec. 2023.

[A16] I. Aliyev, K. Svoboda, and T. Adegbija, "Design space exploration of sparsity-aware application-specific spiking neural network accelerators," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1062–1072, Dec. 2023.

[A17] A. Bhattacharjee, A. Moitra, and P. Panda, "HyDe: A hybrid PCM/FeFET/SRAM device-search for optimizing area and energy-efficiencies in analog IMC platforms," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1073–1082, Dec. 2023.

[A18] Z. Cai, H. R. Kalatehbali, B. Walters, M. R. Azghadi, A. Amirsoleimani, and R. Genov, "Spike timing dependent gradient for direct training of fast and efficient binarized spiking neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1083–1093, Dec. 2023.

[A19] N.-D. Ho and I.-J. Chang, "MiCE: An ANN-to-SNN conversion technique to enable high accuracy and low latency," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1094–1105, Dec. 2023.

[A20] C. Ye and D. S. Jeong, "GEBA: Gradient-error-based approximation of activation functions," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1106–1113, Dec. 2023.

[A21] R. M. Srivatsav, S. Chakrabartty, and C. S. Thakur, "Neuromorphic computing with address-event-representation using time-to-event margin propagation," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1114–1124, Dec. 2023.

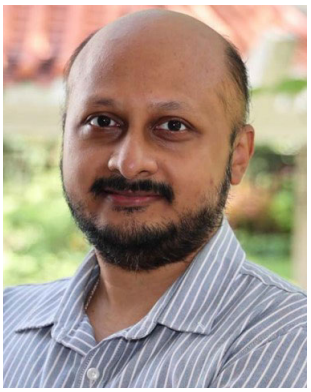
[A22] Y.-C. Chuang, C.-Y. Chang, and A.-Y. Wu, "Dynamic-HDC: A two-stage dynamic inference framework for brain-inspired hyperdimensional computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1125–1136, Dec. 2023.

[A23] D. Yoo and D. S. Jeong, "CBP-QSNN: Spiking neural networks quantized using constrained backpropagation," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 6, pp. 1137–1146, Dec. 2023.

Jason K. Eshraghian (Member, IEEE) received the B.E. degree in electrical and electronic and the Bachelor of Laws and Ph.D. degrees from The University of Western Australia, Perth, WA, Australia, in 2016 and 2019, respectively.

From 2019 to 2022, he was a Post-Doctoral Research Fellow with the University of Michigan, Ann Arbor, MI, USA. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, University of California at Santa Cruz, Santa Cruz, CA, USA. He is also a Developer of snnTorch, a widely used Python library used to train and model spiking neural networks. His research interests include neuromorphic computing, spiking neural networks, and memory circuits.

Dr. Eshraghian serves as the Secretary-Elect for the Neural Systems and Applications Technical Committee. He was awarded the 2023 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS Darlington Best Paper Award, the 2019 IEEE Very Large Scale Integration Systems Best Paper Award, the Best Paper Award from the 2019 IEEE Artificial Intelligence Circuits and Systems Conference, and the Best Live Demonstration Award from the 2020 IEEE International Conference on Electronics Circuits and Systems for his work in neuromorphic computing. He was a recipient of the Fulbright Fellowship (Australian–American Fulbright Commission), the Forrest Research Fellowship (Forrest Research Foundation), and the Endeavour Research Fellowship (Australian Government).



Arindam Basu (Senior Member, IEEE) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, in 2005, and the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2009 and 2010, respectively.

He was a tenured Associate Professor with Nanyang Technological University. He is currently a Professor with the Department of Electrical Engineering, City University of Hong Kong.

Dr. Basu is a Technical Committee Member of the IEEE CAS Societies of Biomedical Circuits and Systems, Neural Systems and Applications (Former Chair), and Sensory Systems. He received the Prime Minister of India Gold Medal from IIT Kharagpur in 2005. He received the Best Student Paper Award from the Ultrasonics Symposium in 2006, the Best Live Demonstration from ISCAS 2010, and a finalist position in the Best Student Paper Contest from ISCAS 2008. He was awarded the MIT Technology Review's TR35 Asia Pacific Award in 2012 and inducted into the Georgia Tech Alumni Association's 40 Under 40 Class of 2022. He is an Associate Editor of IEEE SENSORS JOURNAL, *Frontiers in Neuroscience*, *Neuromorphic Computing and Engineering* (IOP), and IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS. He has served as an IEEE CAS Distinguished Lecturer from 2016 to 2017.

Corey Lammie (Member, IEEE) received the bachelor's degree (Hons.) in electrical engineering, the bachelor's degree in information technology, and the Ph.D. degree in computer engineering from James Cook University (JCU) in 2018 and 2022, respectively.

He is currently a Research Scientist with IBM Research Zurich, Switzerland. His main research interests include brain-inspired computing, and the simulation and hardware implementation of spiking neural networks (SNNs) and artificial neural networks (ANNs) using RRAM devices and FPGAs. He has received several awards and fellowships, including the intensely competitive 2020–2021 IBM International Ph.D. Fellowship, the Domestic Prestige Research Training Program Scholarship (the highest paid Ph.D. scholarship in Australia), the 2020 Circuits and Systems (CAS) Society Pre-Doctoral Grant, and the 2017 Engineers Australia CN Barton Medal awarded to the Best Undergraduate Engineering Thesis at JCU. He has served as a reviewer for several IEEE journals and conferences, including IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, and the IEEE International Symposium on Circuits and Systems (ISCAS).

Shih-Chii Liu (Fellow, IEEE) received the B.Sc. degree in electrical engineering from the Massachusetts Institute of Technology, the M.Sc. degree from UCLA, and the Ph.D. degree from the Computation and Neural Systems Program, California Institute of Technology.

She is currently an Adjunct Professor with the Faculty of Science, University of Zurich. She co-directs the Sensors Group (http://sensors.ini.uzh.ch), Institute of Neuroinformatics, University of Zurich, and ETH Zürich. Her current research interests include the design of low-power low-latency asynchronous neuromorphic spiking sensors, bio-inspired computing circuits, event-driven deep neural network accelerators, and their use in neuromorphic artificial intelligent systems. Her team was awarded the 2020 Misha Mahowald Prize for Neuromorphic Engineering for their work on Hearing with Silicon Cochleas. She was an Associate Editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, the Chair of the IEEE CAS Sensory Systems and Neural Systems and Applications Technical Committees, and the General Co-Chair of the 2020 IEEE Artificial Intelligence for Circuits and Systems Conference. She is the Chair of the IEEE Swiss CAS/ED Society.

Priyadarshini Panda (Member, IEEE) received the B.E. and master's degrees from BITS, Pilani, India, in 2013, and the Ph.D. from Purdue University, USA, in 2019. During the Ph.D. degree, she interned with Intel Labs, where she developed large-scale spiking neural network algorithms for benchmarking the Loihi chip. She is currently an Assistant Professor with the Electrical Engineering Department, Yale University, USA. Her research interests lie in neuromorphic computing, spiking neural networks, energy-efficient accelerators, and in-memory computing. She is the recipient of the 2019 Amazon Research Award, 2022 Google Research Scholar Award, 2022 DARPA Riser Award, 2023 DARPA Young Faculty Award and 2023 NSF CAREER Award. She has also received the 2022 ISLPED Best Paper Award and 2022 IEEE Brain Community Best Paper Award. She has served on the technical program committees for DAC (2019–2022), DATE (2021–2023), ICCAD (2021–2023), ISLPED (2019–2023).