Guest Editorial Unconventional Computing Techniques for Emerging Technology Applications

THIS Special Issue of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS) is dedicated to the latest research advancements in unconventional computing techniques aimed at emerging technology applications.

In recent years, the volume of data generated by the Internet of Things (IoT) has surged as a result of the growing number of interconnected devices and the services they provide. However, IoT devices usually have limited computing capabilities, making it necessary to transmit large volumes of data to centralized data centers in the cloud for further processing. This leads to bandwidth bottlenecks and latency issues. Meanwhile, Artificial Intelligence (AI) has become an essential component of modern applications, with computationally demanding Machine Learning algorithms, Image Processing, and Neural Network architectures. As a result, hardware-friendly implementations for real-time processing are critical. Recent technological advances have led to a shift in data processing and storage towards IoT devices, bringing computations to the edge.

Placing hardware accelerators such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and graphic processing units (GPUs) near sensors allows for processing data directly, making tense computations feasible and reducing required communication bandwidth. However, edge computing presents its own set of challenges. Most modern real-time applications are difficult to implement in hardware using conventional computing methods due to size, low-power consumption, high-computational performance, and massive parallelism requirements. To overcome these design limitations, unconventional computing paradigms and techniques, such as approximate and stochastic computing, memristive devices, and in- and near-memory processing, are being employed.

This Special Issue presents latest developments in the interdisciplinary field of unconventional computing, focusing on the following three general topics.

1) *Novel Techniques and Approaches in Unconventional Computing*—emphasizing on emerging applications.
2) *Circuits, Systems, and Architectures for Approximate and Stochastic Computing*—exploring new architectures to exploit the unique properties of their class.
3) *In- and Near-Memory Processing with an emphasis on Memristive Devices Utilization*—exploring in- and near-memory processing techniques along with the applicability of memristive devices.

After a rigorous peer-review process, 36 articles were selected to comprehensively cover the latest research progress in unconventional computing techniques and approaches for emerging technology applications. Each article is categorized based on the three general topics of the Special Issue and given a brief introduction.

I. Novel Techniques and Approaches in Unconventional Computing

The scientific contributions in the first group are focused on new techniques and approaches in unconventional computing, covering a wide range of areas and levels of integration within the field of circuits and systems. The group is comprised of 12 articles which are briefly summarized below.

In [A1], Luo et al. introduce a novel column stationary dataflow that optimizes the local data reuse of filter weights and feature maps in Convolutional Neural Networks (CNNs). Their approach involves using a reconfigurable spatial architecture to map multiple convolution kernels in parallel to the processing engines (PEs) array.

In [A2], Chang et al. present an Energy-aware Unified Pruning Quantization (E-UPQ) mechanism, a novel framework for automated compression (pruning + quantization) of CNNs while considering the energy-accuracy trade-off.

In [A3], Dave et al. investigate how principles from approximate computing can be effectively employed to further optimize Binary Neural Networks (BNNs). They demonstrate that HW/SW co-design, in which BNNs are either proactively trained in the presence of approximation-induced errors and/or augmented with an appropriate error-mitigation scheme, is a key to realize energy-efficient yet robust BNNs.

In [A4], Liu et. al. propose a novel and efficient way for image processing which exploits the features of DRAM and SRAM. The proposed strategy first approximates and encodes the image to effectively reduce the number of logic 1s in the original pixel data, pushes the processed data into the off-chip DRAM, and then writes into the on-chip SRAM for further computation.

In [A5], Yao proposes a novel technique that utilizes the Game-of-Life (GoL) concept from cellular automata to achieve a lightweight, yet effective temperature-aware Dynamic

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Voltage/Frequency Scaling (DVFS) for tile-based Chip Many-Core Processors (CMPs).

In [A6], Yao proposes a Symbolic-Execution CNN (SE-CNN), which breaks data dependence between CNN layers via value prediction. The SE-CNN works in two successive phases: A parallel computation phase and a serial correction phase, based on the concept that in post-trained CNNs, less than 10% of neurons are activated to identify patterns in inputs.

In [A7], Abreu et al. employ the body biasing feature, available in fully depleted silicon-on-insulator (FDSOI) technology nodes to build CMOS-compatible compact majority (MAJ) and minority (MIN) logic gates. Compared to their CMOS counterpart, the proposed MAJ/MIN gates have considerably fewer transistors, 2.3× and 2×, respectively.

In [A8], Karimi et al. present a novel spiking neuromorphic architecture based on charge-trap transistors (CTTs). The proposed low-power scalable architecture targets large neural network applications, such as machine learning tasks and emulation of brain connectivity networks.

In [A9], Shin et al. present a hardware-aware stochastic simulated annealing (HA-SSA) algorithm that reduces the memory usage of storing intermediate results while maintaining the computing speed of SSA. For evaluation purposes, the proposed algorithm is compared to conventional SSA and SA approaches on maximum cut combinatorial optimization problems.

In [A10], Chang et al. present a comprehensive study of recent developments improving the accuracy-efficiency trade-off of Brain-inspired Hyperdimensional Computing (HDC), covering both algorithm and hardware-level approaches. Unlike mainstream NNs, HDC offers a fast-training strategy and an energy-efficient inference mechanism by computing in high-dimensional spaces with high parallelism.

In [A11], Guirado et al. propose a scale-out HDC architecture called WHYPE, which uses wireless in-package communication technology to interconnect a large number of physically distributed In-Memory Computing cores that either encode hypervectors or perform multiple similarity searches in parallel.

In [A12], Ahmed et al. propose Binary Bayesian NNs with an end-to-end approach from algorithmic level to device level for their implementation. The proposed approach uses the inherent stochastic properties of Magnetic Tunnel Junctions (MTJ), a class of non-volatile memories, as a feature to implement Dropout-based Bayesian Neural Networks.

II. Circuits, Systems and Architectures for Approximate and Stochastic Computing

Approximate and stochastic computing have emerged as promising approaches in error-tolerant and hardware-intensive applications, offering significant area, power, and energy savings compared to traditional binary computing. This group of 12 articles focuses on novel circuits, systems, and architectures.

In [A13], Mohanty has conducted a comprehensive analysis of radix-64 and radix-256 encoding for 4-bit and 5-bit approximations. Drawing from this research, the study proposes a two-term radix-64 and a three-term radix-256 encoding for 4-bit approximation, which enables the calculation of partial-products with the lowest maximum absolute error.

In [A14], Fatemieh et al. combine the concept of In-Memory Computation (IMC) with memristors to build four serial Material Implication (IMPLY)-based approximate full adders. The proposed circuits have a reduced number of calculation steps and improved energy consumption compared to existing exact full adders.

In [A15], Yan et al. propose two novel Processing Element (PE) units for Successive-Cancellation (SC) decoders. These PEs are equipped with an approximate comparator and adder–subtractor, which significantly improve the hardware efficiency of SC decoders without compromising on the bit error-rate (BER) performance.

In [A16], Zhang and Ko present a solution to the challenge of implementing Posit arithmetic in minimal hardware by proposing Posit multipliers that incorporate approximate computing features. The proposed designs truncate the fraction multiplier according to the estimated fraction bit-width of the product so that the resource consumption of the fraction multiplier and thus the fraction adder can be significantly reduced.

In [A17], Pinos et al. propose TFApprox4IL, a software library supporting both symmetric as well as asymmetric quantization modes, approximate 8×N bit multipliers emulated using lookup tables, a new type of approximate layer known as approximate depth-wise convolution, and quantization-aware training. The TFApprox4IL performance is extensively evaluated in the simulation of approximate implementations of MobileNetV2 and ResNet networks.

In [A18], Tabrizchi et al. present the AppCiP architecture, a novel approach that integrates sensing and computing to enable efficient AI on resource-limited sensing devices. By integrating the sensing and computing processes, the AppCiP architecture can significantly reduce the energy consumption and processing time required for AI tasks on these devices.

In [A19], Fan et al. propose a timing-aware configurable adder (TACA) to achieve a good trade-off between energy efficiency and accuracy at low operating voltages. This design relies on the functions of timing-error detection and correction (TEDC) for the newly proposed accuracy-configurable full adders (ACFAs).

In [A20], Rosselló et al. propose an innovative approach to enhance neural network (NN) hardware implementation by combining Stochastic Computing (SC) with Morphological Neural Networks (MNN). The main objective of this approach is to leverage the inherent pruning capability of morphological neurons to significantly reduce the hardware resources required for NN implementation, resulting in a more compact network.

In [A21], Móran et al. propose a novel hardware implementation of a Radial Basis Function Neural Network (RBF-NN) using Stochastic Computing (SC), which employs probabilistic principles in place of traditional digital gates. Moreover, several complex function designs to implement RBF-NNs are presented and theoretically analyzed. The proposed methodology enables the implementation of massively parallel large-scale RBF-NNs with reduced hardware requirements.

In [A22], Tang et al. propose two Delta Sigma Modulator (DSM)-based stochastic dividers. The first one significantly reduces the additional clock cycles needed for division and slightly increases the accuracy. The second one is a second-order DSM and achieves higher division accuracy without requiring additional clock cycles, at the cost of a minor hardware overhead. SC-based neural networks are implemented as a case study to evaluate the advantages of the proposed architectures.

In [A23], Temenos et al. introduce a stochastic computing adder (SC) architecture based on sigma-delta (SD) modulation. The SCSD's single-bit output enables the connection to existing Stochastic Finite-State Machines realizing non-linear functions and the formation of cascade processing structures appropriate for efficient realizations of SC artificial neurons. To demonstrate the proposed adder's efficacy, a SCSD adder-based neuron was designed and used as a building block of a SCSD Multi-Layer Perceptron (MLP).

In [A24], Schober et al. have developed a functional sound-source localizer by implementing a sound-source localization algorithm in the stochastic domain. The proposed SC design requires about 40% less area than the conventional binary design. In addition, the authors propose a new cross-correlation (CC) design based on Sobol bitstreams for further area and power saving.

III. In- and Near-Memory Processing With an Emphasis on Memristive Devices Utilization

The 12 articles of the third group of this Special Issue concentrate on the latest advancements in in- and near-memory processing techniques, with a particular emphasis on those utilizing memristive devices.

In [A25], Kumar et al. demonstrate bias-scalable approximate analog computing circuits using the generalization of the margin-propagation principle called shape-based analog computing. They provide evidence of the robustness of their computing modules to variations in transistor biasing and temperature by analyzing the results obtained from prototypes fabricated in a 180-nm CMOS process.

In [A26], Tran and Teuscher propose a novel approach to utilizing cluster networks as memcapacitive reservoirs, enabling them to carry out multiple tasks concurrently. This is a marked departure from traditional memcapacitive reservoirs, which are typically limited to performing a single task. The experimental findings demonstrate that cluster networks outperformed both crossbar and small-world power-law networks across three distinct tasks: Isolated Spoken Digits, MNIST, and CIFAR-10.

In [A27], Zhang et al. introduce Aligner-D, a DRAM-based energy-efficient and high-throughput Processing-in-Memory (PIM) accelerator designed to efficiently execute the Burrows-Wheeler Transformation alignment algorithm for DNA short-read alignment.

In [A28], Xiao et al. propose a circuit implementation scheme for a memristor-based lightweight transformer network. This approach aims to address the computational complexity associated with the large number of multiplications and additions required in traditional Transformer Networks. To showcase the efficacy of their method, the researchers implemented a speech recognition task utilizing a speech command dataset and employing a modular hardware design approach.

In [A29], Korkmaz et al. introduce an analog circuit designed to accelerate the Power Iteration algorithm, which incorporates a normalization circuit and current-mode termination for the memristor crossbars. The authors have integrated transistor level peripheral circuitry around the memristor crossbar and factored in non-idealities, such as wire parasitics, source driver resistance, and finite memristor precision, to improve the circuit's performance.

In [A30], Chang and Chen have created an in-memory Boolean computing architecture based on SRAM. Additionally, they introduce a new multi-logic sense amplifier (MLSA) design, which is an enhancement over conventional ones. The proposed design can generate multiple logical outputs with a lower compute delay, lower power consumption, and less transistor count.

In [A31], Yousuf et. al. employ Jump Tables to simulate emerging memory devices for neural networks. This study examines their accuracy and impact on network performance using two models - binning and Optuna-optimized binning. Bin-based models can produce unpredictable results at low data points, affecting network accuracy. Proposed device-level metrics can assess modeling bias for future investigations.

In [A32], Antolini et al. combine hardware and software concepts to mitigate the impact of Phase Change Memory non-idealities for analog In-memory Computing systems. A model of the behavior of PCM cells is employed to develop a device aware training for DNNs and the accuracy is evaluated in a CIFAR-10 classification task.

In [A33], Garzón et al. propose AM^4, a combination of spin-transfer torque magnetic tunnel junction (STT-MTJ)-based Content Addressable Memory (CAM), Ternary CAM (TCAM), approximate matching (similarity search) CAM (ACAM), and in-memory Associative Processor (AP) design, inspired by the recently announced Samsung MRAM crossbar.

In [A34], Lu et al. propose scalable in-memory annealers to solve the large-scale travelling salesman problem (TSP) with crossbar arrays of FinFET-.based charge trap transistors. The intrinsic temporal noise of the drain current caused by trapping/detrapping is used to realize the annealing process.

In [A35], Khan et al. propose a Programmed Analog Weights for Nonlinearity (PAWN) method to update the conductance of a memristor by following the nonlinear curve during the training in a neuromorphic system. The experimental results demonstrate the effectiveness of the PAWN method in mitigating the impact of nonlinearity on memristors under various Long-Term Potentiation and Long-Term Depression conditions.

In [A36], Kavitha et al. propose an SRAM compute cache with a sense amplifier (SA) based approach to perform in-/near memory Boolean computations with a novel reconfigurable assist sense amplifier (RASA). The RASA exploits assist tran-

sistors to achieve NAND, NOR, and XNOR operations without affecting the transparency of normal read.

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APPENDIX: RELATED ARTICLES

[A1] L. Luo et al., "A reconfigurable spatial architecture for energy-efficient inception neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243619.

[A2] C.-Y. Chang, K.-C. Chou, Y.-C. Chuang, and A.-Y. Wu, "E-UPQ: Energy-aware unified pruning-quantization framework for CIM architecture," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3242761.

[A3] A. Dave, F. Frustaci, F. Spagnolo, M. Yayla, J.-J. Chen, and H. Amrouch, "HW/SW codesign for approximation-aware binary neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243267.

[A4] M. Liu et al., "A selective bit dropping and encoding co-strategy in image processing for low-power design in DRAM and SRAM," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3234402.

[A5] Y. Yao, "Game-of-life temperature-aware DVFS strategy for tile-based chip many-core processor," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3244763.

[A6] Y. Yao, "SE-CNN: Convolution neural network acceleration via symbolic value prediction," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3244767.

[A7] B. A. Abreu et al., "Compact CMOS-compatible majority gate using body biasing in FDSOI technology," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243150.

[A8] M. Karimi, A. S. Monir, R. Mohammadrezaee, and B. Vaisband, "CTT-based scalable neuromorphic architecture," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3244775.

[A9] D. Shin, N. Onizawa, W. J. Gross, and T. Hanyu, "Memory-efficient FPGA implementation of stochastic simulated annealing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243260.

[A10] C.-Y. Chang, Y.-C. Chuang, C.-T. Huang, and A.-Y. Wu, "Recent progress and development of hyperdimensional computing (HDC) for edge intelligence," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3242767.

[A11] R. Guirado, A. Rahimi, G. Karunaratne, E. Alarcón, A. Sebastian, and S. Abadal, "WHYPE: A scale-out architecture with wireless over-the-air majority for scalable in-memory hyperdimensional computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243064.

[A12] S. T. Ahmed, K. Danouchi, C. Münch, G. Prenat, L. Anghel, and M. B. Tahoori, "SpinDrop: Dropout-based Bayesian binary neural networks with spintronic implementation," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3242146.

[A13] B. K. Mohanty, "Efficient approximate multiplier design based on hybrid higher radix booth encoding," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2022.3229831.

[A14] S. E. Fatemieh, M. R. Reshadinezhad, and N. TaheriNejad, "Fast and compact serial IMPLY-based approximate full adders applied in image processing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1.

[A15] C. Yan, Y. Cui, K. Chen, B. Wu, and W. Liu, "Hardware efficient successive-cancellation polar decoders using approximate computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3241012.

[A16] H. Zhang and S.-B. Ko, "Efficient approximate posit multipliers for deep learning computation," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2022.3231642.

[A17] M. Pinos, V. Mrazek, F. Vaverka, Z. Vasicek, and L. Sekanina, "Acceleration techniques for automated design of approximate convolutional neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3235204.

[A18] S. Tabrizchi, A. Nezhadi, S. Angizi, and A. Roohi, "AppCiP: Energy-efficient approximate convolution-in-pixel scheme for neural network acceleration," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3242167.

[A19] X. Fan, T. Zhang, H. Liu, S. Lu, and J. Han, "A timing-aware configurable adder based on timing detection for low-voltage computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243135.

[A20] J. L. Rosselló et al., "Highly optimized hardware morphological neural network through stochastic computing and tropical pruning," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2022.3226292.

[A21] A. Móran, L. Parrilla, M. Roca, J. Font-Rosselló, E. Isern, and V. Canals, "Digital implementation of radial basis function neural networks based on stochastic computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2022.3231708.

[A22] X. Tang et al., "Delta sigma modulator-based dividers for accurate and low latency stochastic computing systems," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3244183.

[A23] N. Temenos and P. P. Sotiriadis, "A stochastic computing sigma-delta adder architecture for efficient neural network design," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243950.

[A24] P. Schober, S. N. Estiri, S. Aygun, A. H. Jalilvand, M. H. Najafi, and N. TaheriNejad, "Stochastic computing design and implementation of a sound source localization system," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243604.

[A25] P. Kumar, A. Nandi, S. Chakrabartty, and C. S. Thakur, "Bias-scalable near-memory CMOS analog processor for machine learning," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3234570.

[A26] D. Tran and C. Teuscher, "Multi-tasking memcapacitive networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3235242.

[A27] F. Zhang, S. Angizi, J. Sun, W. Zhang, and D. Fan, "Aligner-D: Leveraging in-DRAM computing to accelerate DNA short read alignment," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3241545.

[A28] H. Xiao, Y. Zhou, T. Gao, S. Duan, G. Chen, and X. Hu, "Memristor-based light-weight transformer circuit implementation for speech recognizing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3237582.

[A29] A. Korkmaz et al., "Spectral ranking in complex networks using memristor crossbars," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3237836.

[A30] Y.-J. Chang and S.-H. Chen, "Multi-logic sense amplifier (MLSA) design for in-memory computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243434.

[A31] O. Yousuf, I. Hossen, M. W. Daniels, M. Lueker-Boden, A. Dienstfrey, and G. C. Adam, "Device modeling bias in ReRAM-based neural network simulations," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3238295.

[A32] A. Antolini et al., "Combined HW/SW drift and variability mitigation for PCM-based analog in-memory computing for neural network applications," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3241750.

[A33] E. Garzón, M. Lanuzza, A. Teman, and L. Yavits, "AM^4: MRAM crossbar based CAM/TCAM/ACAM/AP for in-memory computing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243222.

[A34] A. Lu et al., "Scalable in-memory clustered annealer with temporal noise of charge trap transistor for large scale travelling salesman problems," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3244485.

[A35] S. A. Khan, M. Oli-Uz-Zaman, and J. Wang, "PAWN: Programmed analog weights for non-linearity optimization in memristor-based neuromorphic computing system," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3235658.

[A36] S. Kavitha, S. K. Vishvakarma, and B. S. Reniwal, "Enabling energy-efficient in-memory computing with robust assist-based reconfigurable sense amplifier in SRAM array," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 1, doi: 10.1109/JETCAS.2023.3243192.

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