Hybrid Pixels With Si Photodiode and 4H-SiC MOSFETs Using Direct Heterogeneous Bonding Toward Radiation Hardened CMOS Image Sensors

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***Abstract*— For radiation hardened image sensors, a Silicon-On-Insulator (SOI) -Si/ 4H-SiC hybrid pixel device was developed. The hybrid pixel device consists of one Si photodiode and three 4H-SiC nMOSFETs. At fabrication, SOI substrate was directly bonded on 4H-SiC substrate via SiO_2. After bonding, the base silicon substrate and Buried Oxide (BOX) were removed by TMAH wet-etching. By using this SOI-Si/ 4H-SiC substrate, the SOI-Si photodiodes and 4H-SiC nMOSFETs were integrated in the same substrate. As a result, a response of the SOI-Si/ 4H-SiC hybrid pixel device to light illumination was successfully demonstrated.**

***Index Terms*— 4H-SiC, MOSFETs, image sensor, wafer bonding, photodiode.**

I. Introduction

HARSH environment electronics have been required for developing new frontiers like space, deep underground, high energy physics, and nuclear science. In addition, radiation resistant electronics have been required for the decommissioning of nuclear power stations, e.g., for the Fukushima Daiichi nuclear power station accident. So far, for such decommissioning operations robots have been utilized, however the available time for operation is limited by the electronics particular image sensors. The typical radiation hardness of Si electronics is 0.2 kGy owing to the total ionization effects on Si MOSFETs [1]. For developing radiation hardened electronics, we need to introduce radiation hardened transistors.

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4H-SiC (Silicon Carbide) is a wide bandgap semiconductor and has excellent properties for harsh environment applications. Thus, 4H-SiC has a wide bandgap of 3.26 eV with a very low intrinsic carrier density. This can be applied to high temperature applications. In addition, 4H-SiC has high atomic displacement threshold energy [2], and high radiation ionization energy for electron-hole pair creation [3]. These properties mean SiC crystal has a hardness to radiation and has potential for electronic devices with low soft errors. Operation of 4H-SiC bipolar junction transistors (BJTs), junction field effect transistors (JFETs), and metal-oxide-semiconductor transistors (MOSFETs) have been demonstrated in high temperature environments [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. In terms of the image sensor, 4H-SiC has already demonstrated operation as a UV imaging system with 256 pixels at 400°C [15]. However, 4H-SiC does not have sufficient absorbance at visible light [16]. For a pixel device in a conventional Si CMOS image sensor, Si MOSFETs used as the reset (RST), source follower (SF), and row selector (RS) are more sensitive and vulnerable to radiation than Si photodiodes (PD). Therefore a combination of SiC MOSFET and Si PD would be a candidate for a pixel device using radiation-hardened CMOS image sensors.

We have already demonstrated total ionizing dose effect (TID) resistance of 4H-SiC MOSFETs and some reports also showed that the MOSFETs work even after high irradiation doses exceeding 100 Mrad [12, [13], [14]. The thick embedded oxide film makes SOI devices relatively vulnerable to TID, however, we suggest that TID effects can be reduced by thinning the BOX layer to the same thickness as the gate oxide film. Takeuchi *et al.* reported that in the case of discrete Si-PD, dark current was within the acceptable range even after gamma irradiation with a dose of 1000 kGy [17].

In this work, SOI-Si PD and 4H-SiC MOSFETs were integrated by applying direct bonding of SOI and 4H-SiC substrates, and the fabrication and optical response of the SOI-Si/ 4H-SiC hybrid pixel device for radiation hardened image sensors were demonstrated.

II. Experiment

The pixel device of the CMOS image sensor consists of one photodiode and three MOSFETs. For the hybrid pixel devices, 4H-SiC n-type MOSFETs were applied as the RST,

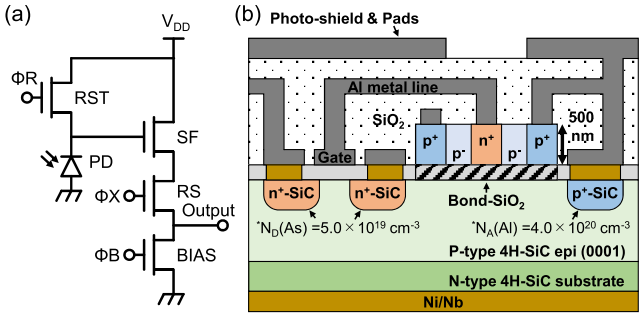

Fig. 1. 1-pixel device: (a) circuit of the pixel device, which consist of 1 photodiode and 3 MOSFETs; (b) cross sectional schematics of the SOI-Si/ 4H-SiC hybrid pixel device.

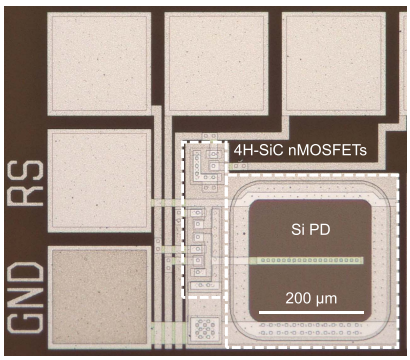

Fig. 2. Microphotograph of the fabricated 1-pixel device.

SF, RS and BIAS transistors. The pixel device was designed based on the characteristics of the 4H-SiC nMOSFETs [12]. The pixel device circuits with the nMOSFETs are shown in Fig. 1 (a).

By light irradiation on this device, electrons as the negative carriers from the Si photodiode are stored in the SF's gate electrode as the capacitor, and by applying voltage on the gate of the RS transistor, the signal corresponding to the stored charges is observed as the output voltage. After sensing the output voltage, by applying gate voltage on the RST transistor, we could reset the charges in PD and SF's gate electrode.

In Fig. 1 (b), a cross-sectional schematic of the SOI-Si/ 4H-SiC hybrid pixel device is shown. On the 4H-SiC substrate, the Si photodiode is integrated in the same substrate. The ideal Si photodiode is made from Si single crystal, then SOI substrate is bonded directly to the 4H-SiC substrate. By removing the base Si substrate and BOX layer of the SOI wafer, a SOI-Si active layer remained on the 4H-SiC substrate. By using the bonded SOI-Si/ 4H-SiC substrate, the hybrid pixel devices were fabricated.

The fabrication process of the SOI-Si/ 4H-SiC hybrid pixel device is as follows. The 4H-SiC nMOSFETs were fabricated on 4H-SiC (0001) 4° p-type epitaxial substrate. First, Arsenic (As) and Aluminum (Al) ions were implanted in the substrate, and the substrate was annealed at a temperature of 1700°C for impurity activation. After impurity activation, thermal oxide was formed at a temperature of 1150°C for the wafer bonding process.

Silicon PDs were fabricated with SOI substrate with a 500 nm Si (100) active layer. The 4H-SiC wafer with a 20 nm SiO_2 bonding layer and the SOI wafer were cleaned in RCA SC-1 (NH_3:H_2O_2:H_2O) solution, and the wafers were bonded. The thick Si handle substrate of the SOI was removed using a wet-etching process.

Subsequently, at the outside of the Si PD regions, BOX layer, Si active layer, and bonding interfacial thermal oxide layer were removed using a wet-etching process. The size of the SOI-Si PDs was 300 μm × 300 μm. A 20 nm gate oxide layer was formed on the 4H-SiC surface with dry oxidation at 1150°C. Subsequently, BOX layer on the SOI-Si PDs was removed. As a result, an SOI-Si (100) layer of 500 nm thickness was formed on the 4H-SiC epitaxial substrate with S/D regions and the gate oxide layer. On the SOI-Si, n+ and p+ regions were form by ion-implantation.

In the thermal oxide on the 4H-SiC, contact-vias to S/D regions were formed, and Nb/Ni thin films were deposited by sputtering. The sample was annealed at a temperature of 930°C in N_2 ambient for 5 minutes. After silicidation, contact-vias to SOI-Si PDs were formed. Subsequently, an Al metal layer was formed by sputtering and was patterned with a lithography process and Al etching process. After forming the Al metal layer, SiO_2 interlayer dielectric film was formed with atmospheric pressure chemical vapor deposition (APCVD).

III. Results and Discussion

A. Device Structure

Figure 2 shows the micrograph of the hybrid pixel devices with the integration of SOI-Si PDs and 4H-SiC nMOSFETs. The typical feature size of SOI-Si PDs was 300 μm × 300 μm and the feature size of 4H-SiC nMOSFETs was channel length/width = 10 μm /10 μm.

The SOI-Si active layer had a resistivity of 8 Ω·cm to 12 Ω·cm, and in the photosensitive area we didn't apply additional doping. The SOI-Si thickness was limited to 500 nm in this study because of the step coverage of the Al interconnects and the etching process of the SOI-Si layer. A lateral junction structure was used for the photodiode in the pixel to achieve sufficient quantum efficiency values with a thin Si film. Inside the photodiode, n+ regions with a width of 5 μm were patterned in stripes. As a result, 28 line PN junctions were formed. The total PN junctions width is 5.8 mm.

A square Al metal line was formed around the SOI-Si photodiode. This metal line was connected to the GND metal pad electrode through a p+-SiC body contact. The Al metal line in the center of the SOI-Si photodiode was connected to the n+-Si region of the SOI-Si photodiode. This metal line was extended to the 4H-SiC SF transistor and was directly connected to the gate electrode of the SF transistor.

These metal lines and gate electrodes were formed in the lower Al first layer. The gate electrodes of the RS MOSFET, RST MOSFET and BIAS MOSFET were also formed in the same Al layer.

B. SOI-Si photodiodes and 4H-SiC nMOSFETs

The current-voltage characteristics of the photodiode in the dark condition are shown in Fig. 3. The ideality factor indicating the quality of the PN junction is 1.5 at a cathode voltage of −0.55 V, suggesting that the Si layer contains defect levels that contribute to the diffusion current. During device fabrication, several thermal processes after wafer bonding may cause serious defect formation in the bulk. The ideality factor value suggests that some defects are formed in the photodiode, both at the interface and in the bulk, but under sufficient light

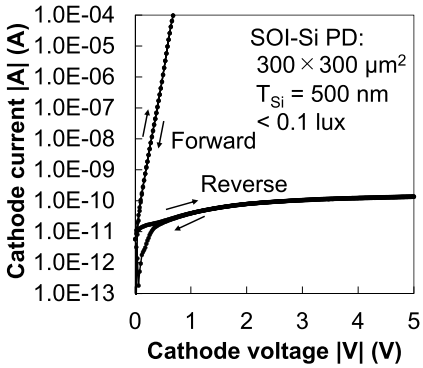

Fig. 3. Typical current-voltage characteristics of SOI-Si PD on 4H-SiC substrate.

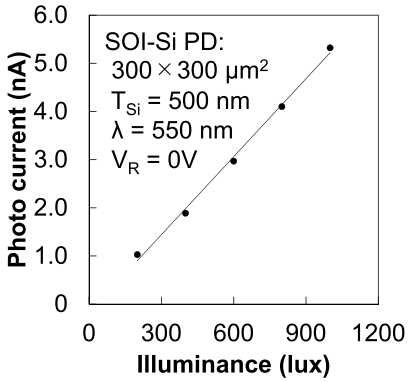

Fig. 4. Photocurrent of the SOI-Si PD ($\lambda = 550$ nm).

intensity, the photodiodes in this study are expected to work as photosensitive devices.

Figure 4 shows the visible-light illumination response characteristics of SOI-Si PDs. The size of the measured PD is 300 μm × 300 μm, which is the same size as the one in the pixel device. This graph shows the photocurrent of the PD against the light intensity at the visible wavelength of 550 nm, and shows a linear characteristic in the range of light intensity from 200 to 1000 lux. The PD showed quantum efficiencies of 62%, 24%, and 19% for blue light (450 nm), green light (550 nm), and red light (600 nm), respectively.

This PD took its peak efficiency at 450 nm. At the wavelength, the incident light's penetration depth becomes of the same order as the SOI-Si PD's thickness.

The threshold voltage of the 4H-SiC nMOSFET in the same chip as the pixel devices was 4.8 V, and field effect mobility was 3.1 cm^2/Vs. The high threshold voltage of MOSFETs is due to the manufacturing process for high temperature tolerance above 200°C.

C. Pixel Devices

Figure 5 shows pixel output characteristics. In the RST MOSFET, a rectangular voltage of $V_{Hi} = 10$ V and $V_{Low} = 0$ V was applied to the gate electrode for resetting the Si photodiode carriers and the gate electrode of the SF transistor. Frequency of the RST signal was set to 60 Hz. The output voltage swing increased with the illuminance, and saturated at 800 lux.

The output electrode of the pixel was connected to a oscilloscope via a probe needle and coaxial cable, and buffer amplifier was not used. Therefore, by the measurement setup,

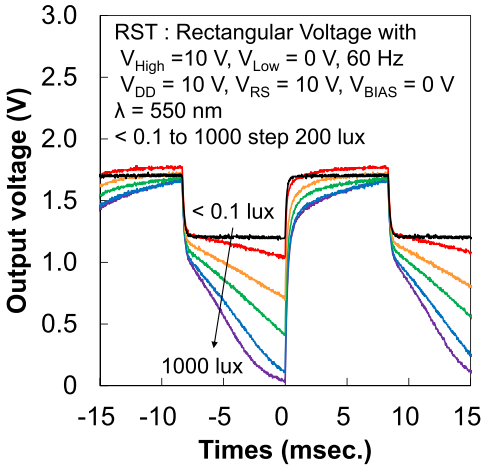

Fig. 5. Output characteristics of the fabricated 1-pixel device at the condition of RST voltage frequency 60 Hz.

the parasitic capacitance and impedance of the pixel's load were approximately 300 pF and 1 MΩ, respectively. The parasitic capacitance induced transient effect at the reset operation.

The maximum swing of the output voltage was limited by the voltage drop (0.5 V) at the PD node immediately after the reset operation. This voltage drop (reset feedthrough) is due to the ratio of the gate-to-source overlap capacitance of the RST MOSFET to the PD node capacitance, which is estimated to be about 5% assuming an SF gain value 1 [18]. The value is one order of magnitude higher than the designed value. As for the PD capacitance, the cause of the capacitance mismatch was considered to be the presence of a low concentration carrier layer in the Si film at the bonding oxide film interface, or an unexpected drop in capacitance due to the growth of the bonding oxide layer. ∗-

The saturation of the output voltage swing is determined by the threshold voltage of the SF MOSFETs as well as the PD node capacitance. The MOSFETs in this study has its threshold voltage at approximately half of VDD, so this effect is expected to be significant.

IV. Conclusion

We developed a SOI-Si/ 4H-SiC hybrid pixel device, in which a Si photodiode and a 4H-SiC MOSFET are integrated on a single chip by direct heterojunction of SOI and 4H-SiC substrates. In the pixel part, the relationship between the irradiance and the output voltage swing at 550 nm visible light wavelength is shown. In SOI-Si PDs, the linear characteristics, its irradiance range, and quantum efficiency at 550 nm visible light wavelength are shown. The operation of the pixel was examined at an operating frequency of 60 Hz. The reset period should be kept small enough compared to the integration period. This 60 Hz operating speed remains a challenge. However, we have successfully demonstrated the reset and integration operation of the pixel and shown its feasibility. By employing a preamplifier in the output stage of the pixel or pixel array, a higher operating frequency is expected to be achieved.

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