A 3D Vertical-Channel Ferroelectric/Anti-Ferroelectric FET With Indium Oxide

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***Abstract*— A vertical channel ferroelectric-FET (FeFET) with HfO_2-based ferroelectric (Fe-HfO_2) and atomic layer deposition (ALD) Indium oxide (InOx) channel has been developed and demonstrated for 3D high-density memory applications. Reliable memory operation has been confirmed with memory window (MW) >1V in gate length (L_g) = 50nm short channel FeFETs. Polar-axis transition of Fe-HfO_2 from in-plane in the initial film to out-of-plane after electrical cycling has been verified by both experimental and theoretical studies. A vertical channel anti-ferroelectric (AFe) FET (AFeFET) with ZrO_2 has been also demonstrated by making use of half-loop hysteresis in AFe, which can be a new solution for the weak erase problem seen in oxide semiconductor channel FeFETs.**

***Index Terms*— Ferroelectrics, hafnium zirconium oxide, ferroelectric memory, FeFET, endurance, retention.**

I. Introduction

FERROELECTRIC FET (FeFET) is a promising candidate for high density memory with high-speed and low-power operation due to its field-driven write operation. Since the discovery of HfO_2–based ferroelectric (Fe-HfO_2), FeFET has attracted much attention because of its CMOS-compatibility [1]. Moreover, 3D vertical-channel FeFET has the potential for high-density storage memory [2]. For 3D vertical-channel FeFET, compared to poly-Si, oxide semiconductor (OS) has potential benefits as a channel material, such as high mobility and no low-k interfacial layer between Fe-HfO_2 and OS layers [3]–[7]. However, while program operation can be easily done due to the high majority carrier concentration in OS, erase operation is weak due to the low minority carrier concentration in OS.

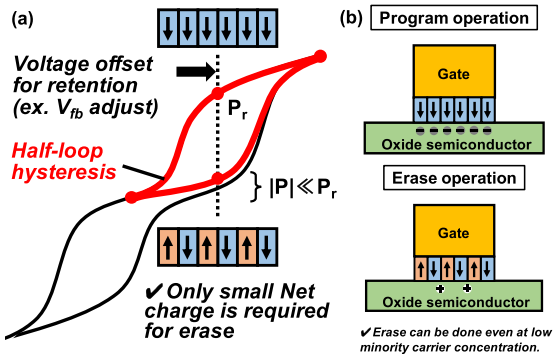

Fig. 1. (a) Half-loop hysteresis in AFe can be used to improve erase operation with small net charge. (b) Program and erase operations in AFe-FET that can achieve efficient erase operation with low minority carrier concentration.

Previous works theoretically and experimentally show that shorter gate length (L_g) and thinner channel help to mitigate the weak erase issue by enhancing the electric field in the Fe-HfO_2 layer [8]–[10]. For 3D vertical channel FeFETs, OS channel material should be conformally deposited by atomic layer deposition (ALD) in a high-aspect ratio trench structure [11]–[14]. In addition, 3D FeFETs demand out-of-plane polarization of Fe-HfO_2 with respect to any type of surface in the 3D structure. Anti-ferroelectric (AFe) gate insulator is another approach instead of Fe-HfO_2 and used for planar AFeFET [15]–[19]. We think that AFeFET is a practical approach because the use of half-loop hysteresis only requires small net charge in anti-parallel polarization and thus low carrier concentration for erase operation, but has not been demonstrated in 3D vertical structure yet (Fig. 1).

Based on the motivations above, in this study, (1) we develop and demonstrate a vertical channel FeFET/AFeFET with ALD indium oxide (InOx) channel at L_g = 50nm for high-density memory, (2) experimentally and theoretically investigate the polar-axis transition of FE-HfO_2 under the electric field.

II. Device Fabrication

The device fabrication process for the proof-of-concept starts from SOI substrate. L_g = 50nm N^+ Si gate was formed by ion-implantation, thermal activation, and SOI thinning. A trench was formed by EB lithography and RIE, followed

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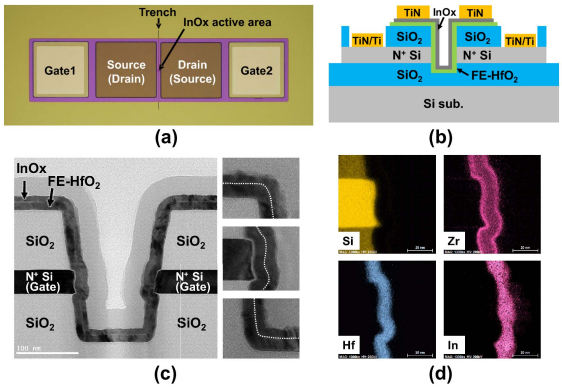

Fig. 2. (a) Top-down microscope image for a single device. (b) Cross-sectional schematic for a single device. (c) Cross-sectional TEM images of the vertical channel FeFET with ALD InOx. (d) EDX elemental mapping of the vertical channel FeFET at the region of gate, Fe-HfO_2, and InOx channel.

by gate isolation RIE. 1nm ZrO_2/10nm $HfZrO_2$/1nm ZrO_2 and 12nm ZrO_2 were grown by ALD at 250°C for FeFETs and for AFeFETs, respectively. Crystallization anneal was done at 600°C by RTA. 5nm InOx was grown by ALD at 200°C and patterned. O_3 anneal was applied at 200°C to reduce oxygen vacancy [20]. S/D metal contacts were formed with 20nm TiN. Gate contact was formed with 5nm Ti and 20nm TiN.

Fig. 2(a) shows the top-down microscope image and Fig. 2(b) shows the cross-section schematic of a single device that contains two FETs in series, sharing source and drain. One FET is kept turned on while the other is in measurement. Fig. 2(c) and (d) show the cross-sectional TEM images and EDX elemental mapping of the fabricated vertical-channel FeFET, respectively. Conformal and uniform formation of the gate insulator and the channel is confirmed thanks to the ALD process. Note that the parasitic resistance is large between gate and source/drain in this work because of the N^+ Si resistance and patterning process limitation, which limits write pulse width $\sim 100\mu s$ but can be improved in the future work.

III. Results and Discussion

First, we show and discuss the results of the fabricated vertical channel FeFETs. Before FeFET characteristics, ferroelectricity was examined in a Fe-HfO_2 capacitor with the same Fe-HfO_2 layer as the FeFET, and N^+ Si and TiN electrodes. Fig. 3(a) shows the measured polarization charge (Q) – voltage (V) curves and Fig. 3 (b) shows the measured current (I) - V curves. As the voltage amplitude increases from 3V to 5V, the ferroelectric hysteresis approaches to a saturation curve till the leakage current becomes prominent. Both curves are not symmetric, showing the negative shift $\sim$1V in the voltage axis. The shift is made by the two factors: 1) work function difference and 2) positive fixed charge in the Fe-HfO_2 layer. The work function difference $\sim$0.5eV between N^+ Si and TiN generates built-in bias and causes the shift of the hysteresis loop [21], [22]. The remaining shift is caused by the fixed charge.

Fig. 3(c) shows the memory-read drain-current (I_d) – gate voltage (V_g) curves of the vertical channel FeFET with $L_g = 50$nm, varying program and erase pulse voltage. As the pulse voltage increases, memory window (MW) increases. This corresponds to Fig. 3(a) where hysteresis increases as the voltage on the Fe-HfO_2 layer increases. MW of $>$1V was obtained and applicable for memory operation. Note that, since the fast I-V measurement module was used for read I_d-V_g curves, the off-state current was limited by the resolution of the module at the dynamic range. Fig. 3(d) and Fig. 3(e) show measured endurance and retention characteristics, respectively. $>10^3$ endurance cycles and $>10^3$ seconds retention were obtained. Threshold voltage (V_{th}) at erase state decays faster than at program state, which is due to the larger depolarization field at erase state with OS channel [3].

Next, we show the results of the polar-axis transition of Fe-HfO_2 under the electric field. Fig. 4(a) shows the surface energies of the Fe-phase of crystalline HfO_2 in slab structure calculated by the first-principles simulation [23]. While the out-of-plane polar Fe-HfO_2 with (001) orientation shows the largest surface energy, the in-plane polar Fe-HfO_2 with (010) orientation has the lowest and the most stable surface energy. Fig. 4(b) shows the plan-view TEM images of the annealed $HfZrO_2$ films with and without the 10^4 electric-field cycling as wake-up operation. The grain maps within $1\mu m^2$ area and their colored orientation analyses are also shown in Fig. 4(b). Fig. 4(c) is the inverse polar mapping from Fig. 4(b), which represents the distribution of the grain crystal orientations [24]. In the film without wake-up, the dominant grain orientation is in-plane polar (010), which is consistent with Fig. 4(a). After wake-up, however, the dominant grain orientation becomes out-of-plane polar (001). This indicates that the initial in-plane polar-axis transits to the out-of-plane polar-axis in the Fe-HfO_2 grains under the electric field.

Fig. 4(d) shows the simulated kinetic pathway of the atomic structure transition. For typical up/down polarization switching, the transition barrier is comparable because of the symmetry. For the transition from the in-plane polar to the out-of-plane polar Fe-HfO_2, there is an intermediate tetragonal phase (t and t') [25]. The transition barrier is low between t and t'. Therefore, the out-of-plane polar axis can be realized from the initial in-plane polar axis via the tetragonal phases. This finding is useful in that Fe-HfO_2 can maximize the polarization for memory operation on any type of surface in 3D structure.

Then, we show the results of the fabricated vertical channel AFeFETs. Before AFeFET characteristics, half-loop hysteresis behavior was examined in an AFe- capacitor with the same AFe-layer as the AFeFET, and N^+ Si and TiN electrodes. Fig. 5(a) shows the measured Q-V curves and Fig. 5 (b) shows the measured I-V curves. In the voltage sweep between -3V and 5V or narrower range, half-loop hysteresis was obtained similar to ferroelectric hysteresis. Moreover, as we saw in Fig. 3(a) and (b), the built-in bias generated by the work function difference and the positive fixed charge shift the Q-V and I-V curves in the negative direction in the voltage axis. This results in one polarization switching at positive voltage and the other polarization switching at negative voltage, which realizes ferroelectric-like nonvolatile behavior in AFe [21], [22].

Fig. 5(c) shows the memory-read I_d–V_g curves of the vertical channel AFeFET with $L_g = 50$nm, varying program and erase pulse voltage. MW of $>$0.5V was obtained. This value is smaller than that of the FeFET because of the smaller hysteresis in the half-loop hysteresis. Fig. 5(d) and Fig. 5(e) show measured endurance and retention characteristics, respectively. $>10^3$ endurance cycles and $>10^3$ seconds retention were obtained. V_{th} decay at erase state is slower than that of the FeFET. This indicates that erase operation requires only small net polarization charge and channel charge in the AFeFET, so that the depolarization field is small and the retention is maintained. The small retention loss at erase state can be due to the depolarization of the excess polarization

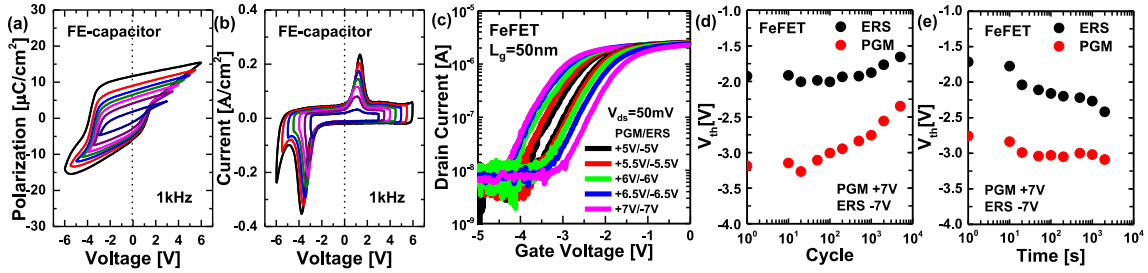

Fig. 3. (a) Measured Q-V and (b) I-V curves of the fabricated N^+ Si / ZrO_2-$HfZrO_2$-ZrO_2 / TiN Fe-capacitor, varying voltage amplitude from 3V to 6V at 1kHz. (c) Measured read I_d-V_g curves of the vertical channel FeFET. Measured (d) endurance and (e) retention characteristics of the vertical channel FeFET.

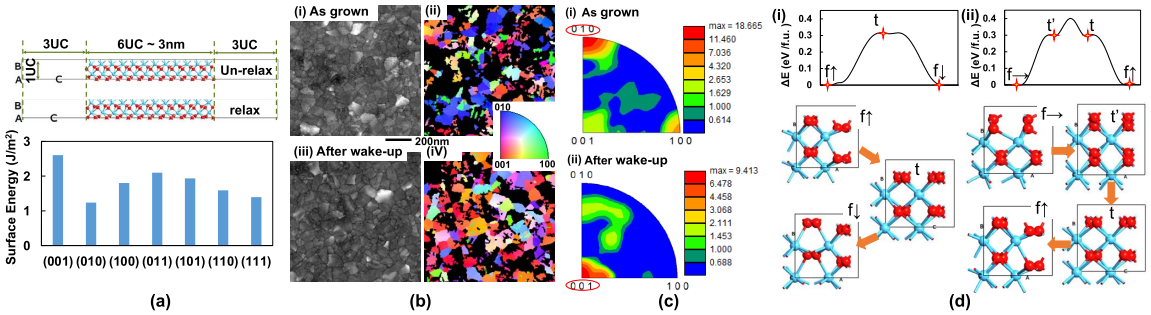

Fig. 4. (a) Calculated surface energies of Fe-HfO_2 slabs with different orientations. (b) Plan-view TEM images and crystal-orientation color-maps of FE-HfO_2 film (i-ii) without and (iii-iv) with wake-up operation. (c) Inverse polar maps from (b) (i) without and (ii) with wake-up operation by 10^4 electrical cycling. (d) Simulated pathway of (i) up/down polarization switching and (ii) in-plane/out-of-plane polarization transition via t-phases as intermediate steps.

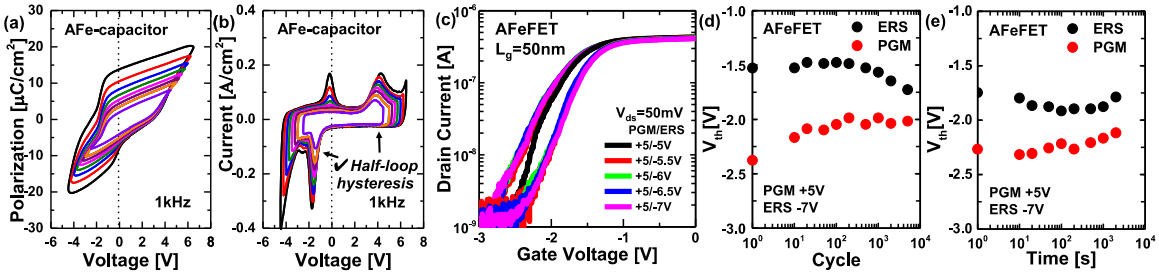

Fig. 5. (a) Measured Q-V and (b) I-V curves of the fabricated N^+ Si / ZrO_2 / TiN AFe-capacitor, setting offset voltage and varying voltage amplitude at 1kHz. (c) Measured read I_d-V_g curves of the vertical channel AFeFET. Measured (d) endurance and (e) retention characteristics of the vertical channel AFeFET.

TABLE I
BENCHMARK OF Fe-HfO_2 VERTICAL CHANNEL FeFET

	This work		[2]	[27]	[28]	[4]
Channel material	InOx		poly-Si	poly-Si	SiGe	InZnOx
Channel length	50nm		50nm	50nm	39.5nm	100nm
Gate insulator thickness	FE ZrO_2/$HfZrO_2$/ZrO_2 12nm	AFe ZrO_2 12nm	Si:HfO_2 15nm	Si:HfO_2 12nm	$Hf_{0.5}Zr_{0.5}O_2$ 10.2nm	HfZrOx 24nm
MW	1.3V	0.7V	2V	2.2V	2.3V	2V
PRG/ERS voltage	± 7V	+5V/ -7V	± 10V	± 10V	± 9V	± 5V
Endurance	10^4 cycles	10^4 cycles	10^4 cycles	10^4 cycles	10^4 cycles	10^8 cycles
Retention at room temperature	$>10^3$s	$>10^3$s	$>10^3$s	$>10^5$s	$>10^4$s	NA

induced by slight over-erase in the current write operation. Retention loss due to polarization charge loss in imprint may not be severe based on the previous work on IGZO-capped ferroelectric capacitors [26]. Further study will be needed to elucidate the retention behavior in AFeFET. Note that low V_{th} in the FeFET and AFeFET in this work are attributed to InOx channel. Higher V_{th} can be obtained by engineering gate stack and OS channel.

Table I benchmarks the vertical channel FeFET and AFeFET in this work with previously reported FeFETs with Fe-HfO_2 and various channel materials. The FeFET in this work shows the comparable MW and reliability characteristics at given thickness at relatively low voltage operation. We demonstrated the first vertical InOx channel AFeFET, showing its feasibility for vertical channel memory devices. Smaller MW in AFeFETs can be improved by AFe thickness while robust erase operation and reliability are maintained.

IV. CONCLUSION

We demonstrated a vertical channel FeFET with ALD InOx at L_g = 50nm. The FeFET shows >1V MW with reliable memory operation. We confirmed polar-axis transition from in-plane to out-of-plane in Fe-HfO_2 by experimental and theoretical study. We also demonstrated a vertical channel AFeFET with ALD InOx at L_g = 50nm. The AFeFET shows >0.5V MW. Erase state retention is improved by AFeFET thanks to the efficient erase operation by using the half-loop hysteresis of AFE. This work shows the feasibility of 3D vertical channel FeFETs and AFeFETs with OS channel for high-density storage memory.

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