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Scaled T-Gate β-Ga_2O_3 MESFETs With 2.45 kV Breakdown and High Switching Figure of Merit

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***Abstract*—We demonstrate a passivated MESFET fabricated on (010) Si-doped β-Ga_2O_3 with breakdown over 2.4 kV without field plates, high Power Figure of Merit (PFOM), and high estimated Huang's Material Figure of Merit (HMFOM), owing to low gate charge and high breakdown. MESFETs with 13 μm source-drain spacing and 75 nm channel exhibited a current density of 61 mA/mm, peak transconductance of 27 mS/mm, and on-resistance of 133 $\Omega \cdot$ mm. The device showed a PFOM competitive with state-of-the-art β-Ga_2O_3 devices and a record high estimated HMFOM for a β-Ga_2O_3 device, competitive with commercial wide-band gap devices. This demonstrates high-performance β-Ga_2O_3 devices as viable multi-kV high-voltage power switches.**

***Index Terms*—Field effect transistors, gallium oxide, MESFET, power transistors, ultra wide band gap semiconductors.**

I. Introduction

β-Ga_2O_3 is an emerging ultra-wide band gap (UWBG) semiconductor that shows great promise in the high-voltage, high-power, and high-efficiency device space, particularly for power switching and switch-mode amplification [1], [2]. β-Ga_2O_3 has a range of compatible shallow n-type dopants, including Sn, Si, and Ge [3], allowing for tunable carrier densities from 10^{15} cm^{-3} to $>10^{20}$ cm^{-3} [4], [5] enabling a wide range of breakdown voltages V_{bk} with low on resistance R_{on}. The material has a high critical electric field strength E_c estimated at 8 MV/cm due to its wide band gap of 4.8 eV [1], resulting in a Baliga's Power Figure of Merit (PFOM) of 28 GW/cm^2, exceeding that of GaN (8.6) and SiC (3.35).

Baliga defined the inherent trade-off between V_{bk} and R_{on} leading to the PFOM $V_{bk}^2/R_{(on,sp)}$ [6]. A similar tradeoff exists between switching charge Q_G and R_{on}, compelling a Huang's power switching material figure of merit (HMFOM) of $\sqrt{\mu}\cdot E_c = V_{bk}/\sqrt{R_{on}Q_G}$ for comparing devices to the unipolar material limit [7], where μ is the majority carrier mobility. Here β-Ga_2O_3 also excels, with an HMFOM of 126 $(W/C)^{1/2}$ versus 114 for GaN and 79 for SiC [8].

Many transistor topologies have been demonstrated, including MOSFETs [9]–[13], MESFETs [14]–[16], MODFETs [17], FinFETs [18], [19] and vertical devices [18], [20], both with optimized field plates [14], [21], [22] and without [23].

This letter presents a β-Ga_2O_3 MESFET that simultaneously achieves a state-of-the-art PFOM, an estimated HMFOM competitive with commercially available wide-band gap devices, and a V_{bk} of 2.45 kV, the highest reported for a non-field-plated β-Ga_2O_3 MESFET. Elimination of the gate oxide and the parasitic capacitance from source-connected field plating results in a device well-optimized for power switching, as corroborated by pulsed I-V measurements. We estimate Q_G, extracting the contributions of source-side and drain-side charge, and compare these values and methods to those of prior reported devices.

II. Methods

A device schematic and scanning electron micrograph (SEM) plan view with T-gate cross-section are shown in Figures 1a and b, respectively, for the device under test (DUT). A 75 nm Si-doped layer was homoepitaxially grown *via* ozone molecular beam epitaxy on an (010)-oriented, semi-insulating Fe-doped substrate by Novel Crystal Technologies, Japan. Devices were isolated using a high power BCl_3/Cl_2 ICP etch.

Ohmic contacts were formed first by Si ion implantation and a 900 °C furnace anneal in N_2 ambient, followed by electron beam evaporation and liftoff of a Ti/Al/Ni/Au metal stack and subsequent 60 s RTA anneal at 470 °C in N_2 ambient. A scaled T-Gate was defined *via* electron beam lithography with a gate

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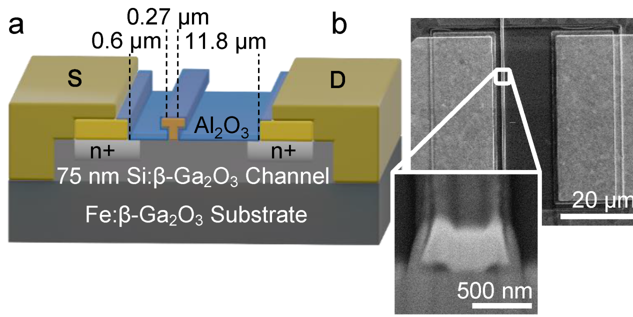


Fig. 1. a) Cross-sectional schematic of MESFET design and dimensions, and b) SEM plan view of the device under test; inset, SEM FIB cross-section of the scaled T-gate.

length L_g of ~270 nm and head spanning ~730 nm. The gate and source-drain contact pads consisted of Ni/Au deposited via electron beam evaporation and liftoff. An Al_2O_3 passivation layer with a nominal thickness of 20 nm was deposited by plasma-enhanced atomic layer deposition over the device's channel region outside the gate.

The resulting transistor had a source-drain spacing L_{sd} of nominally 13 μm, source-gate access length $L_{gs}$of 0.6 μm, gate-drain length L_{gd} of 11.8 μm, and channel width W of 50 μm.

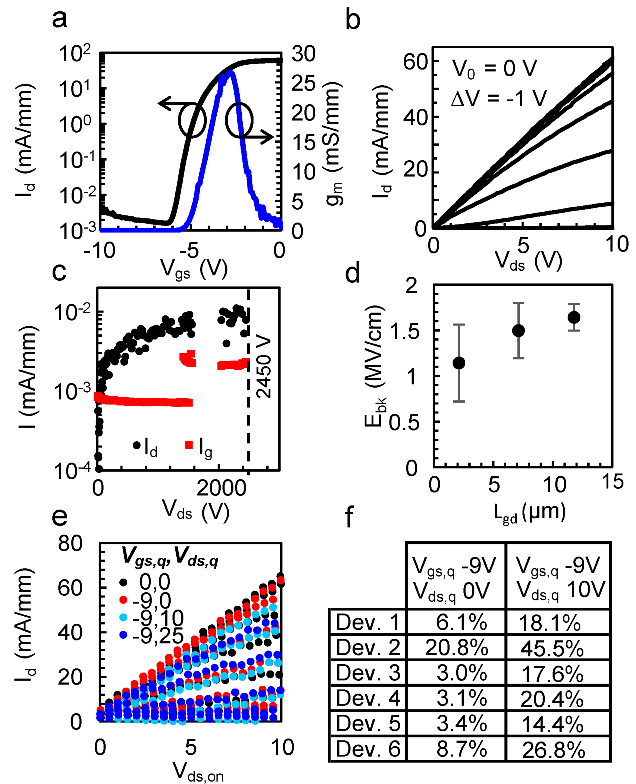
III. Results

MESFETs were characterized at room temperature (Figure 2). The DUT exhibited an off-voltage V_{off} of -6 V, a threshold voltage $V_{th}$of -4.2 V, an on/off ratio of 10^4, and a subthreshold slope of 329 mV/dec (Fig. 2a) measured at $V_{ds} = 10$ V, along with a peak current I_{max} of 60 mA/mm at $V_{ds} = 10$ V and transconductance $G_{m,peak}$ of 26.5 mS/mm. Reverse leakage and non-ideal subthreshold slope may be attributed to defect states induced by the passivation, and contamination at the substrate-epilayer interface. Conduction at $V_g = 0$ V was linear (Fig. 2b) indicating ohmic contacts but high series resistance, with an R_{on} of 133 $\Omega \cdot$ mm ($R_{on,sp}$ of 17.3 $m\Omega \cdot cm^2$ normalized to the active device area).

Wafer-scale contact resistance was determined by Transfer Length Method (TLM) to be 15 ± 4 $\Omega \cdot$ mm ($2 \times 10^{-4} \pm 8 \times 10^{-5} \Omega \cdot \text{cm}^2$). Hall measurements on micro-van der Pauw structures indicated a charge carrier density of $1.1 \pm 0.4 \times 10^{18}$ cm^{-3} and a Hall mobility of 84±7 cm^2/(V·s) in the epilayer. Breakdown under Fluorinert occurred at $V_{ds} = 2.45$ kV (Fig. 2c), a record for a β-Ga_2O_3 MESFET without field plating [14]. Average electric field at breakdown increases as function of L_{gd} across all measured MESFETs (Fig. 2d). Pulsed I-V measurements (Fig. 2e) indicate negligible gate lag, and drain lag that increases with increasing quiescent drain bias $V_{ds,q}$. Pulsed I-V performance at $V_{ds,on} = 10$ V is consistent across most devices tested (Fig. 2f).

IV. Discussion

The PFOM of the DUT (Fig. 3a) was 347 MW/cm^2, exceeding the theoretical performance of both Si and GaAs, nearly as high as record field-plated β-Ga_2O_3 MESFETs (Fig. 3a, inset) and a record for non-field plated MESFETs, three times



	$V_{gs,q}$ -9V $V_{ds,q}$ 0V	$V_{gs,q}$ -9V $V_{ds,q}$ 10V
Dev. 1	6.1%	18.1%
Dev. 2	20.8%	45.5%
Dev. 3	3.0%	17.6%
Dev. 4	3.1%	20.4%
Dev. 5	3.4%	14.4%
Dev. 6	8.7%	26.8%

Fig. 2. a) Transfer curve (black) and transconductance (blue) of the DUT *vs* V_{gs} at $V_{gd} = 10$ V; b) family of curves I_d *vs.* V_{ds} of the DUT; c) gate and drain currents I_d and I_g of the DUT measured in the off state at $V_{gs} = -8$ V, exhibiting breakdown at $V_{ds} = 2450$ V; d) average breakdown field of MESFETS *vs.* L_{gd}; e) pulsed I-V (1 ms off, 200 ns on) measurements of a 13 μm L_{sd} device at four quiescent biases; f) table of gate and drain lag (current collapse) at $V_{ds} = 9.5$ V for six 13 μm L_{sd} devices with performance comparable to the DUT.

higher than the previously reported record of 115 MW/cm^2 [14], [16], [24]. Other devices from the same sample are also shown in Figure 4, with L_{sd} of 3 μm, 8 μm, and 13 μm.

The device PFOMs increase with increasing L_{gd}, as a result of an increase in V_{bk} disproportionate to the increase in R_{on}. Treating channel depletion as a one-dimensional, single-sided abrupt junction predicts a maximum depletion width of 400 nm and V_{bk} of ~160 V at this channel doping, independent of L_{gd}. Larger devices appear to spread the applied potential over longer distances (higher depletion widths) than predicted, leading to decreased peak fields and thus higher V_{bk} than expected. The head of the T-gate likely provides some degree of electric field management in all devices, independent of L_{gd}. This observed deviation in the device depletion profile from the 1D approximation—as well as the apparent increase in average field with increasing L_{gd} (Fig. 2d)—is not intuitive, and determining the underlying mechanism is a subject of ongoing modeling and investigation.

Pulsed I-V measurements show very little current collapse as a result of gate bias alone. The lack of gate oxide and its associated defect traps plays a role, though previously reported β-Ga_2O_3 MOSFETs also show low gate lag [25], [26]. Drain lag is comparable to previous reports, and even at a quiescent drain bias of 25 V, current collapse at $V_{ds,on} = 10$ V is under 30% (Fig. 2e). Among devices with DC characteristics similar

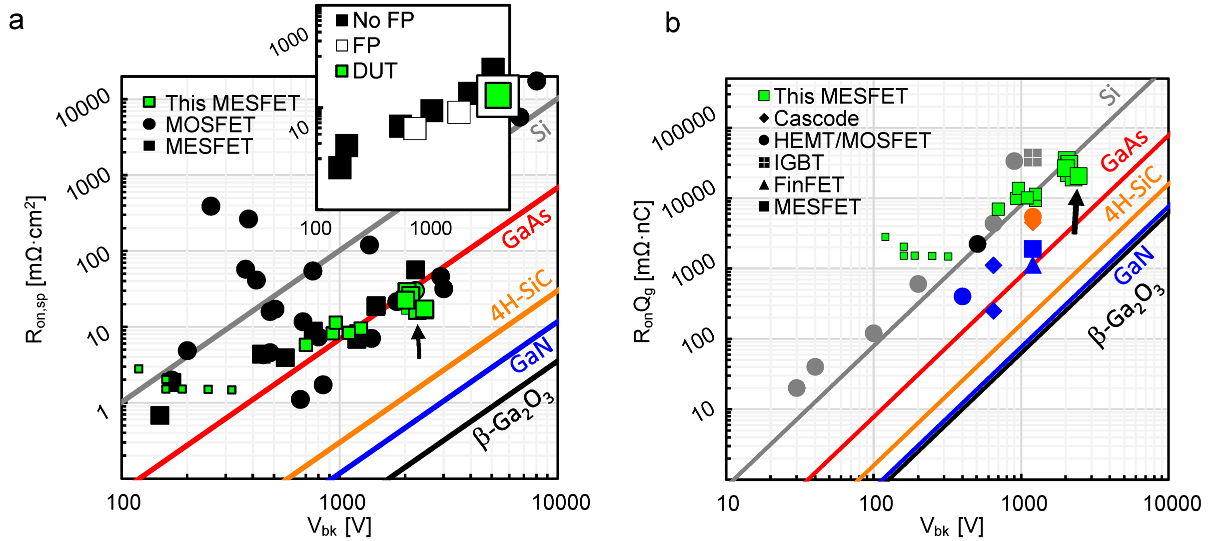


Fig. 3. a) Baliga's Figure of Merit $R_{on,sp}$ *vs.* V_{bk} for reported β-Ga_2O_3 devices (green) and β-Ga_2O_3 devices in literature (black). Devices with source-drain spacings of 3 μm, 8 μm, and 13 μm are indicated by small, medium, and large symbols, respectively. Inset: MESFETs from this work (green) and, from literature with field plates (empty) and without (filled). b) Huang's Material Figure of Merit $R_{on}Q_{gd}$ *vs.* V_{bk}, including this device (green) and reported devices in literature and data sheets. Color indicates material system and shape indicates device geometry.

to the DUT, pulsed I-V performance is consistent across most devices tested (Fig. 2f).

The DUT breaks down at an average source-drain electric field of 2.08 MV/cm. Field plates and passivation layers could potentially increase V_{bk} further [14], [27]; however, field plating and other field management are likely to increase parasitic capacitance, potentially in excess of the intrinsic capacitance accounted for by simple methods of estimating Q_G used next for HMFOM calculation.

The estimated HMFOM for the DUT was 17.15 $(W/C)^{1/2}$ (Fig. 3b), which was calculated by considering that the Miller charge Q_{gd} dominates Q_G (true for high-voltage applications [28]) and by estimating $Q_{gd} = qN_Dt_DA = 7.89$ pC that considers full depletion of the drift region, as proposed by Zhang *et al.* [29]. Here, N_D is the channel doping of 1.1×10^{18} cm^{-3}, t_D is the channel thickness of 75 nm, $A = L_{GD} \cdot W \sim 597$ μm^2 and q is the elementary charge. (Fig. 1a). This estimated HMFOM is the highest reported for β-Ga_2O_3, competitive with commercial SiC devices, [29] and comparable to some GaN [30] devices but at a markedly higher V_{bk}.

We also estimated the source-side charge $Q_{gs} = 0.128$ pC by assuming that at V_{th} the full thickness of the channel was depleted along with a lateral depletion radially from the source-side gate edge of 75 nm. Calculated Q_{gs} is therefore negligible compared to Q_{gd}, but may require consideration for low-voltage, high-current applications. The remaining component of Q_G, *i.e.*, reverse capacitance charge Q_{rss}, has been ignored as it is negligible in unipolar devices [29]. Therefore, a geometric estimation of the drift region depletion charge provides the best conservative estimate of Q_G for benchmarking purposes, as it overestimates the intrinsic channel charge while disregarding extrinsic capacitances. This method produces a conservative estimate only in the absence of sources of extrinsic capacitance integral to device performance, *i.e.* field plates or other field management schemes.

Future work is underway to fabricate a large-periphery device to measure an experimental value of Q_G directly from the dynamic measurement [28]. Further care must be taken in comparing values of HMFOM or Q_G to commercial devices, as data sheets often do not report V_{bk}, and the switching conditions and relative contributions for different components of Q_G.

We also envision future device optimizations by improving contact resistance to 0.5 $\Omega \cdot$ mm which would improve the PFOM to 390 MW/cm^2 and the estimated HMFOM to 18.2 $(W/C)^{1/2}$. Eliminating access resistance—*via* a self-aligned gate design, *e.g.* [13]—would improve them to 408 MW/cm^2 and 18.6 $(W/C)^{1/2}$, respectively. One can also gain by improving carrier mobility towards the predicted room-temperature value of $\sim$200 cm^2/V$\cdot$s [31]; this will increase the PFOM and estimated HMFOM to 967 MW/cm^2 and 28.6 $(W/C)^{1/2}$, respectively. Gains from eliminating extrinsic resistances will be limited, as most of the series resistance in this device comes from the drain region used for obtaining large V_{bk}.

On account of the V_{bk} of these devices being significantly higher than predicted by the single-sided abrupt junction assumption for material of this geometry and doping level, future device design may move towards higher-doped channels, as multi-kV devices can be fabricated at dopings in excess of 1×10^{18} cm^{-3}. This allows for low-R_{on}, high-V_{bk} parts with performance tunable both by doping and gate-drain spacing.

V. Summary

β-Ga_2O_3 MESFETs with high PFOM and multi-kV V_{bk} show competitive performance with commercial wide-band gap devices, and a record-high estimated HMFOM for a β-Ga_2O_3 device, without the use of field plating. This work demonstrates the great potential for β-Ga_2O_3 power switches and switch-mode amplifiers.

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