Area-Selective Electroless Deposition of Cu for Hybrid Bonding

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***Abstract*—This letter describes the use of area-selective electroless Cu deposition for topography control of Cu-SiCN hybrid bonding pads. The electroless deposition of Cu allows one to obtain protrusions on hybrid bonding Cu pads without further polishing optimization. A recessed Cu pad after chemical mechanical polishing becomes a protrusion after electroless deposition. This indicates that the electroless Cu film was selectively deposited on Cu, without deposition on the SiCN surface. A void-free Cu-Cu bonding interface was observed after annealing at 350 °C with an electroless Cu layer at the interface. 100% electrical connection was obtained at 1.4-μm pitch where the deposition thickness was on target.**

***Index Terms*—Hybrid bonding, electroless deposition, area-selective deposition.**

I. Introduction

Hybrid bonding is a promising direct wafer bonding approach which creates mechanical joints (dielectric-dielectric) and electrical connections (Cu-Cu) simultaneously [1]–[4]. The higher flexibility of the system design allowed by hybrid bonding enables us to make higher-density connections for the top and bottom wafers. In hybrid bonding, two wafers are finished by a Cu/dielectric damascene process with atomic-scale dielectric surface roughness and minimal Cu protrusion/recess [1], [2]. The capabilities of this approach strongly depend on the quality of the chemical mechanical polishing (CMP) processes. The required range of the recess and protrusion of a Cu pad from the dielectric field is below 5 nm for fine-pitch connections [1], [2]. It is known that the mechanism of Cu-Cu connection during hybrid bonding is “Cu pumping” during post-bond annealing [5]–[7]. If the Cu surface is recessed on both sides of the wafer, the Cu-Cu interface will be under high tensile stress after cooling, which may be a concern for reliability. Therefore, the ideal shape of the Cu pad is zero recess for both sides of the wafer.

However, the CMP process needs to be optimized for within-wafer uniformity across the wafer edge, residue control

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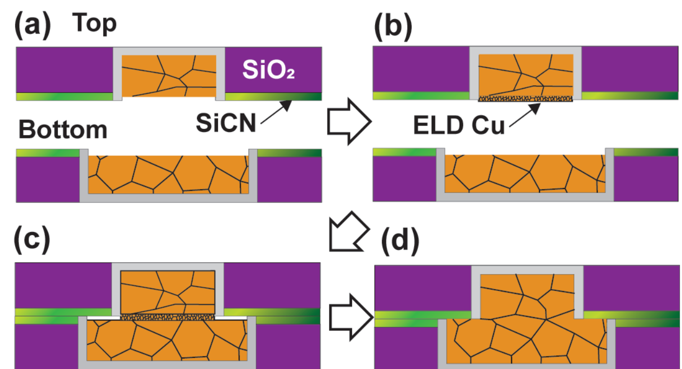

Fig. 1. Schematic illustration of process flow of electroless Cu deposition on hybrid bonding interface. (a) Post-barrier CMP, (b) post-ELD on top pad, (c) post-hybrid bonding, and (d) after post-bond annealing.

(e.g. over-polishing and post-cleaning) and galvanic corrosion, as well [1], [2], [8]. Therefore, controlling the selectivity of the Cu, barrier and dielectric during barrier CMP becomes significantly challenging, in particular when the pitch size becomes finer. The Cu pad eventually tends to be recessed at the few nanometer level in hybrid bonding pads.

Electroless deposition (ELD) has unique properties compared to other film deposition processes. The method selectively deposits metals on metal with no deposition on non-catalytic surfaces, such as a dielectric layer [9]–[15]. Furthermore, the deposition rate is controllable at the nanometer level. In this study, we investigated reshaping the Cu pad topography by area-selective ELD Cu. The impact of the ELD Cu was confirmed by electrical measurements in daisy chains and cross-sectional images of the interface.

II. Experimental

All wafer scale processes were performed using 300-mm Si wafers as the substrate. A high-resolution damascene surface containing sub-micron size Cu pads was used for the experiments. The top and bottom pad sizes used in the experiments were 540 and 1080 nm for 2.0-μm pitch and 360 and 720 nm for 1.4-μm pitch. Plasma enhanced chemical vapor deposited SiCN was used as the bonding interfacial dielectric layer [16], [17]. To minimize the SiCN dielectric roll-off, a hard substrate configuration in the CMP hardware system in combination with the proper slurry enabled stable and controllable performance. A wafer-scale ELD tool was used for the test. The ELD bath was a commercial

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solution with a metal base complexing agent, which does not generate hydrogen during the chemical process. The surface topography was analyzed by atomic force microscopy (AFM). The statistical Cu step height was characterized by converting the AFM image raw data into numerical data. Both top and bottom wafers were activated by nitrogen plasma and cleaned by megasonic DI water prior to bonding. Wafers with two different topographies prepared by a CMP process were stacked face-to-face [18]. After wafer bonding, the double-thickness wafers were annealed by a two-step process: an initial step at 250 °C to increase the adhesion strength of the brittle SiCN-SiCN surface, then a final step at 350 °C to contact the Cu-Cu nano-pad surface. After post-bonding annealing, the interface voids were detected by scanning acoustic microscopy (SAM). Afterwards, the bonded wafers were thinned to 5 μm, revealing 5 μm-diameter and 8 μm-depth Through-Si vias (TSVs) [19], [20]. The backside was finalized by aluminum metallization for electrical probing. The cross-sectional images were observed by transmission electron microscopy (TEM) for high-resolution imaging.

III. Results and Discussion

The typical bath temperature used for the solution provided by the chemical vendor is 70 °C. However, the deposition rate was 1.75 nm/s at 70 °C, which implies that it would take only 2.8 s to reach the 5-nm deposition target. Uniformity control within 2.8 s is significantly difficult for a 300-mm wafer. Therefore, the temperature was adjusted for application of the hybrid bonding pad. Although the data is not shown here, the deposition thickness, which was confirmed by Rutherford backscattering spectrometry and the sheet resistance of Cu, increased linearly with time regardless of the temperature. By decreasing the temperature of the ELD Cu process to 30 °C, the deposition rate also decreased to 0.25 nm/s. The obtained within-wafer uniformity of the ELD film thickness on a blanket Cu wafer was 5.7% at an average deposition thickness of 4.7 nm within-wafer.

After optimization on the blanket wafer, the low-temperature ELD process was applied on the hybrid bonding pad surface after CMP. Figure 2(a) and (b) show the AFM results on hybrid bonding pads before and after electrodeposition on the top wafer. Prior to electrodeposition, the average recess amount of the Cu against the SiCN surface was −2.28 nm (STDEV 0.35 nm) and −2.18 nm (0.31 nm) for 1.4-μm and 2.0-μm pitch, respectively. This was quite similar for the bottom wafer (−2.49 nm for 1.4-μm pitch and −1.92 nm for 2.0-μm pitch) as shown in Figure 2 (c) and (d).

The exact same ELD process which was used for the blanket Cu wafer was applied on the hybrid bonding pad. Post-ELD, all the Cu recesses became protrusions. The AFM measurement is executed on exactly the same pad before and after ELD Cu. This indicates that no Cu was deposited on the SiCN surface and that Cu was selectively deposited on Cu surfaces. ELD Cu can only deposit on a surface which is catalytic for the reducing agent. The SiCN does not have such a catalytic effect for the reducing agent of this ELD chemistry. Therefore, the ELD Cu shows area selective deposition on hybrid bonding surface.

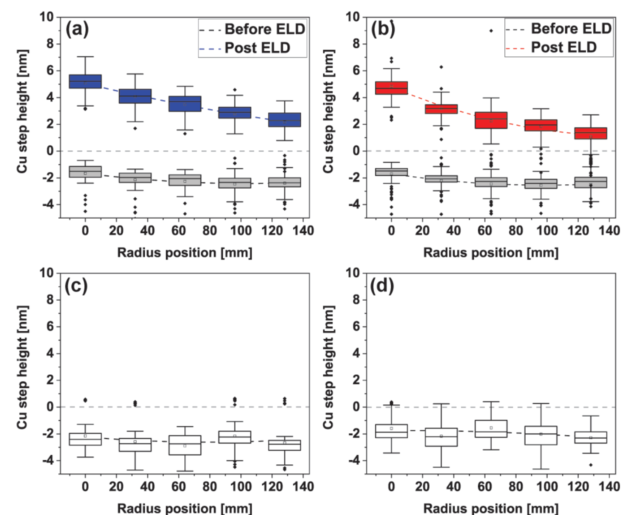

Fig. 2. Statistical AFM data within wafer for top and bottom wafers. (a) Top wafer at 1.4-μm pitch. (b) Top wafer at 2.0-μm pitch. (c) Bottom wafer at 1.4-μm pitch. (d) Bottom wafer at 2.0-μm pitch.

The protrusion amount of Cu varied from the wafer center towards the edge with values of 4.84, 3.19, 2.26, 1.84 and 1.06 nm for 1.4-μm pitch. The deposited ELD was 6.54 nm at the wafer center and 3.55 nm at the edge; such a difference in the deposition thickness was not seen for the blanket wafer. This might be explained by a loading effect, probably due to electrochemical surface potential differences caused by underlying metal lines. The delta (bottom recess to top protrusion) was 2.70 nm for the wafer center, −0.63 nm for the wafer middle and −1.6 nm for the wafer edge. We attempted to distinguish the ELD layer and damascene electrochemical deposited (ECD) Cu layer by TEM observation; however, there were homogeneous Cu grains/layers at the top surface of the pads. This might be due to self-annealing growth of ELD Cu due to the residual stress in the ECD Cu [21]–[23]. The ELD Cu layer might be recrystallized immediately along with the underlying ECD Cu layer by self-annealing.

Despite the non-uniformity of the ELD Cu caused by loading effects, the wafer pair was bonded with a high alignment accuracy. The result of the overlay model parameter was T(x) = 92 nm, T(y) = −124 nm and R = −0.355 μrad. The overlay total misalignment of the wafer was 252 nm with 121 nm of residuals. The misalignment value was slightly higher than the wafer pairs without ELD (<200 nm for the alignment and <120 nm for the residuals). This might be due to the protruding part of the ELD Cu around the wafer center, such that the surface topography might cause extra misalignment.

Figure 3 shows SAM images after bonding. The white area indicates where significant acoustic sound reflection is obtained (= non-bonded area or void). The non-bonded area is clearly seen to encompass the entire wafer right after bonding. Although most of the non-bonded area has a finer pitch pad area than 1.4-μm, some of the area above 1.4-μm pitch is also not bonded. The wafer pair had a 2-step annealing process consisting of 250 °C for 2 h and 350 °C for 2 h. The voids were significantly reduced after annealing at 250 °C for 2 h. The bondability at the wafer edge seemed to be better than

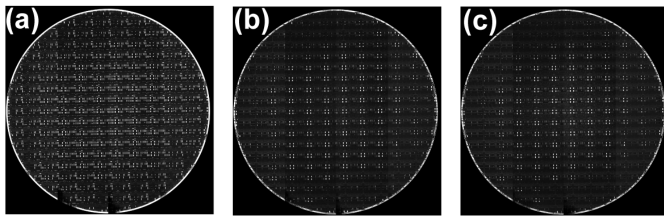

Fig. 3. SAM scan images of 300 mm bonded wafers for a pair (a) post-bonding, (b) post-1st-annealing at 250 °C for 2 h, and (c) post-2nd-annealing at 350 °C for 2 h.

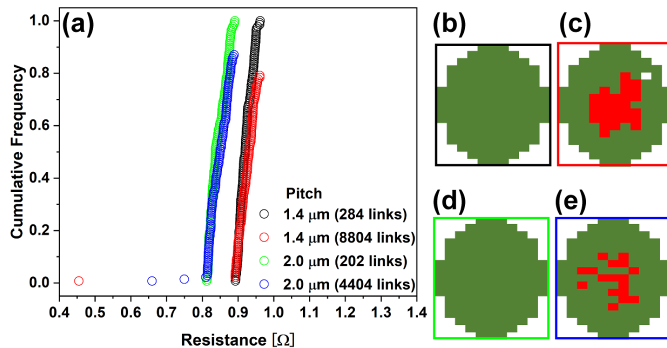

Fig. 4. (a) Electrical resistance distribution of daisy chains. (b) Wafer map of electrical connection at (b) 284 links (1.4-μm pitch), (c) 8804 links (1.4-μm pitch), (d) 202 links (2.0-μm pitch), and (e) 4404 links (2.0-μm pitch).

at the wafer center. There was no significant change from the state after 250 °C annealing for 2 h to that after 350 °C annealing for 2 h. The good bondability at the wafer middle and edge can also be explained by the delta of ELD protrusion and CMP recess for the bottom wafer, which is close to zero or minus.

After the bonding and annealing, the top Si wafer was thinned down to 5 μm. The 8-μm depth via-middle TSVs were revealed from the backside by the thinning process. The electrical yields of daisy chains were measured through the TSVs. Figure 4(a) shows daisy chain electrical yields. The electrical resistance value when the hybrid bonding pad is formed only by CMP can be found in Ref [2]. The obtained contact resistance with ELD Cu at the interface is equivalent to the surface formed by CMP for both 1.4 and 2.0 μm pitch. 100% yield was obtained for 284 links of 1.4-μm pitch and 202 links of 2.0-μm pitch over the entire wafer. However, the yield of 1.4-μm pitch with 8804 links was 79% and that of 2.0-μm pitch with 4404 links was 88%. Figure 4(b)–(e) shows the wafer map of the electrical measurement. The dies with non-connected daisy chains are indicated in red. The non-yielding area corresponds to the area where the ELD Cu created protrusions. In other words, if the protrusion-recess control of ELD works like the wafer middle and wafer edge, the ELD Cu layer itself does not have an impact on the electrical yields.

Figure 5 (a) shows cross-sectional TEM images of the Cu-Cu interface. The specimen was taken from the wafer middle where good electrical yield was obtained. Homogeneous Cu can be observed in the image, and there are no defects, voids, or clear indication of an interface at the Cu-Cu junction. This means that ELD Cu only played the role of topography

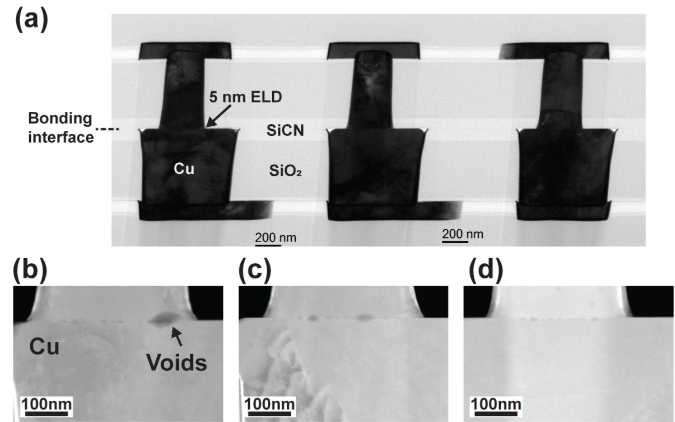

Fig. 5. Cross-sectional TEM images of 1.4-μm pitch hybrid bonding interface after 350 °C anneal for 2 h. (a) A specimen taken from an area with good electrical yield at the wafer middle and high-resolution STEM-HAADF images at the (b) wafer center, (c) wafer middle, and (d) wafer edge.

control prior to bonding and had no negative impact on the Cu-Cu bonding. Figure 5(b), (c) and (d) show higher magnification STEM of the Cu-Cu interface at the wafer center, middle and edge. Although a minor void (low density area) was observed at the wafer center (see Figure 5(b)), a Cu connection was formed for all the locations. There was no gap in between the top and bottom Cu even though an ELD layer existed at the interface.

IV. Conclusion

We demonstrated area-selective Cu deposition on hybrid bonding Cu pads by electroless deposition. ELD Cu only deposited on the Cu pads, without deposition on the SiCN surface. Hence, the electroless Cu process had no impact on the SiCN-SiCN bonding interface. Although there was some wafer-level non-uniformity of ELD Cu caused by a micro-loading effect, the recess shape of Cu pads was repaired by ELD Cu. As a result, excellent hybrid bonding connection was obtained, where the delta between recess and protrusion was near zero nanometers. The superior electrical connection results are encouraging for the future of electroless Cu deposition for hybrid wafer bonding applications. As the control of surface topography using CMP alone will become more challenging for finer pitch hybrid bonding, such a nano-level area-selective "repair" approach may become essential. The results obtained in this study are encouraging for the concept of area selective deposition works for future node fine pitch hybrid bonding.

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