On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET

Lucas Nyssens, *Graduate Student Member, IEEE*, M. Rack, A. Halder, J.-P. Raskin, *Fellow, IEEE*, and V. Kilchytska, *Member, IEEE*

***Abstract*—This paper proposes an original approach to separately characterize self-heating and substrate effects in Fully-Depleted Silicon-on-Insulator (FD-SOI) devices. As both dynamic self-heating and drain to source coupling through the back-gate and substrate of an FD-SOI MOSFET induce a frequency transition in the Y-parameters in a common frequency range, it is crucial to properly separate them for further modeling. The proposed novel method is based on the extraction of the back-gate and substrate networks from the S-parameters measured at the zero-temperature coefficient bias. It enables the accurate and unambiguous extraction of thermal impedance for different biases, thus providing the extraction of the device thermal resistance and capacitance for different power levels from S-parameters measurements.**

***Index Terms*—Back-gate modeling, FD-SOI MOSFET, RF extraction, self-heating, S-parameters measurements, substrate coupling, ultra-wideband modeling.**

I. Introduction

THE downscaling of CMOS technology has been crucial for improving device performance and reducing manufacturing cost. However, aggressive scaling results in higher current and power densities, thereby increasing the self-heating (SH) effect and the lattice temperature (T_c). Fully-Depleted Silicon-on-Insulator (FD-SOI) transistors offer outstanding electrostatic control, very low mismatch, excellent analog and RF figures of merit [1]–[4]. However, due to the presence of the buried oxide (BOX), SH of more significance is present in FD-SOI MOSFETs than in their bulk counterparts [5]. Dynamic self-heating is known to induce a transition in the Y-parameters over frequency that is used in turn to extract the thermal parameters [5]–[13]. Furthermore, the drain to source coupling through the back-gate (B-G) node (or Si substrate under the BOX) also induces a transition in the Y-parameters in a similar frequency range [9], [14]. Although this transition was originally very pronounced in FD-SOI devices with thin BOX [9] contrarily to previous device generations [14], the introduction of a highly-doped region below the BOX strongly reduces the transition [5]. The transition associated to the coupling via substrate is thus usually neglected/ignored in these devices, which may however lead to misinterpretation and erroneous modeling of SH [5], [10]. To the best of the authors' knowledge, no method has been proposed to separately characterize each contribution, i.e. SH and B-G effect (also called substrate effect, SE), into Y-parameter frequency response. In this paper, we will (i) demonstrate that the SE partially overlaps SH forming a common, indistinguishable distributed transition from 100 kHz to 10 GHz, (ii) show that the dynamic SH effect vanishes at the zero-temperature coefficient (ZTC) bias point, (iii) use this bias point to extract the SH-free transistor electrical model including the B-G and substrate nodes, (iv) extract the frequency-dependent thermal impedance $Z_{th}(f)$ for different bias conditions, and (v) compare it to the conventional extraction procedure that neglects the transitions associated to the B-G node.

Manuscript received March 15, 2021; accepted March 25, 2021. Date of publication April 5, 2021; date of current version April 26, 2021. This work was supported by Ecsel JU project Beyond5 through EU H2020 and Innoviris (Brussels/Belgium) funding under Grant 876124. The work of Lucas Nyssens was supported by the Fonds de la Recherche Scientifique - FNRS. The review of this letter was arranged by Editor B. S. Doyle. *(Corresponding author: Lucas Nyssens.)*

Lucas Nyssens is with the ICTEAM Institute, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium, and also with the Fonds de la Recherche Scientifique - FNRS, 1000 Bruxelles, Belgium (e-mail: lucas.nyssens@uclouvain.be).

M. Rack, A. Halder, J.-P. Raskin, and V. Kilchytska are with the ICTEAM Institute, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LED.2021.3071272.

Digital Object Identifier 10.1109/LED.2021.3071272

II. Self-Heating and Back-Gate Node Extraction

A. Advantage of ZTC Bias for Unambiguous Extraction

An FD-SOI super-low threshold voltage nMOSFET from 22FDX® [2] featuring a gate length of 20 nm, finger width of 0.5 μm, 20 fingers and a multiplicity of 6 for a total width of 60 μm is studied. Its S-parameters are measured on-wafer from 100 kHz to 10 GHz using a vector network analyzer from Keysight, coupled with a probe station hosting a thermal chuck for additional dc I-V measurements at 300, 320, 335, 350, 370 and 390 K. The back-gate voltage (V_{bg}) is set to 0 V. The RF MOSFETs are probed using a Ground-Signal-Ground (GSG) configuration. A Short-Open-Load-Thru (SOLT) calibration is performed and dedicated open and short structures are measured to de-embed the transistor measurements down to the first metal layer.

The conventional method to extract SH parameters from S-parameter measurements [6]–[8] relies on the fact that the lattice temperature is able to follow a "slowly" (w.r.t. its thermal time constant) varying ac signal, but ceases to follow the ac signal if it is too "fast", leading to a step between the low and high frequency values of Y_{dd} (Y_{22}) and Y_{dg} (Y_{21}). This so-called dynamic SH effect has been rigorously put into equations for a general two-port device in [11]. In our case, the equations simplify into:

$$Y_{dd} = Y_{ddT} + Z_{th}\frac{dI_d}{dT_A}\left(Y_{ddT}V_d + I_d\right), \quad (1a)$$

$$Y_{dg} = Y_{dgT} + Z_{th}\frac{dI_d}{dT_A}Y_{dgT}V_d \quad (1b)$$

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

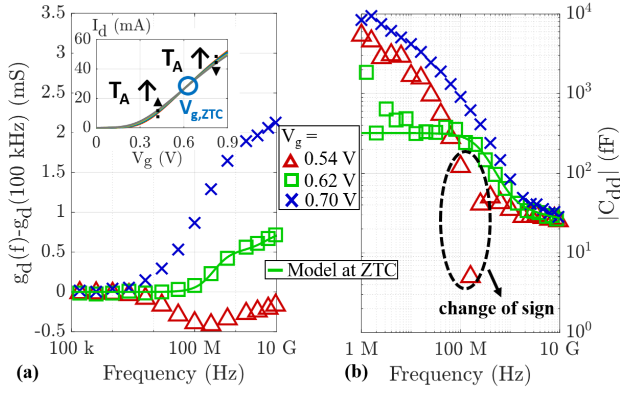

Fig. 1. Variation of the output conductance $g_d(f)$ ($Re(Y_{dd})$) w.r.t. its value at 100 kHz (a) and $C_{dd}(f)$ ($Im(Y_{dd}/\omega)$), (b) of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8$ V and $V_g = 0.54$, 0.62 and 0.7 V (symbols). Fitted electrical model at ZTC bias point $V_g = V_{g,ZTC} = 0.62$ V in solid lines, such that the dynamic self-heating effect is not present. Inset of (a): Measured I_d-V_g at $V_d = 0.8$ V from an ambient temperature of 300 K to 390 K.

with Y_{ddT} and Y_{dgT} being the admittances for the isothermal case, i.e. when the lattice temperature does not vary with the ac signal. Y_{ddT} and Y_{dgT} are by definition not affected by dynamic self-heating. T_A is the ambient temperature.

The inset in Fig. 1(a) shows the I_d-V_g curves for different ambient temperatures. Due to the threshold voltage reduction with increasing temperatures, I_d increases with T_A at low V_g. Whereas, I_d decreases with T_A for large V_g biases because of stronger phonon scattering decreasing carrier mobility. These two mechanisms compensate each other at the ZTC bias point [15], such that the I_d associated to this bias does not change with temperature. For the studied device, the ZTC bias is $V_{g,ZTC} = 0.62$ V for $V_d = 0.8$ V and $V_{bg} = 0$ V.

Fig. 1(a) shows the variation of $g_d(f)$ computed as $Re(Y_{dd})$. The curve for $V_g = 0.54$ V shows a monotonic decrease in $g_d(f)$ starting from ~1 MHz related to SH, followed by an increase for frequencies above 100 MHz that cannot be described by dynamic self-heating (1a) and which is attributed to the SE. The SE is also present at the other biases. For $V_g > V_{g,ZTC}$, both substrate and self-heating effects contribute to a step increase in $g_d(f)$, such that the thermal resistance R_{th} (and thus lattice temperature) would be overestimated if the SE were to be ignored. At the ZTC bias, the dynamic SH does not affect the ac curves and the observed transition (Fig. 1, green data) is solely due to the SE. Similar trends are observed in the output capacitance C_{dd} (computed as $Im(Y_{dd})/\omega$) in Fig. 1(b). The ZTC bias point therefore enables the extraction of the small-signal parameters associated to the B-G and substrate nodes without any dependency on the SH effects. As the ZTC bias point is not specific to this technology [16]–[20] and has been experimentally verified down to cryogenic temperatures [21], [22], the proposed methodology can be widely applied.

By taking the real and imaginary parts of (1a), we can derive the equations describing the dynamic SH effect on $g_d(f)$ and $C_{dd}(f)$:

$$g_d \equiv Re\left(Y_{dd}\right) \approx g_{dT} + Re\left(Z_{th}\right)\frac{dI_d}{dT_A}\left(g_{dT}V_d + I_d\right), \quad (2)$$

$$C_{dd} \equiv \frac{Im\left(Y_{dd}\right)}{\omega} \approx C_{ddT} + \frac{Im\left(Z_{th}\right)}{\omega}\frac{dI_d}{dT_A}\left(g_{dT}V_d + I_d\right). \quad (3)$$

From (2) and (3), it is plain to see that the low frequency values of g_d and C_{dd} (and the transition sign) depend on the

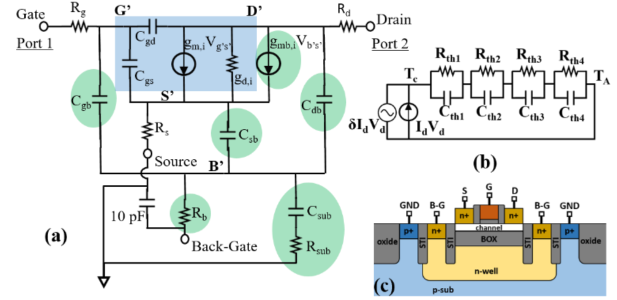

Fig. 2. (a) Small-signal equivalent circuit of an FD-SOI MOSFET including back-gate and substrate nodes and, (b) 4th-order thermal network used to model the thermal impedance $Z_{th}(f)$. (c) Schematic cross-section of an FD-SOI nMOSFET (not to scale).

sign of dI_d/dT_A, and is thereby governed by the two opposing mechanisms of mobility and threshold voltage reduction with increasing temperature [6], [7], [23]. The frequency transition in itself is due to a delay in the heat transport mechanism from device to heat sink, yielding a lattice temperature that is not able to follow instantaneous variations of an ac power at frequencies above the isothermal frequency.

B. Extraction of Substrate and Back-Gate Nodes Model

The substrate and B-G lumped circuit parameters (in green in Fig. 2(a)) are extracted from optimization for a best fit of the measured Y-parameters to the small-signal equivalent circuit in Fig. 2(a) in the frequency range from 10 MHz to 10 GHz, similar to [24]–[26]. The series resistances R_g, R_d and R_s are extracted beforehand with Bracale's method [27]. The resulting fitting of $Y_{dd}(f)$ and measurements at the ZTC bias point is shown in Figs. 1(a) and 1(b) in solid (green) lines.

C. Thermal Impedance Extraction

Knowing the B-G model, the complex thermal impedance $Z_{th}(f)$ is extracted at other bias conditions than at ZTC. The values of some bias-dependent parameters (C_{gd}, C_{gs}, $g_{m,i}$, $g_{d,i}$, in blue in Fig. 2(a)) are updated accordingly. However, the parameters associated to the B-G and substrate nodes (in green in Fig. 2(a)) are assumed to remain constant with V_g in the (strong) inversion regime. It is nevertheless important to emphasize that they are not assumed independent of V_d and V_{bg}, since for any applied V_d and V_{bg} there will exist a V_g yielding ZTC conditions. The frequency dependent (due to SE) $Y_{ddT}(f)$ term is then computed using the updated small-signal equivalent circuit parameters for each bias.

Next, an nth-order thermal network representing Z_{th} is used to fit the $Y_{dd}(f)$ data according to (1a). Both the imaginary and real parts of Y_{dd} are used for fitting, although only fitting $Im(Y_{dd})$ gives very close results. The term dI_d/dT_A is experimentally obtained from dc I-V measurements at several T_A (see inset of Fig. 1(a)). In our case, selecting $n = 4$ (cf. Fig. 2(b)) appeared to be sufficient to correctly model the distributed transition. The resulting thermal and electrical model is shown for different bias points and compared with the measured Y-parameters in Fig. 3.

III. Results

We observe that a very good fitting is obtained across a very wide frequency range from 100 kHz up to approximately 10 GHz for the different bias points. The sign of the step (either positive or negative) is correctly reproduced in accordance with (2) and (3). To the best of our knowledge, it is

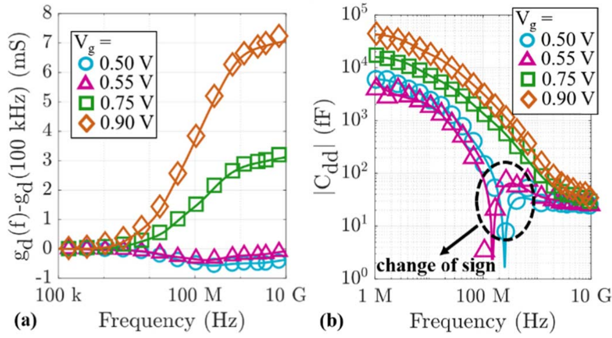

Fig. 3. $g_d(f)$ (left) and $C_{dd}(f)$ (right) of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8$ V and different V_g, with dynamic self-heating. Measurements in symbols and fitted model (with n = 4) in solid lines.

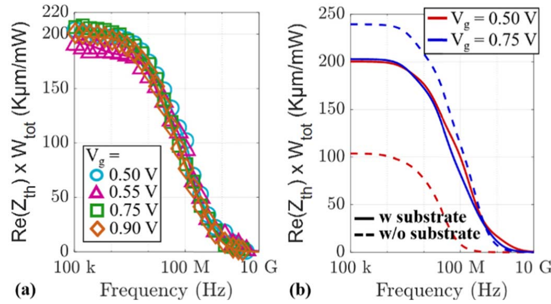

Fig. 4. Left (a): $Re(Z_{th})$ normalized to the total device width of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8$ V and different V_g. Measurements in symbols and fitted model in solid lines. Right (b): extracted self-heating model of $Re(Z_{th})$ including back-gate and substrate nodes (solid lines) and ignoring their modelization (dashed lines).

the first time that $g_d(f)$ and $C_{dd}(f)$ curves for $V_g < V_{g,ZTC}$ with a negative step in $g_d(f)$ are shown and that the total R_{th} is extracted from them. Although the physical origin of this negative step is known and explained in Section II.A, such curves have not been presented previously, since high biases -where SH has higher impact, and thus a positive step in $g_d(f)$- are commonly used in self-heating characterization. With technology scaling down and power reduction, the voltage range below ZTC becomes of interest. Even if SH is lower in that range, it nevertheless has to be taken into account (in particular its frequency response).

Fig. 4(a) shows the real part of the extracted Z_{th} for different biases. All curves superimpose meaning that the frequency-dependent Z_{th} (f) is power-independent (or almost), as expected at room temperature, thus confirming the consistency of the method. Though a roughly constant R_{th} with power is extracted in this work, it is not necessarily the case for other devices or in different conditions, such as at cryogenic temperatures [28]. We also observe that $Re(Z_{th})$ becomes negligible only above 2.4 GHz (<1% its maximum value), therefore yielding an isothermal frequency above 2.4 GHz. This confirms our previous statement that SH and the SE cannot be easily distinguished in such devices as they appear in the same frequency range.

Indeed, Fig. 4(b) shows that extracting Z_{th} without taking into account the B-G and substrate nodes, i.e. by using constant g_{dT} and C_{ddT} versus frequency as in [12], [13], can lead to a strong misestimation of Z_{th}. Ignoring the existance of the B-G associated transition leads to an overestimation (underestimation) of the total R_{th} ($R_{th} = \sum_i R_{th,i}$) when $V_g > V_{g,ZTC}$ ($V_g < V_{g,ZTC}$), because its effect adds up

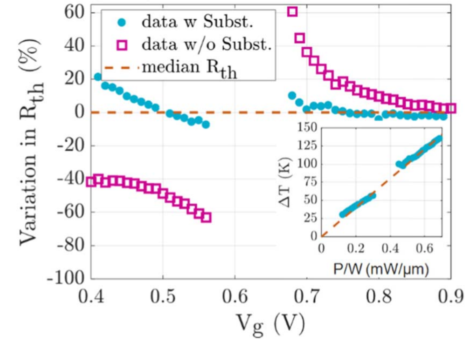

Fig. 5. Variation of total $R_{th,n} = W_{tot} \sum_i R_{th,i}$ of a 20 nm FD-SOI MOSFET biased at $V_d = 0.8$ V and different V_g, in dots. Median $R_{th,n}$ of 202 Kμm/mW in dashed line. Variation of $R_{th,n}$ extracted neglecting the back-gate and substrate nodes, in squares. Inset: extracted temperature rise versus dissipated power normalized by the total transistor width (60 μm).

(counteracts) with the SH effect, respectively, as shown in Fig. 5, which plots the extracted total R_{th} for different V_g, with (blue data) and without (pink data) accounting for SE. The R_{th} is not extracted close to the ZTC bias point, because of the singularity (divide by zero) provided by the dI_d/dT_A term tending to 0 as V_g tends to $V_{g,ZTC}$, thus introducing a larger error.

While for large $I_d(V_g)$ bias conditions (as in [5], [10]), the SH effect dominates the transition and neglecting the B-G/substrate nodes leads to a minor (5%) error in the R_{th} evaluation, accounting for SE (and its independent modeling) is crucial for low-power applications. An extensive comparison of the electrical characteristics of the model extracted with and without taking into account the corrected value of R_{th} merits additional investigations, but is out of scope of this Letter. Indeed, neglecting the SE modeling can lead to an error as large as 60% in R_{th} at lower $I_d(V_g)$ (red curves in Fig. 4b).

In contrast, the novel method achieves an excellent accuracy at intermediate power and still performs well at low power, with resulting errors below 5% and 20%, respectively. The small remaining error at low V_g can be explained by a slightly bias-dependent Y_{ddT} not accounted for. The corresponding temperature rise ($\Delta T = R_{th}.P$) versus power (P) is displayed in the inset of Fig. 5. The extracted R_{th} is roughly constant across the whole V_g range and gives a median value of 202 Kμm/mW.

IV. Conclusion

In this paper, we propose a method to extract the thermal impedance from device measurements unaffected by the substrate network in the frequency range of interest for dynamic self-heating. The ZTC bias condition can be used to extract any dynamic self-heating-free small-signal model. It can therefore be directly applied to measurements without requiring a compact model or simulation to capture the transition not related to SH. The developed procedure enables the extraction of $R_{th}(P,T_A)$ from S-parameters at different bias conditions and could be of particular interest for measurements at cryogenic temperatures for which R_{th} is not constant versus power.

Acknowledgment

The authors thank GlobalFoundries for chip fabrication and research support. This article was published with the support of the University Foundation of Belgium.

References

[1] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P.-O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Beranger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28 nm FDSOI technology platform for high-speed low-voltage digital applications," in *Proc. Symp. VLSI Technol. (VLSIT)*, Honolulu, HI, USA, Jun. 2012, pp. 133–134, doi: 10.1109/VLSIT.2012.6242497.

[2] R. Carter, J. Mazurier, L. Pirro, J.-U. Sachse, P. Baars, J. Faul, C. Grass, G. Grasshoff, P. Javorka, T. Kammler, A. Preusse, S. Nielsen, T. Heller, J. Schmidt, H. Niebojewski, P.-Y. Chou, E. Smith, E. Erben, C. Metze, C. Bao, Y. Andee, I. Aydin, S. Morvan, J. Bernard, E. Bourjot, T. Feudel, D. Harame, R. Nelluri, H.-J. Thees, L. M-Meskamp, J. Kluth, R. Mulfinger, M. Rashed, R. Taylor, C. Weintraub, J. Hoentschel, M. Vinet, J. Schaeffer, and B. Rice, "22 nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Oct. 2016, pp. 2.2.1–2.2.4, doi: 10.1109/IEDM.2016.7838029.

[3] S. Makovejev, B. K. Esfeh, V. Barral, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Wide frequency band assessment of 28 nm FDSOI technology platform for analogue and RF applications," in *Proc. 15th Int. Conf. Ultimate Integr. Silicon (ULIS)*, Stockholm, Sweden, Apr. 2014, pp. 53–56, doi: 10.1109/ULIS.2014.6813904.

[4] B. Kazemi Esfeh, V. Kilchytska, V. Barral, N. Planes, M. Haond, D. Flandre, and J.-P. Raskin, "Assessment of 28 nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements," *Solid-State Electron.*, vol. 117, pp. 130–137, Mar. 2016, doi: 10.1016/j.sse.2015.11.020.

[5] S. Makovejev, N. Planes, M. Haond, D. Flandre, J.-P. Raskin, and V. Kilchytska, "Comparison of self-heating and its effect on analogue performance in 28 nm bulk and FDSOI," *Solid-State Electron.*, vol. 115, pp. 219–224, Jan. 2016, doi: 10.1016/j.sse.2015.08.022.

[6] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730–736, Apr. 2001, doi: 10.1109/16.915707.

[7] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan, and M. J. Uren, "Impact of self-heating and thermal coupling on analog circuits in SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1037–1046, Jul. 1998, doi: 10.1109/4.701253.

[8] S. Makovejev, S. H. Olsen, and J.-P. Raskin, "RF extraction of self-heating effects in FinFETs of various geometries," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, doi: 10.1109/SIRF.2011.5719331.

[9] S. Makovejev, J.-P. Raskin, M. K. Md Arshad, D. Flandre, S. Olsen, F. Andrieu, and V. Kilchytska, "Impact of self-heating and substrate effects on small-signal output conductance in UTBB SOI MOSFETs," *Solid-State Electron.*, vol. 71, pp. 93–100, May 2012, doi: 10.1016/j.sse.2011.10.027.

[10] M. A. Karim, Y. S. Chauhan, S. Venugopalan, A. B. Sachid, D. D. Lu, B. Y. Nguyen, O. Faynot, A. M. Niknejad, and C. Hu, "Extraction of isothermal condition and thermal network in UTBB SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1306–1308, Sep. 2012, doi: 10.1109/LED.2012.2205659.

[11] N. Rinaldi, "Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, doi: 10.1109/16.902734.

[12] A. J. Scholten, G. D. J. Smit, R. M. T. Pijper, L. F. Tiemeijer, H. P. Tuinhout, J.-L. P. J. van der Steen, A. Mercha, M. Braccioli, and D. B. M. Klaassen, "Experimental assessment of self-heating in SOI FinFETs," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Oct. 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424362.

[13] R. Singh, K. Aditya, A. Veloso, B. Parvais, and A. Dixit, "Experimental evaluation of self-heating and Analog/RF FOM in GAA-nanowire FETs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3279–3285, Aug. 2019, doi: 10.1109/TED.2019.2924439.

[14] V. Kilchytska, D. Levacq, D. Lederer, J.-P. Raskin, and D. Flandre, "Floating effective back-gate effect on the small-signal output conductance of SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 414–416, Jun. 2003, doi: 10.1109/LED.2003.813373.

[15] F. Shoucair, "Design consideration in high temperature analog CMOS integrated circuits," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 9, no. 3, pp. 242–251, Sep. 1986, doi: 10.1109/TCHMT.1986.1136646.

[16] J. Martino, V. Mesquita, C. Macambira, V. Itocazu, L. Almeida, P. Agopian, E. Simoen, and C. Claeys, "Zero temperature coefficient behavior for advanced MOSFETs," in *Proc. 13th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Hangzhou, China, Oct. 2016, pp. 785–788, doi: 10.1109/ICSICT.2016.7999041.

[17] M. Emam and J.-P. Raskin, "Partially depleted SOI versus deep N-Well protected bulk-Si MOSFETs: A high-temperature RF study for low-voltage low-power applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1496–1504, Apr. 2013, doi: 10.1109/TMTT.2013.2250513.

[18] J.-P. Eggermont, D. De Ceuster, D. Flandre, B. Gentinne, P. G. A. Jespers, and J.-P. Colinge, "Design of SOI CMOS operational amplifiers for applications up to 300°C," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 179–186, Feb. 1996, doi: 10.1109/4.487994.

[19] V. Kilchytska, L. Vancaillie, and D. Flandre, "SOI technology for harsh environment applications," in *Solid State Electronics Research*, B. K. Sergo, Ed. Aichi, Japan: Nova, 2008, pp. 185–215.

[20] V. Kilchytska, S. Makovejev, S. Barraud, T. Poiroux, J.-P. Raskin, and D. Flandre, "Trigate nanowire MOSFETs analog figures of merit," *Solid-State Electron.*, vol. 112, pp. 78–84, Oct. 2015, doi: 10.1016/j.sse.2015.02.003.

[21] B. Kazemi Esfeh, N. Planes, M. Haond, J.-P. Raskin, D. Flandre, and V. Kilchytska, "28 nm FDSOI analog and RF figures of merit at N_2 cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 77–82, Sep. 2019, doi: 10.1016/j.sse.2019.03.039.

[22] L. Nyssens, A. Halder, B. K. Esfeh, N. Planes, D. Flandre, V. Kilchytska, and J.-P. Raskin, "28-nm FD-SOI CMOS RF figures of merit down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 646–654, Jun. 2020, doi: 10.1109/JEDS.2020.3002201.

[23] P. S. Barlow, R. G. Davis, and M. J. Lazarus, "Negative differential output conductance of self heated power MOSFETs," *IEE Proc. I-Solid-State Electron Devices*, vol. 133, no. 5, pp. 177–179, Oct. 1986, doi: 10.1049/ip-i-1.1986.0036.

[24] C. Enz, "MOS transistor modeling for RF integrated circuit design," in *Proc. IEEE Custom Integr. Circuits Conf.*, Orlando, FL, USA, May 2000, pp. 189–196, doi: 10.1109/CICC.2000.852646.

[25] S. H.-M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Trans. Electron Devices*, vol. 46, no. 11, pp. 2217–2227, Nov. 1999, doi: 10.1109/16.796299.

[26] I. Kwon, M. Je, K. Lee, and H. Shin, "A simple and analytical parameter-extraction method of a microwave MOSFET," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 6, pp. 1503–1509, Jun. 2002, doi: 10.1109/TMTT.2002.1006411.

[27] A. Bracale, V. Ferlet-Cavrois, N. Fel, D. Pasquet, J. L. Gautier, J. L. Pelloie, and J. du Port de Poncharra, "A new approach for soi devices small-signal parameters extraction," *Anal. Integr. Circuits Signal Process.*, vol. 25, no. 2, pp. 157–169, 2000, doi: 10.1023/A:1008332732738.

[28] K. Triantopoulos, M. Casse, S. Barraud, S. Haendler, E. Vincent, M. Vinet, F. Gaillard, and G. Ghibaudo, "Self-heating effect in FDSOI transistors down to cryogenic operation at 4.2 K," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, doi: 10.1109/TED.2019.2919924.